MODEL EFFECTIVITY	REVISIONS			
	REV	DESCRIPTION	DATE	APPROVED
	B	Replaces Rev A with change. See Revision Notice requested by ECR M03447/01 Incorporated EO's 1122D, 1372D and 1480D.	97-05-14	

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TITLE

MODIS COMMAND, TELEMETRY, SCIENCE AND ENGINEERING DESCRIPTION

SIZE	CAGE CODE	NUMBER
A	11323	151840

SCALE

SHEET 1 OF 280

X Engineering Change Request (ECR) ECR No. _____ ECR Rev. M03447/01	HUGHES AIRCRAFT CAGE Code 11323	ENGINEERING CHANGE Document No. 151840	Current Rev A	☐ Engineering Order (EO) EO No. _____ X Revision Notice (RN) Direct Incorporation

Document Title: MODIS Command, Telemetry, Science and Engineering Description

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Change Class	Other Affected Engineering Documents	Outstanding EOs	Incorp Rev	GLA/WA
☐ I X II	None	1122D 1372D 1480D	B	VJ50-222N

Item Disposition	Manufacturing Identification: Roll up to and including dwg:	Effectivity Type
X Not Applicable ☐ Items Conform Incorporate w/Deviation ☐ Incorp Change ☐ Reject	CI Effectivity: Control Item 405000 Serno 001 & Subq Control Item _____ Serno _____ & Subq	X Exact ☐ Not Later Than

Engineering Change Request Approval									
Requested by	Date	REA	Date		Date	CDMO Reviewer	Date		
J. Mehrten	5/9/97		5/13/97	C.E. Vaalter	5-14-97	Teresa M Cabrera	5-14-97		
Engineering Order/Revision Notice Approval									
Checked by	Date	Manufacturing	Date	Quality	Date	Reliability	Date		
	5/14/97		5/14/97		5/14/97		5/14/97		
Systems Engineering	Date	Project Manager	Date	Program Manager	Date	RELEASED BY:	Date		
	5/13/97						97-05-14		

Reason and Description of change:

Revisions needed to provide unique and updated PFM command, telemetry, science & engineering parameters resulting from System ambient and TV tests.

ıted EO's are incorporated plus several direct Rev B changes. For History see EO's and file copy in EDCC for direct changes.

Summary of changes: Both EO's & direct changes contain several telemetry 8 to 12 bit framing and resultant scale factor changes. EO's contain some engineering packet bit location or value changes (Tables 30-5C, 30-5D). Direct Rev B summary follows.

Basic
1. Minor text description that all ECAL occurs over Space View (vs prior PV over SD view).

Appendix A Commands
1. Clarifications for several of the 1553 bus defintion tables.
2. New Table 10-27 MODIS CP07 Mode Commands.

Appendix B Telemetry
1. Scan Assy LED Current & Encoder Amplitude Monitor 8 to 12 bit Table 20-4 Frame Changes.
2. Bit change scale factor updates & and several limit updates to Table 20-5 Active Analog Telemetry and Table 20-6 Passive Analog Telemetry.

Appendix C Science and Engineering
1. Table 30-5D change in start of Space View (EO had SD & BB view chgs)

Appendix D Command & Telemetry
1. Revised several values of Table 40-2 Control Processor Defaults.

Appendix E References
1. Add new SW reference sections 50.2, 50.3, 50.4, 50.5 & 50.6

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10. MODIS COMMAND DATA

(55 sheets, see sheet 10-1 for contents. Includes a convenience copy of Figure 11 MODIS Exploded View with Subsystem Abbreviations.)

APPENDIX B

20. MODIS TELEMETRY DATA

(68 sheets, see sheet 20-1 for contents. Includes a convenience copy of Figure 11 MODIS Exploded View with Subsystem Abbreviations.)

APPENDIX C

30. MODIS SCIENCE AND ENGINEERING DATA

(79 sheets, see sheet 30-1 for contents. Includes a convenience copy of Figure 11 MODIS Exploded View with Subsystem Abbreviations.)

APPENDIX D

40. MODIS COMMAND AND TELEMETRY RELATIONS

(26 sheets, see sheet 40-1 for contents. Includes a convenience copy of Figure 11 MODIS Exploded View with Subsystem Abbreviations.)

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1. SCOPE

1.1 Scope. This document describes the Moderate Resolution Imaging Spectroradiometer (MODIS) command, telemetry, science and engineering data. Commands and telemetry primarily flow from/to the spacecraft (S/C) via the MIL-STD-1553 bus. The science and engineering data flow to the spacecraft via the high rate link in CCSDS packets. Science data is defined as FPA sensor data. Engineering data supports science operations, and includes onboard calibrator data and other signals that are telemetry-like in form. This description document is needed to understand the overall and particular, command, telemetry, science and engineering operations of the many MODIS subsystems, including a suite of onboard calibrators. Most subsystems are fully redundant, which adds to the overall complexity.

1.2 Purpose. The release of this document continues to serve the needs of the following activities:

a. Command, telemetry, science and engineering data for instrument hardware and software development, test and system integration.

b. Interface command and telemetry data to go into EOS-AM 20008847 Command and Data Handling ICD.

c. Command, telemetry, science and engineering data to support operations planning documents

d. User's Guide of the MODIS Flight Software System (in lieu of CDRL 306J)

NOTE

Because of this common usage, some data may not be applicable to all activities. Thus, the particular user should not confuse the intent of some data or remarks that do not relate to his area of interest.

1.3 Prior CDRL continuity. This document was initially prepared to fulfill CDRL requirements (CDRL 302 commands and CDRL 305 telemetry), but did not undergo engineering release control. To preserve and facilitate user orientation to the former CDRLs, the initial engineering release included change ID to critical tables in sections 10, 20, 30 & 40. ID change history is summarized on the last pages of such tables. Text generally has right side change bars for the latest revision.

1.4 Structure and content. The document has always been formatted in a specification style to facilitate its release as a controlled document. Its structure was established to easily accept evolving details. It is structured as a main body and five focused appendices as follows (also shown in Table 1):

a. This front body provides an overview of MODIS, operating modes, scan cycle timing, MIL-STD-1553B Command and Telemetry Bus, and high rate science link packet description.

b. Appendix A addresses commands. It contains direct S/C commands, 1553 bus command definitions, lists, formats, support tables, and command constraints.

c. Appendix B addresses telemetry. It contains the basic telemetry list, definitions, formats, frame description, alarm limits, and scale factor equations.

d. Appendix C addresses science data, which is FPA sensor data, and engineering data, which is related to interpretation of sensor data and onboard calibrator data. It includes details of the CSSDS packets.

e. Appendix D addresses command and telemetry verification relations.

f. Appendix E contains miscellaneous data, or points to references, that might apply to any part of this document.

g. Most appendices contain some information that relates directly to software design contained in 152930 Flight Software Detailed Design (CDRL F306E, DM VJ50-0125).

NOTE

- *Some points appear in both housekeeping telemetry and engineering data to facilitate test control operations.*
- *This document does not contain command procedures/sequences. It only contains the tools used to generate them. Command procedures will be defined in CDRL 405 General Operating Command Procedures.*

1.5 Document format conventions Some document formats deviate from specification style formats to facilitate the use of many tables and growth. Arabic numbers are used for all tables, e.g., Table 1, 2, Table 10-1, 10-2, etc, and appendices use local page numbering, e.g., 10-1, 20-1 and 30-1.

TABLE 1. DOCUMENT CONTENTS - WHERE IS IT?

MAIN BODY GENERAL	APPENDIX A COMMAND DATA	APPENDIX B TELEMETRY DATA
• Scope/Structure • MODIS Description & Diagrams • Operational Modes • Scan Cycle • 1553 Bus Overview • C & T Abbreviations	• Command Implementation • Command Flow Diagrams • S/C Pt-Pt Commands • 1553 Bus Commands • Bus Command Structures • Command Constraints • Command Lists	• Telemetry Implementation • Telemetry Flow Diagrams • S/C Pt-Pt Telemetry • 1553 Bus Telemetry • Telemetry List • Frame Structure • Scale Factors/Limits • Temperature Sensors
APPENDIX C SCIENCE & ENGINEERING DATA	**APPENDIX D COMMAND & TELEMETRY RELATIONS**	**APPENDIX E MISCELLANEOUS REFERENCE DATA**
• Band Registration • Unformatted FPA Data • Formatted FPA Data • Science Packets • Engineering Data	• Commands & Related Tlmy • Related Engineering Data • Redundandcies & Dependancies • Processor Defaults • Processor Event Codes	• Background Memos • Supplemental FYI data

2. APPLICABLE DOCUMENTS

2.1 Government documents. The following documents of the issue in effect, or of the specific issue date indicated, form a part of this specification to the extent specified herein.

SPECIFICATIONS

Goddard Space Flight Center (GSFC), Greenbelt, MD 20771

420-03-02	General Instrument Interfaces Specification (GIIS) for the EOS Observatory
421-12-04-01	Unique Instrument Interface Document, MODIS, EOS-AM Project
422-20-02	Specification for the Moderate-Resolution Imaging Spectroradiometer (MODIS)

STANDARDS

Military

MIL-STD-1553B	Aircraft Internal Time Division Command/Response Multiplex Data Bus

2.2 Non-Government documents. The following documents of the issue in effect, or of the specific issue date indicated, form a part of this specification to the extent specified herein.

SPECIFICATIONS

SBRC

151759	Moderate Resolution Imaging Spectroradiometer (MODIS) Instrument, System Specification For
151783	Analog Electronics Module, Space View, Specification For
151784	Analog Electronics Module, Forward View, Specification For
151785	Main Electronics Module, Specification For
152929	MODIS Flight Software System Architecture Document (CDRL F306D)
152930	MODIS Flight Software Detailed Design (CDRL F306E)
152932	Maintenance Manual of the MODIS Flight Software System

OTHER PUBLICATIONS

Lockheed Martin Missiles & Space, Valley Forge Operations, PA

20008847	MODIS Command and Data Handling ICD
EOS-DN-C&DH-048	Command and Telemetry Bus Utilization Table

SBRC

DM VJ50-0068	General Operating Command Procedure (CDRL 405)

3. MODIS DESCRIPTION

3.1 General description. MODIS is designed to make long-term spectral observations of the earth's land surface, ocean surface layer and lower atmosphere. It is a passive imaging spectroradiometer, which views the earth, calibration devices and space by means of a continuously rotating scan mirror as illustrated in Figure 1. It collects data from both sides of the scan mirror with four focal plane assemblies (FPAs) containing 36 bands spread over 5 spectral regions (412 nm to 14,235 nm). Ground Nadir resolution varies with 29 bands at 1000 m, 5 at 500 m, and 2 at 250 m. The number of detectors per band are 10 for 1000 m resolution bands, 20 for 500 m, and 40 for 250 m. In addition, 2 of the 1000 m bands have a set of TDI detectors, which results in a total of 490 detectors. A total of 990 raw samples are collected due to multiple samples from some bands. A total of 830 samples are sent to the ground after on-board processing by the formatter to combine multiple samples and to reorder samples for spatial registration. Due to the inherent FPA band layout offsets, 30 frames of data have to be collected and stored until this aligned sample set can be formatted. At a 705 km orbit, the optical arrangement and scan mirror coverage of ±55° from Nadir, result in a cross track swath of 2330 km and an along track swath of 10 km at Nadir. MODIS has stringent radiometric, spectral center, spectral bandwidth, and spatial registration requirements. After on-orbit activation, MODIS will continuously collect science data, except during periodic S/C orbital adjustments. See Figures 1 to 4 for an overall perspective of MODIS.

MODIS also has four high performance onboard calibrators: an ambient or heated Blackbody (BB); a Solar Diffuser (SD) with 2 output levels of reflectance obtained by limiting the solar input to the SD via a commandable 8.5% transmission screen, a Solar Diffuser Stability Monitor (SDSM), which compares the Solar Diffuser reflectance to direct solar view with a fixed 2% transmission screen, and a Spectral Radiometric Calibration Assembly (SRCA) which operates in 4 modes (spectral, spectral self calibration, spatial, and radiometric). In addition to these calibrators, MODIS has an electronic calibration available, which provides a stair step signal. The PV FPAs, Bands 1-30, temporarily disconnects the FPA sensors for this calibration, but the PC FPA, Bands 31-36, remain connected. Electronic calibration collects occur over the cold space view for both PV FPA Bands (positive steps) and PC FPA Bands (negative steps). See Figures 5 to 7 for a perspective of the calibrators.

The general physical electrical interface between the EOS-AM Spacecraft and MODIS is illustrated by Figure 8. The MODIS internal interconnect diagram is shown in Figure 9. Figure 10 presents the MODIS Electronics Block Diagram. The major subsystems addressed by this document are shown in this diagram. There are two microprocessors contained in MODIS. The first is the Command and Telemetry Processor (CP). The other processor is the Format Controller. The Format Controller together with the hardware Format Engine form the Formatter (FR), which formats science and engineering data into CCSDS packets to be sent over the high rate data link.

Table 2 summarizes the top MODIS requirements (details in GSFC 422-20-02), and Table 3 summarizes the MODIS top baseline parameters to fulfill the requirements.

3.2 Functional description. The hardware functional elements of MODIS are shown by its interconnect diagram in Figure 9, which can be matched up with the functional design depicted in Figure 3. Additional electronic block diagram detail is shown in Figure 10. An exploded view of MODIS hardware is shown in Figure 11 (which also serves as a vehicle to show 2-character subsystem abbreviations). The SWIR/MWIR and LWIR FPAs are cooled to ~85 K by the passive radiative cooler. The PV FPAs produce sampled analog output signals, which are buffered and digitized by the Space View Analog Module (SAM). PC detectors on the LWIR FPA produce continuous analog signals, which are preamplified by the Cooler Located Amplifier Module (CLAM, not separately depicted in Figure 2), then post amplified, integrated and digitized by the Forward View Analog Module (FAM).

The Formatter, first-in-first out (FIFO) memory buffer and Fiber Distributed Data Interface (FDDI) circuits form a digital processing chain that formats the sensor signals and related engineering data into CCSDS science packets, buffers them to smooth out data transmission peaks, and sends them over the high rate science link to the spacecraft (S/C).

A limited number of command and telemetry signals are processed directly by the S/C Bus Data Unit (BDU) point-to-point controls. The bulk of command and telemetry signals flow over the MIL-STD-1553 bus, and are processed by the Command & Telemetry microprocessor (CP). The S/C BDU directly controls the CP's and power supplies. The CP provides general control over all other subsystems, which are not controlled by the S/C BDU. The CP contains the master system clock (48 MHz), which is counted down to 12 MHz for the single board computers in the CP and the Formatter. Digital telemetry circuits are contained on one of the two boards that form the CP single board computer. Analog telemetry circuits are packaged on a separate board but its functions are associated with the CP, including its power control.

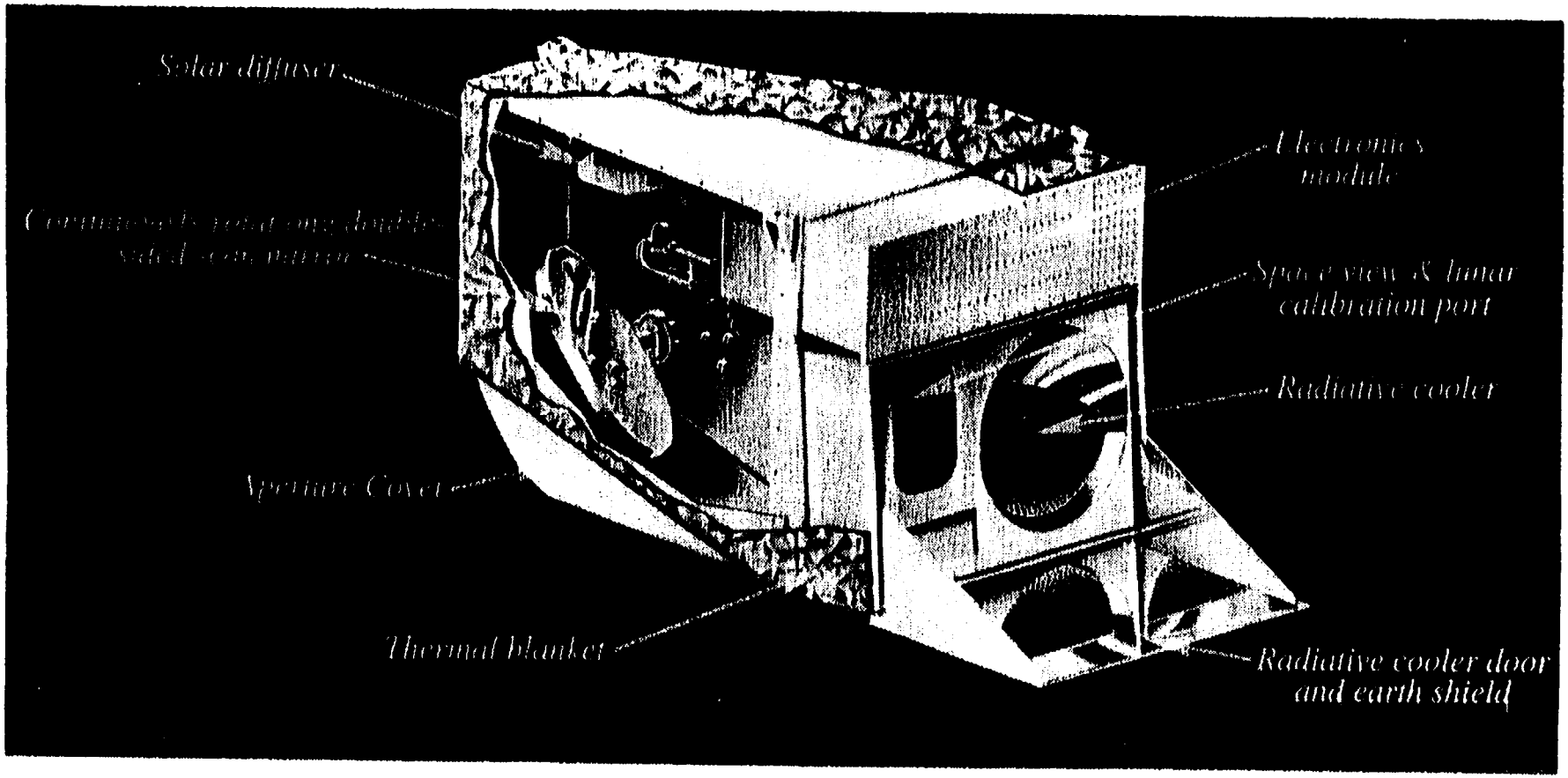
A 9.6 MHz clock is provided to the Timing Generator from the CP, which generates the various frame and pixel clocks sent to the Formatter, FAM and SAM analog modules, and scan mirror drive electronics.

Other controllers within the MEM provide scan mirror drive, mechanism control of doors, temperature control of CFPA and outgas heaters, and control of on-board calibrators and related mechanisms.

For a description of the MODIS software architecture see 152929 MODIS Flight Software System Architecture Document (CDRL F306D). For a description of the MODIS software detail design, see 152930 MODIS Flight Software Detailed Design (CDRL F306E).

- 36 Spectral Bands
- 4 On-Board Calibrators
- Weight ≤ 250 kg
- Average Power ≤ 225 watts
- Peak Power ≤ 275 watts

- Day Data Rate = 10.6 Mbps
- Night Data Rate = 3.2 Mbps
- Orbital velocity is +X (to right in figure)
- Radiative Cooler looks to +Y cold space
- Aperture looks to +Z Nadir



MODERATE RESOLUTION IMAGING SPECTRORADIOMETER

Figure 1. MODIS

Equatorial Radius = 6378.17 m
Earth Rotation Rate = 0.4651 km/s
Orbit Altitude = 705.295
Orbit Inclination = 98.21°
Ground Velocity = 6.75457 km/s

IFOV = 1 km/705.295 km = 1.41785 mr
IFOV = 0.5 km/705.295 km = 0.708923 mr
IFOV = 0.25 km/705.295 km = 0.354462 mr

Dwell Time = 333.333 μs, (48 MHz Master Osc.)
166.667 μs, 83.3333 μs

Object Space Scan Rate =
1.41785 mr/333.333 μs = 4.25354 r/s
Object Space Scan Period = 1.47717 s

Swath Width = 10 km
Distance Along-Track Per Scan = 9.92426 km
Sampling Gap Along Track = 0.0757 m (Worst Case)

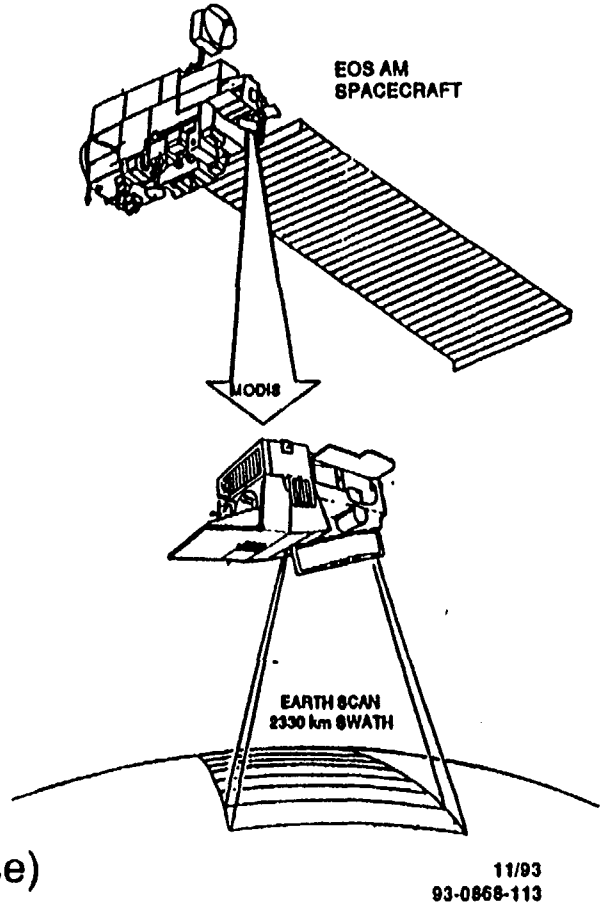


Figure 2. MODIS Orbital Features

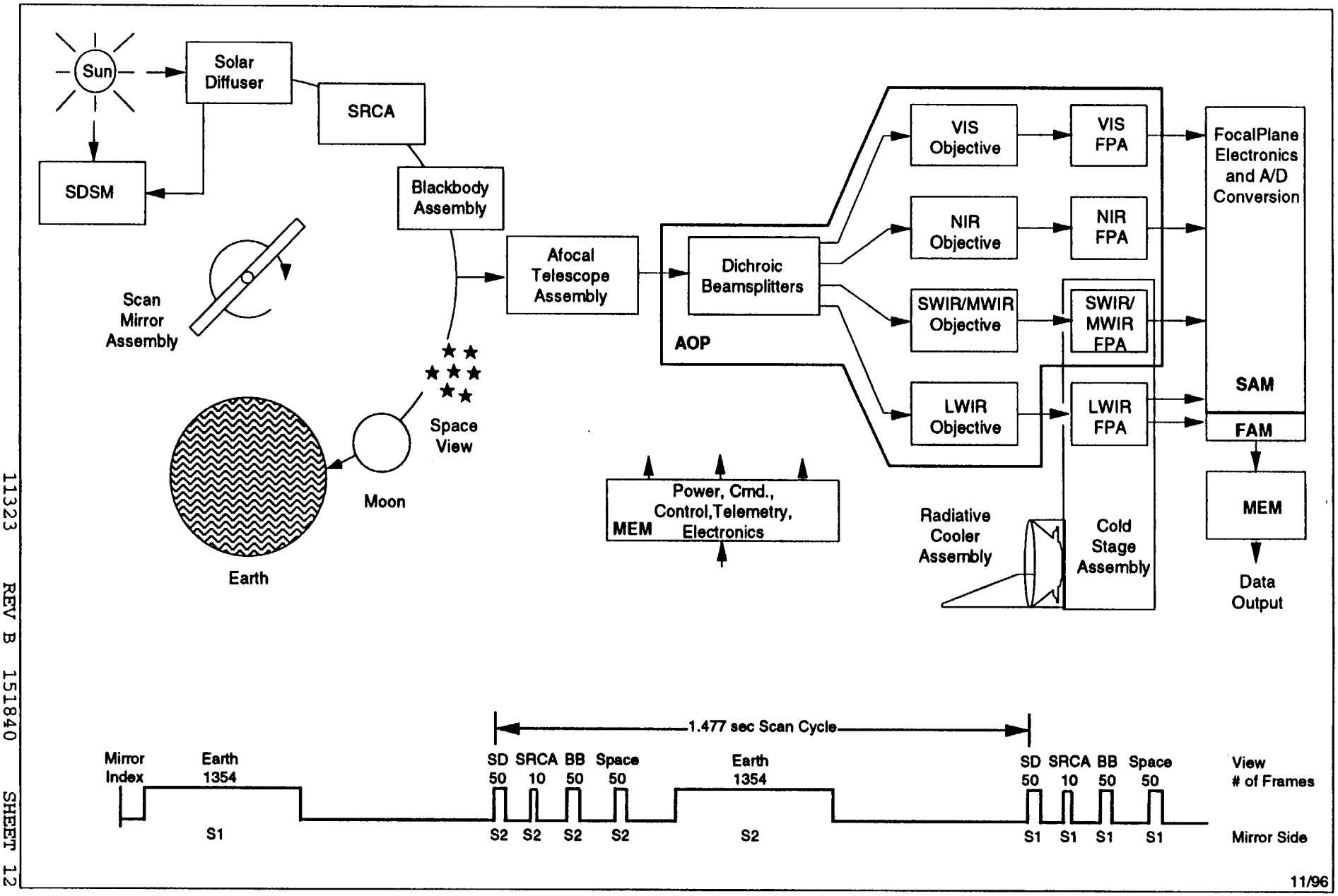


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Figure 3. MODIS Functional Design

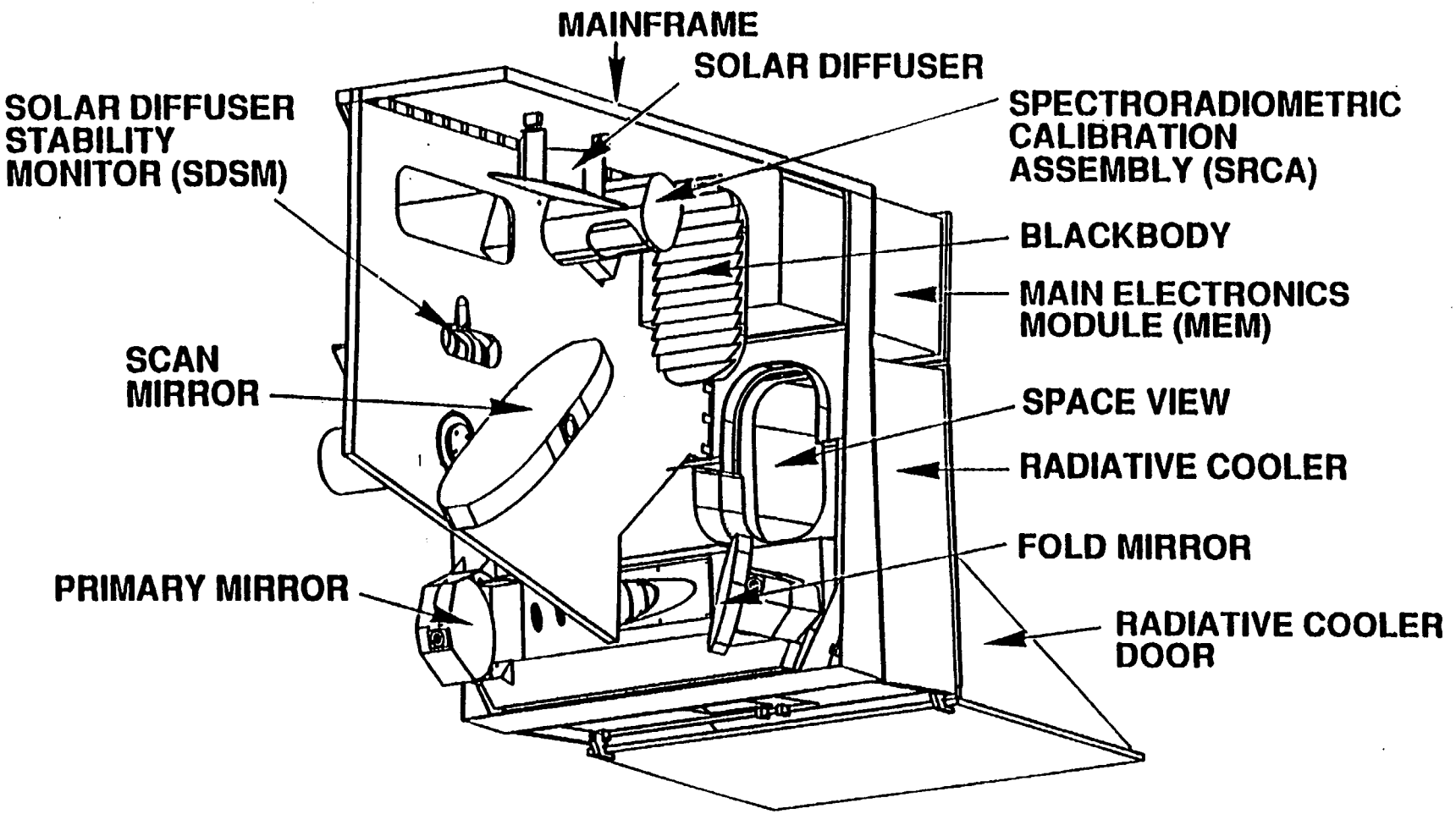


Figure 4. MODIS Scan Cavity View

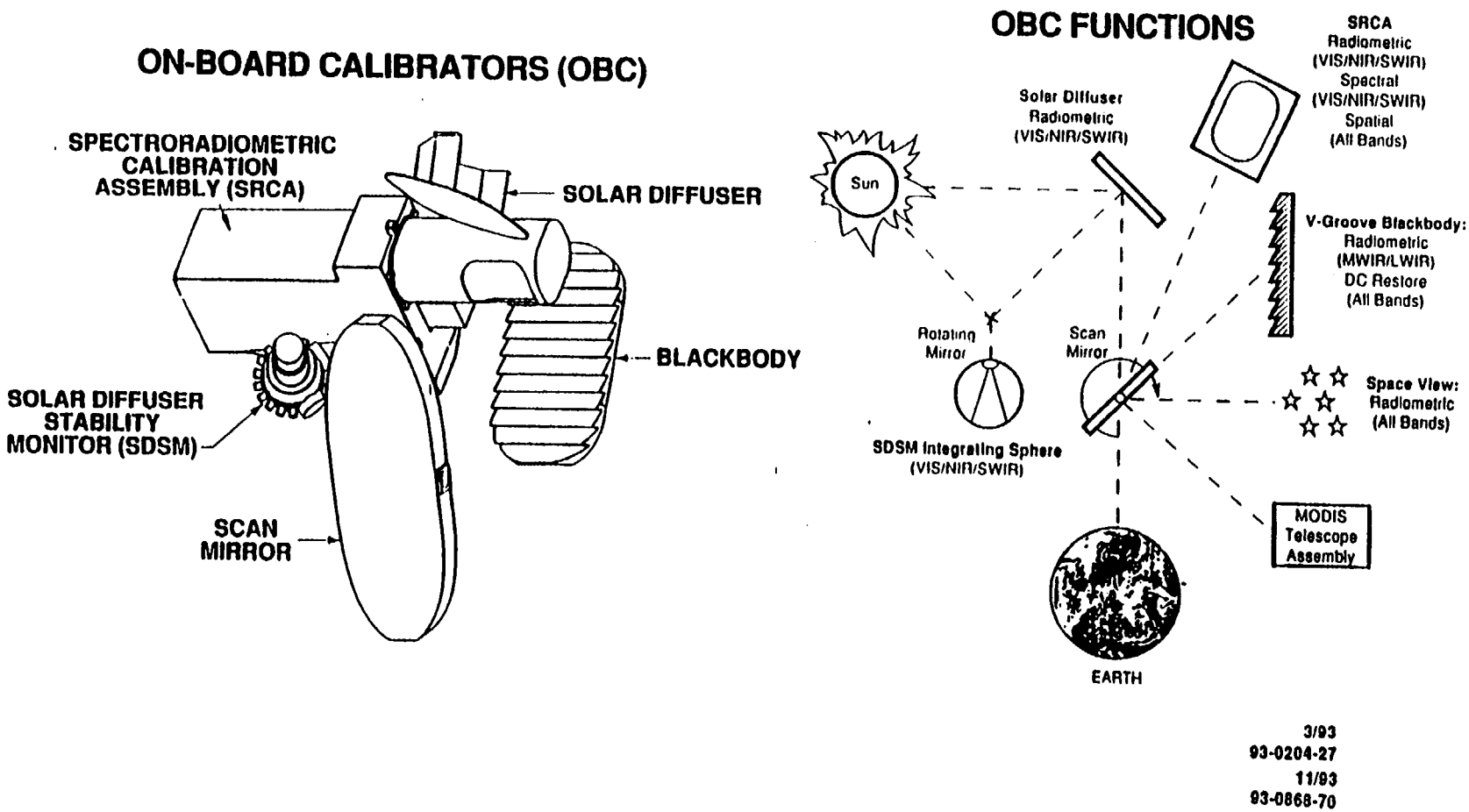
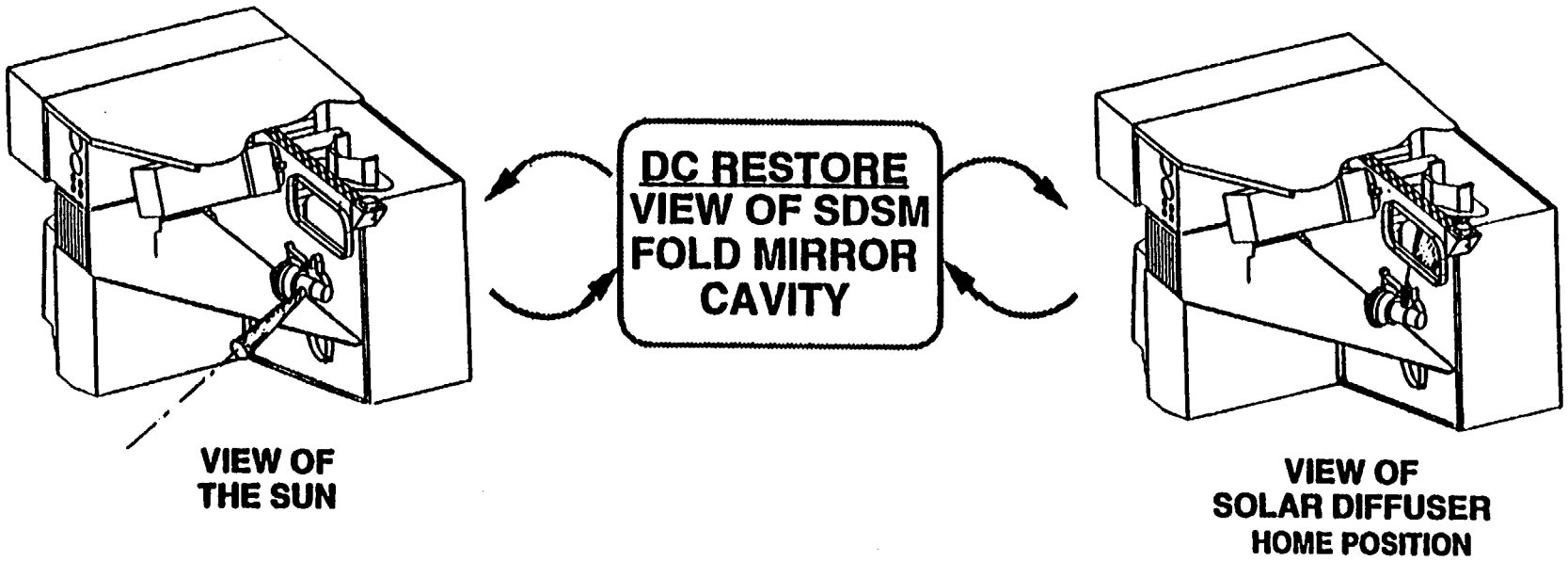
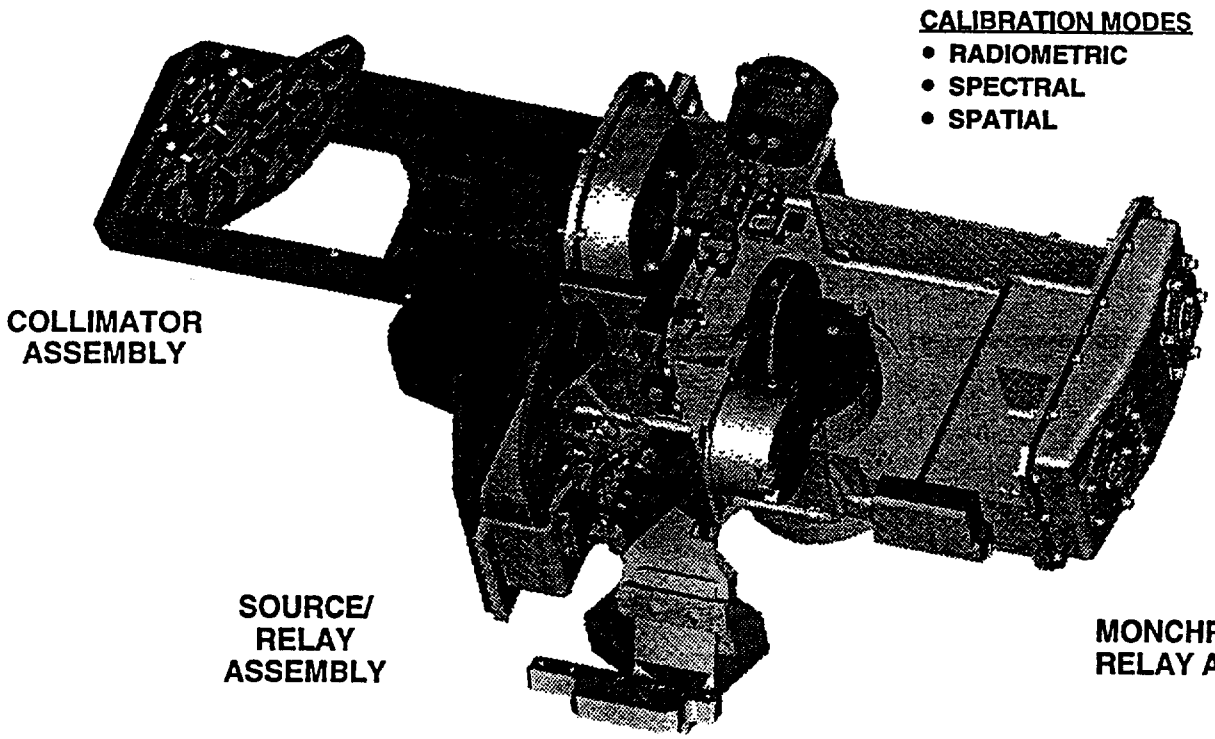


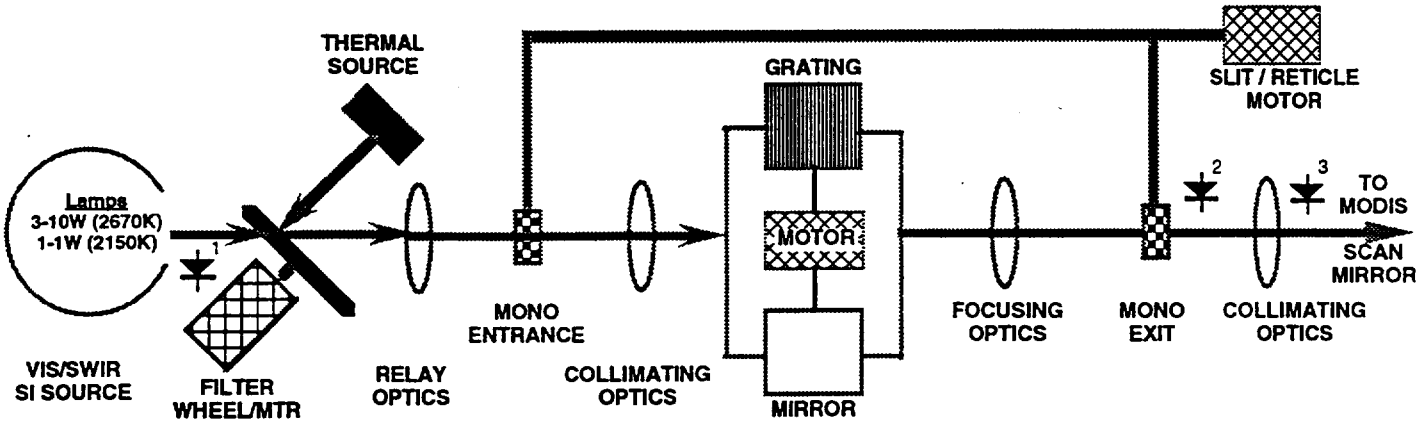
Figure 5. Calibrator Functional Views



- SDSM INFORMATION AVAILABLE WHENEVER CALIBRATION USING SOLAR DIFFUSER IS PERFORMED (AVAILABLE ONCE PER ORBIT FOR A MINIMUM OF 1 MINUTE DURATION).
- MULTIPLE SAMPLES COLLECTED PER SDSM VIEW FOR ALL 9 DETECTORS.
- FREQUENCY FOR SUN AND SOLAR DIFFUSER VIEWING IS APPROXIMATELY 10 CYCLES PER MINUTE.

Figure 6. SDSM Three Views





DETECTORS: 1 = SIS FEEDBACK CONTROL, 2 = DIDYMIUM SPECTRAL SELF CAL , 3 = SPECTRAL REFERENCE

CALIBRATION MODE	SOURCE	FILTER	MONO ENTRANCE	GRATING / MIRROR	MONO EXIT	TIME REQD Minutes
RADIOMETRIC	VIS/SWIR	CLEAR & ND	OPEN	MIRROR	OPEN	44
SPECTRAL	VIS/SWIR	ORDER (3)	SLIT	GRATING	SLIT / SIPDs	126(30W),136(10W)
SPATIAL	VIS/SWIR & THERM	ITO DICHROIC	OPEN	MIRROR	RETICLES	65

Figure 7. SRCA Calibration Modes & Internal View

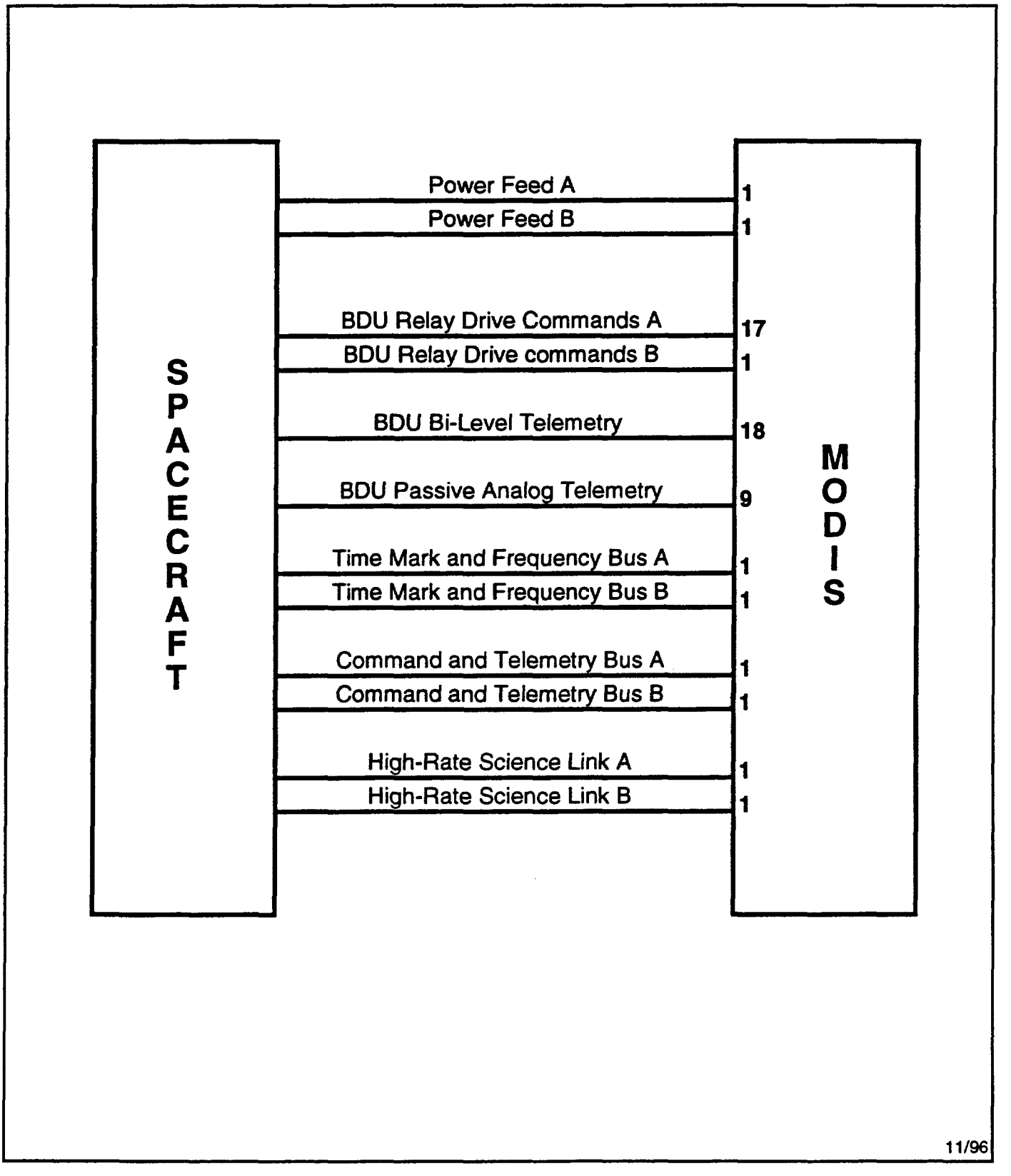


Figure 8. Spacecraft/MODIS Physical Electrical Interfaces

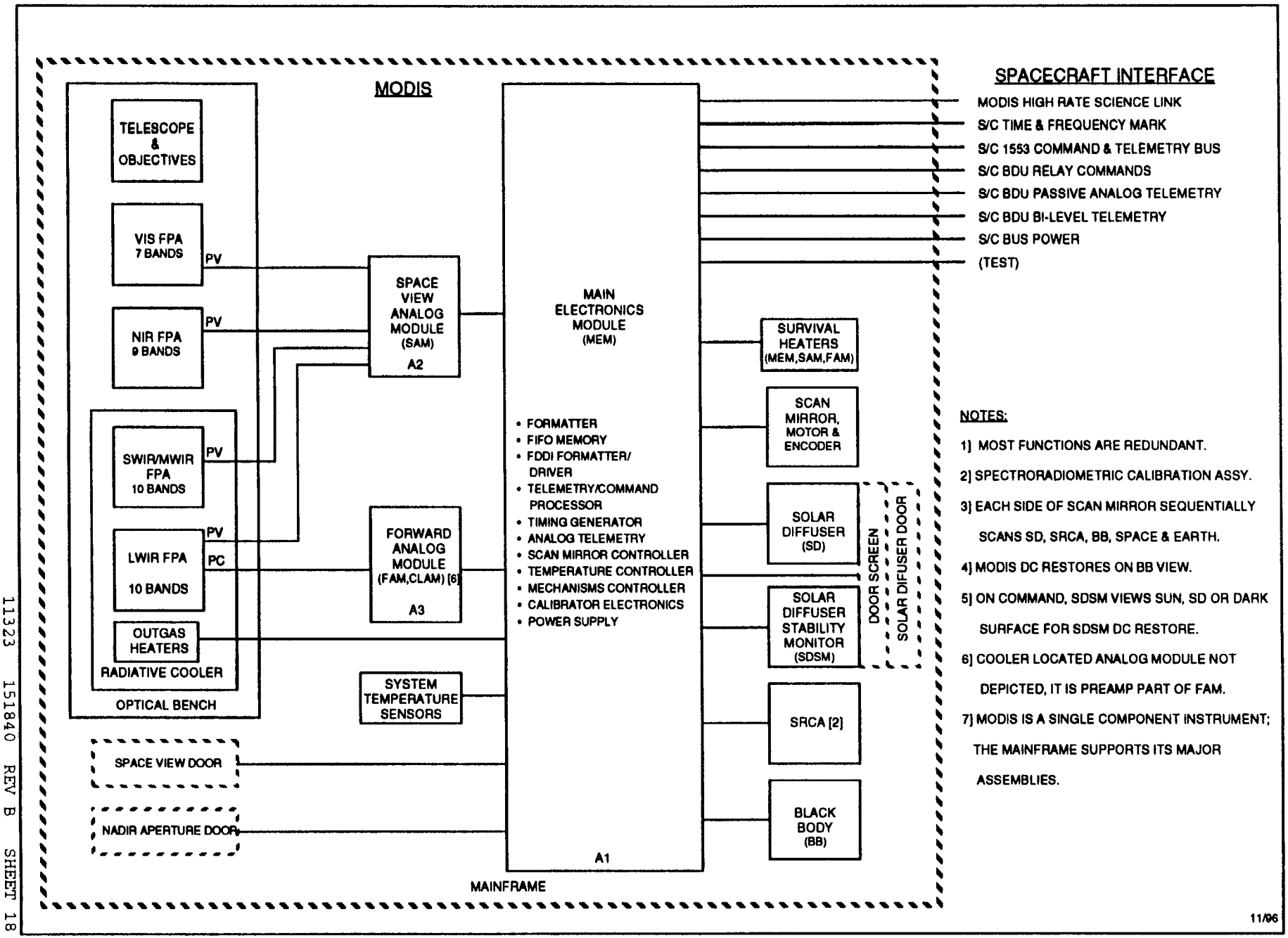


Figure 9. MODIS Interconnect Diagram

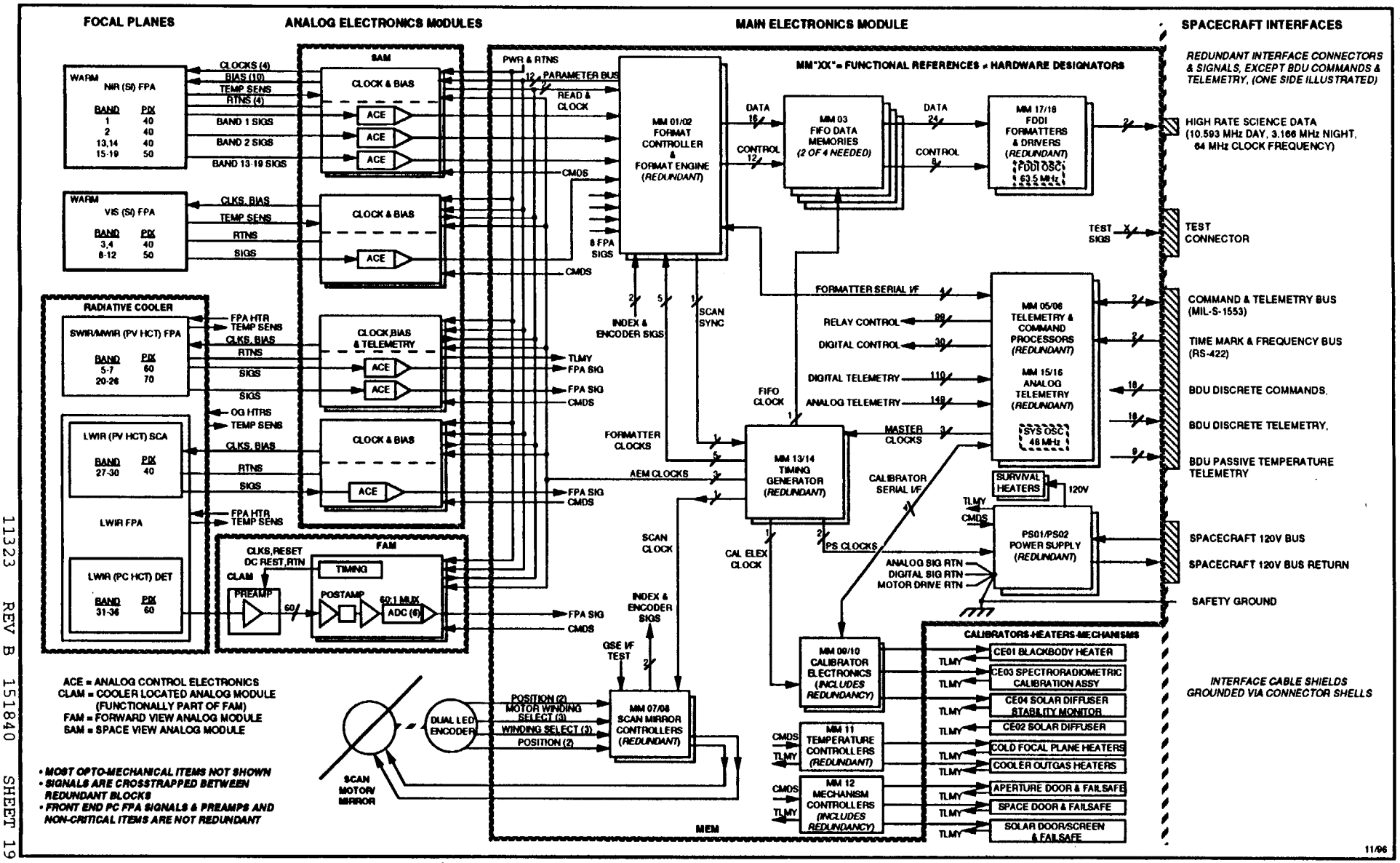


Figure 10. MODIS Electronics Block Diagram

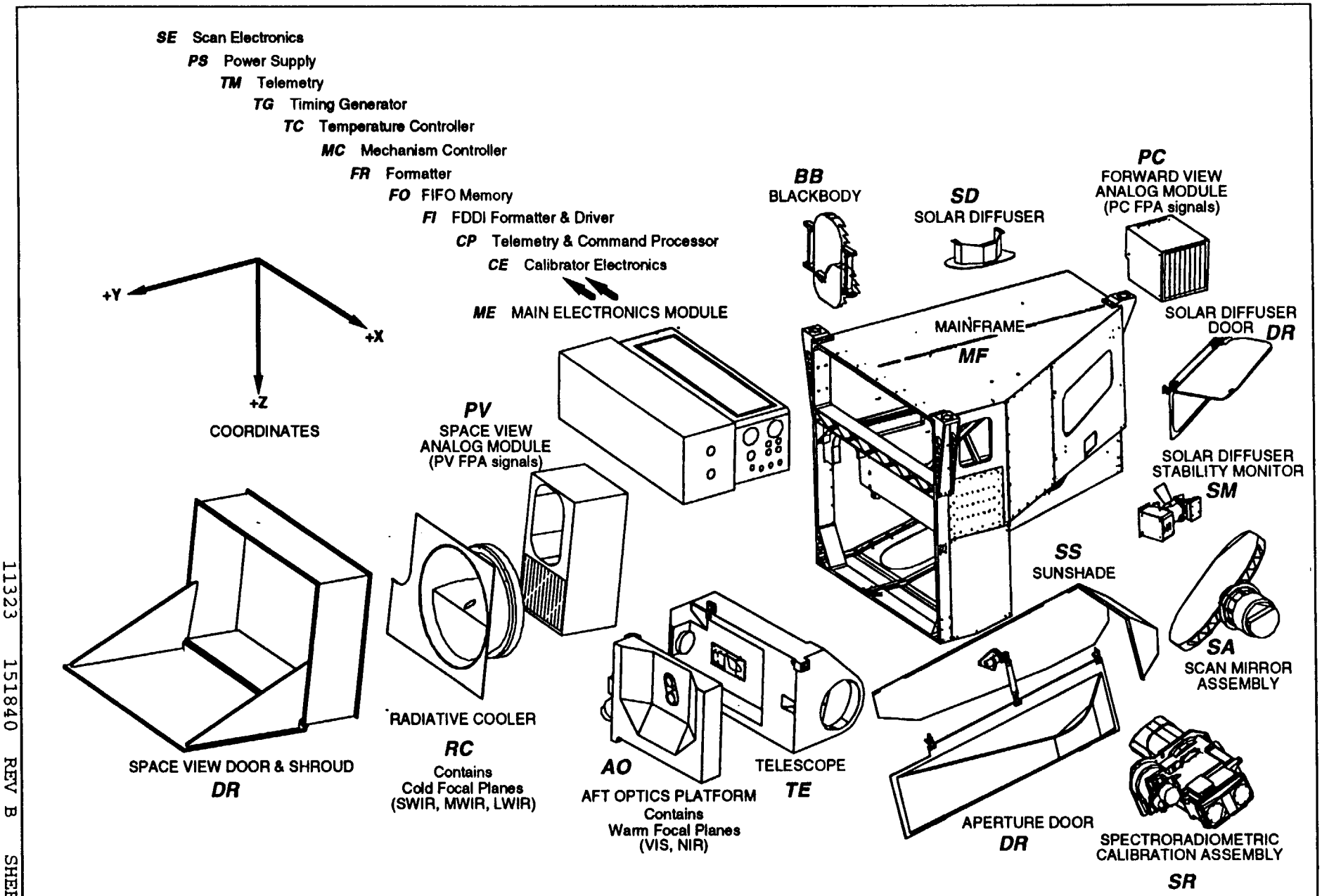


Figure 11. MODIS Exploded View With Subsystem Abbreviations

TABLE 2. MODIS REQUIREMENTS

• Spectral Coverage	• 0.412 μm - 14.235 μm, 36 bands
• Spectral Resolution	• 10 nm ≤ Δλ ≤ 500 nm
• SPECTRAL Stability	• λ & Δλ Stable to ≤ 2 nm (VIS, NIR) λ & Δλ Stable to ≤ 1% (All Other Bands)
• Spatial coverage	• ±55°, 2330 km Swath Length At 705 km (Contiguous Nadir Scans at the Equator)
• Spatial Resolution	• 250 m, 500 m, 1000 m at Nadir
• Spatial Registration	• 0.2 IFOV (0.1 IFOV goal)
• IFOV	• 0.354 mr, 0.709 mr, 1.418 mr (All ±6%)
• Radiometric Range	• 0.002% ≤ ρ ≤ 100%, 3K ≤ T ≤ 700K
• Dynamic Range	• NEΔL to Lmax (requires 12 bits)
• Radiometric Performance	• ≥ 57 to 1087, ≤ 5.0 to 0.05K
• Polarization Isolation	• ≤ 2%, 0.43 μm ≤ λ ≤ 2.2 μm
• Calibration Accuracy	• Absolute Calibration: ±1% λ > 3 μm; ±5% λ < 3 μm; ±0.75% Band 20; ±0.5% Bands 31, 32; ±2% Reflectance (λ < 3 μm)

TABLE 3. MODIS BASELINE PARAMETERS

• Orbit	• 705 km 10:30 AM Descending
• Swath	• ±55°, 10 km Track x 2330 km Scan
• Scanning	• 360° Scan, Double Sided, 20.3 RPM, 2.954 Sec Period
• IFOV	• 0.354 mr(0.25 km), 0.709 mr(0.50 km), 1.418 MR(1 km)
• Dwell Time	• 83.3 μS(0.25 km), 166.7 μS(0.50 km), 333.3 μS(1 km)
• Telescope	• 2-Mirror Off-AXIS Afocal Gregorian, 4X Magnification, EPD 17.8 cm
• Reimaging Optics	• Refractive, EFL 380.8 mm, 282.1 mm (LWIR Only)
• Spectral	• 36 Bands From 0.412 μm to 14.235 μm, Dichroic Beamsplitters, Bandpass Filters
• Focal Planes	• Silicon (0.4 μm ≤ λ ≤ 1 μm), PV HgCdTe (1 μm ≤ λ ≤ 10 μm); PC HgCdTe (λ > 10 μm), CTIA Readouts For PV, Bipolar Preamps For PC
• Detector Sizes	• Nominally Square: 135 μm (0.25 km), 270 μm (0.5 km), 540(400 LWIR) μm (1.0 km)
• Detector Cooling	• Three Stage Radiative Coller, T≈85K
• Calibration	• Laboratory, Ground Truth, On-Board Blackbody, Solar Diffuser, SRCA, And SDSM
• Data Rates	• 10.6 MBPS Day Mode, 3.2 MBPS Night Mode, With CAL And Overhead
• Size, Weight, Power	• 0.97 m x 1.59 m x 0.99 m, 224 kg, 225 W (90 W Science margin)

4. MODIS OPERATIONAL MODES

4.1 Operational mode definition. Table 4 identifies the MODIS Operational Modes. Operational modes define subsystem configurations to perform particular mission functions, and have particular related power loads. The science data rate is either the day rate (10.6 MHz) or the night rate (3.2 MHz). The power is the same at either rate because all bands are on in order to collect all band data from the on-board calibrators (OBC). The operational modes are independent of whether side A or side B is used in the case of redundant subsystems, or if a mix is used. However, for simplicity of operations, Side A items have been selected for initial flight software coding for 1553 bus CP07 mode commands. Memory upload changes or external command sequences can bring any redundant command selections on line. CDRL 405 General Operating Command Procedures addresses which commands are needed to establish the operational modes defined in Table 4.

The MODIS operational modes are indicated in Figure 12.

TABLE 4. MODIS OPERATIONAL MODES

Mode	Mode Description
Launch	No operational or survival power for 2 hrs; survival power on by 6 hrs; doors closed and latched for launch.
Survival	No operational power; survival heaters enabled (MEM, SAM, & FAM); doors closed.
Safe	Power ON 1/; survival heaters enabled; doors closed as S/C attitude may not be controlled; minimum power 1553 telemetry monitor state with command capability.
Standby (utility activity)	Power ON 1/; doors open or closed; any utility activity: e.g. mechanism failsafe activation; fault isolation operations; short term delays; major memory uploads.
Outgas & Science	Power ON 1/ Outgas with 2 OG htrs and open space & nadir doors for VIS & NIR Science. (Outgas with 3 OG htrs and no imaging is a Standby utility activity>)
Science	Power ON 1/; all bands on; ~10.6 Mbps day rate has all Band 1-36 scene data in 2 science packets; engineering data in 4 packets. ~3.2 Mbps night rate all bands on; only Band 20-36 scene data in 1 science packet for earth; engineering data in 4 packets.
Science choices	- Solar Diffuser data with SD door/screen open. - SD Stability Monitor data of SD, SDSM black surface, sun for VIS/NIR/SWIR bands. - SRCA spectral calibration for VIS/NIR/SWIR bands. - SRCA radiometric calibration for VIS/NIR/SWIR bands. - SRCA spatial calibration for all bands. - Blackbody heated (DC restore on all bands heated or ambient). - Electronic calibration (ECAL) stair steps over space view sector; PV bands positive steps; PC bands negative steps; PC/PV together or separately - Science link Test/Operate: fixed pkt to check link

1/ The 1553 command & telemetry bus is available anytime MODIS power is ON.

NOTE

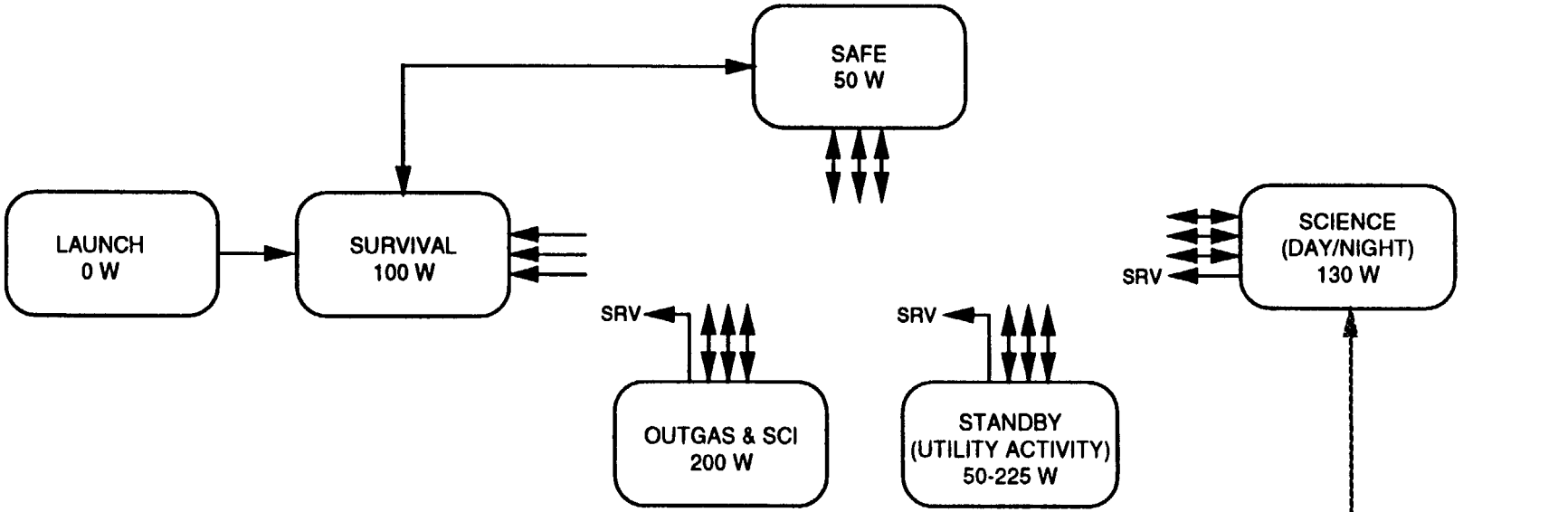
These are the normal mode functions established by 1553 bus command CP07 mode selections, or external command sequences. Utility variations to the Standby Mode require external command sequences and/or TBD flight command macros. Initial flight SW CP07 command sequences will be based on Side-A selections.

4.2 Operational mode power. MODIS power allocations, as specified in GSFC 421-12-04-01, are as follows. The MODIS 1-orbit average power limit shall not exceed 230 W. The specified 2-orbit average limit is 225 W. Peak power shall not exceed 285 W.

The average power estimated at 120V nominal bus voltage for each operational mode is indicated in Table 5.

TABLE 5. MODIS OPERATIONAL MODES AVERAGE POWER

Mode	Average Power (Nominal 120V Bus) - Watts
Launch	0
Survival	≤100 for MEM, SAM & FAM heaters, ~80 at equilibrium
Safe	≤225 minimum configuration, normally ≤50
Standby (utility activity)	≤225 configuration dependent, normally 50 - 225 door unlatch, 3-OG heater outgas, pseudo science, failsafe, etc
Outgas & Science	≤225 2-OG heater outgas and VIS & NIR science, ~200
Science	≤135, Science w/o calibration
- SD	≤135
- SDSM	≤140 10 min orbit duty cycle
- SRCA spectral	≤178 54 percent lamp use factor over 72 min orbit duty cycle
- SRCA radiometric	≤160 39 percent lamp use factor over 57 min orbit duty cycle
- SRCA spatial	≤175 48 percent lamp use factor over 78 min orbit duty cycle
- BB heated	≤162 continuous orbit
- ECAL	≤135



NOTES:

1. Chart defines on-orbit MODIS Operating Modes. Side A is arbitrary primary choice.
2. SURVIVAL Entry & Exit to SAFE requires spacecraft BDU pt-pt commands.

   Remaining Modes are established by 1553 bus command CP07 Flight SW sequences.
3. Standby reflects the prior Mode except for high power items (OBC's & outgas heaters).

   Standby also supports all utility activities as augmented by ground commands.
4. Mode changes are only by spacecraft command (including SAFE by missing "SCC IMOK").
5. SURVIVAL & SAFE Modes allow 30 seconds to close all doors.
6. Science data rates are DAY = 10.6 Mbps & NIGHT = 3.2 Mbps.
7. Survival Heaters are enabled between 2 & 6 hours after launch, then On at all times.
8. 1553 Bus telemetry is available from MODIS whenever either power supply is ON

Five Variable Calibration Configurations

- Solar Diffuser View
  - None
  - SD (0 W)
  - SDSM (2 W)
  - Bands 1-30 Elec Cal (0 W)
- Spectroradiometric Assembly View
  - None
  - Spectral (48 W)
  - Radiometric (26 W)
  - Registration (38 W)
- Black Body View
  - Ambient (0 W)
  - Heated (31 W)
- Space View
  - Normal (0 W)
  - Bands 31-36 Elec Cal (0 W)
  - Lunar View (0 W)
- Science Link Test Pattern (0 W)

11/96

Figure 12. MODIS Operational Modes

5. MODIS SCAN CYCLE/1553 BUS RELATIONS

The MODIS 1.477 second scan cycle synchronizes the 333.3 μs electronic pixel sample clock to each view, but it runs nonsynchronous to the 1.024 second major cycle of the MIL-STD-1553 Command and Telemetry bus. The relation of these three items is described below.

5.1 MODIS scan sector synchronization. The double-sided scan mirror has a period of 2.954 seconds which produces a 1.477 second side 1 scan cycle and a 1.477 second side 2 scan cycle. During each 1.477 second scan cycle, 5 view sectors (solar diffuser, SRCA, blackbody, space and earth) are observed. For each view, the formatter synchronizes the pixel sample clock (333.3 μs) to the scan by resetting it based on the combination count of the number of scan mirror encoder pulses (180.3 μs) since the mirror index pulse, plus a number of vernier clock pulses (6.6 μs). The pixel sample clock is actually reset 3 sample times before the view sector to allow it to settle from the reset transient. Only one mirror index pulse occurs per mirror revolution, which contains 16,384 encoder pulses. Figure 13 illustrates the view sectors in a pie chart form and a time line scan cycle. The start of a scan cycle is defined as the start of the SD view sector. Details of encoder counts and vernier counts for each view sector can be found in the SBRC 151785 MODIS MEM Specification.

5.2 Scan cycle activities. MODIS internal control activities are synchronized to the 1.477 second scan cycle. As a general guide, many CP tasks are held in abeyance whenever FPA sensor data is being collected, in order to minimize the chance of noise corrupting the sensor data. Thus, main scan cycle tasks are as follows:

a. Commands can be received any time over the 1553 bus, but in Science Mode they may not be immediately executed. In particular, commands to move mechanisms will only occur between view sectors.

b. FPA sensor data is collected, formatted into CCSDS science packets and sent to the S/C throughout all the view sectors. Transmission to the S/C continues past the view sectors until the buffered FIFO data has emptied.

c. Science engineering data packets are only sent to the S/C once per scan cycle at the end of the earth scan.

d. DC restore data is calculated from blackbody view sensor data, and the results are applied between earth and solar diffuser views.

e. Acquisition of internal telemetry data occurs after the end of earth view, and is placed in a buffer for downloading to the S/C at the 1553 bus major cycle rate of 1.024 seconds/cycle. The 1553 bus acquisition at the 1.024 second rate will result in "old" data occasionally due to the slower 1.477 MODIS scan rate. There are no critical functions affected by this. In Figure 13, major cycle M is marginally too soon to pick up the telemetry data from the scan above it, so the prior telemetry collect will be used. Major cycles M+1 and M+2 will both have updated data. In all cases Major Cycle number count is consecutive.

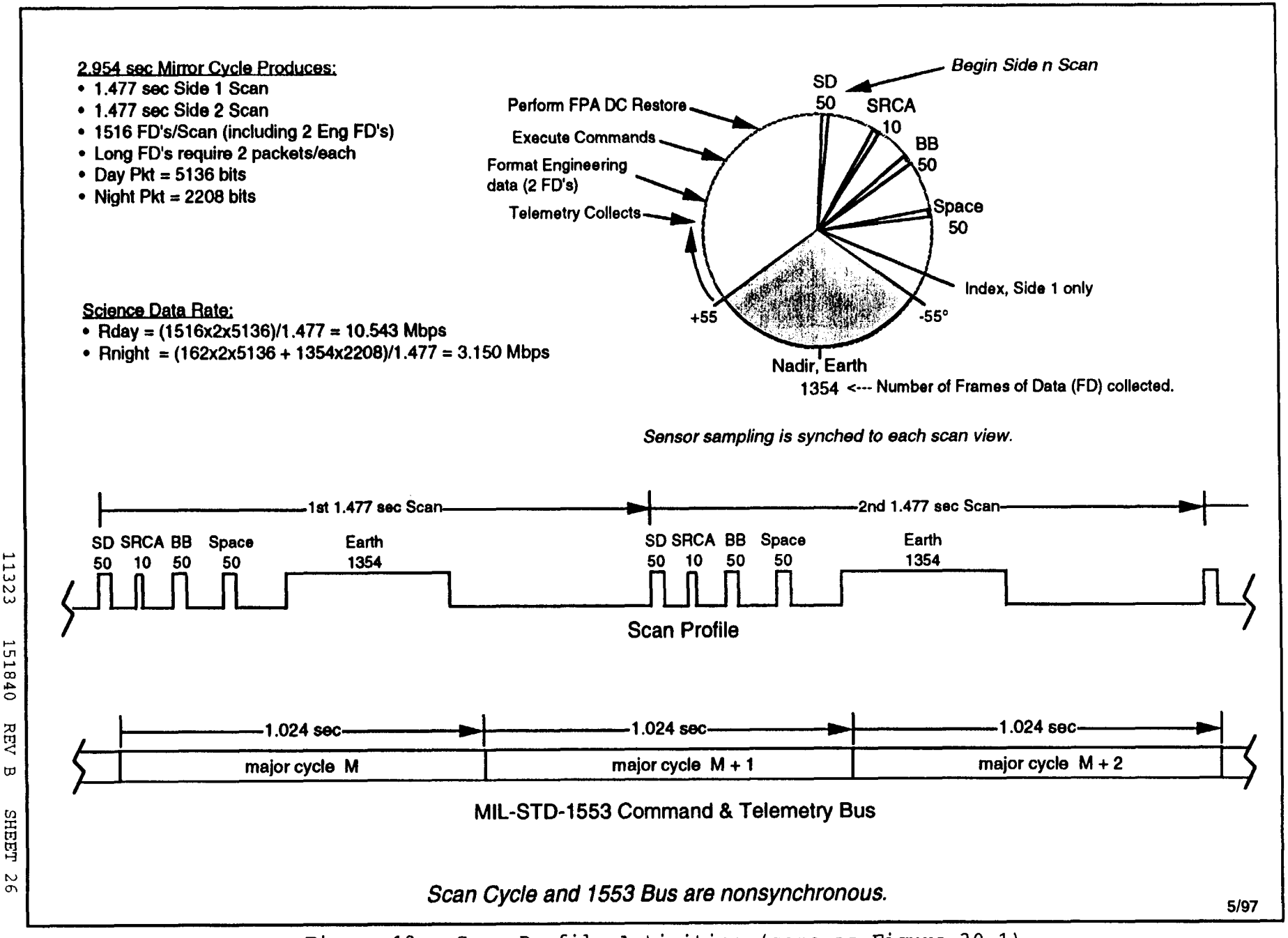


Figure 13. Scan Profile Activities (same as Figure 30-1)

6. COMMAND & TELEMETRY BUS OVERVIEW

MODIS receives commands from the spacecraft (S/C) by direct point-to-point paths and over the MIL-STD-1553B command and telemetry bus (1553 bus). Both interfaces are implemented as specified in Sections 5, 6 & 7 of the 423-03-02 General Instrument Interface Specification (GIIS), EOS-AM Project. A brief overview of the 1553 bus is presented here. MODIS operational details are presented in Appendix A for commands and Appendix B for telemetry.

6.1 MIL-STD-1553 bus fundamentals. The 1553 bus is a serial bus with bidirectional data flow between major system hardware elements, with one element designated as the Bus Controller (BC) and the other elements as Remote Terminals (RT). Control and transfer of data is accomplished by the use of 3 types of 20-bit words in 10 different message formats. Five of the 1553 formats are not used by the EOS project, which relate to use in a broadcast mode and RT-RT message transfers. The five information transfer formats used by EOS, which require an RT status word for receipt of an error-free message from the BC, are shown in Figure 14. The 20-bit word structure for the command word, the status word and the data word are shown in Figure 15. All have a 3-bit sync pattern and a parity bit, based on odd parity of the 16 bits of data and parity bit. Data transfer from the BC to RTs is accomplished with the first message format in Figure 14, and can contain 1 to 16 32-bit data words. Data transfer from the RTs to the BC is accomplished with the second message format in Figure 14. The remaining message formats relate to bus control modes (immediately below).

The 1553 architecture utilizes mode codes for communications management of the bus. Table 6 lists the mode codes used by the EOS-AM spacecraft (GIIS Table 6-1). See MIL-STD-1553B or MIL-HDBK-1553 for more details.

TABLE 6. MIL-STD-1553B MODE CODE UTILIZATION

Transmit/ Receive Bit	Mode Code	Function	Related Data Word
1	00010	Transmit status word	No
~~1~~	~~00001~~	~~Synchronize (see note 1)~~	~~No~~
1	00011	Initiate self-test	No
1	00100	Transmitter shutdown	No
1	00101	Override transmitter shutdown	No
1	00110	Inhibit terminal flag bit	No
1	01000	Reset remote terminal	No
~~1~~	~~10000~~	~~Transmit vector word (see note 1)~~	~~Yes~~
0	10001	Synchronize (see note 2)	Yes
1	10010	Transmit last command	Yes
1	10011	Transmit BIT word	Yes

Notes:
1/ ~~Used on the Low Rate Science Data Bus only~~, not applicable to MODIS.
2/ Used on the Command and Telemetry Bus only.

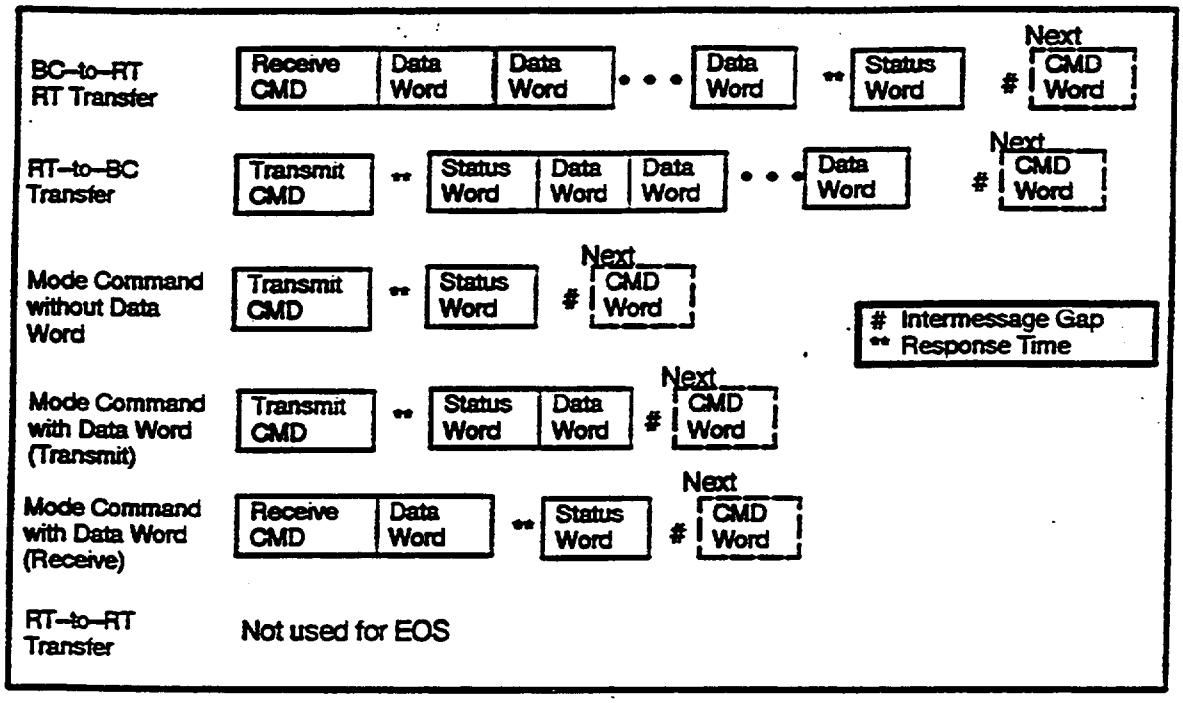


Figure 14. 1553B Bus Information Transfer Formats

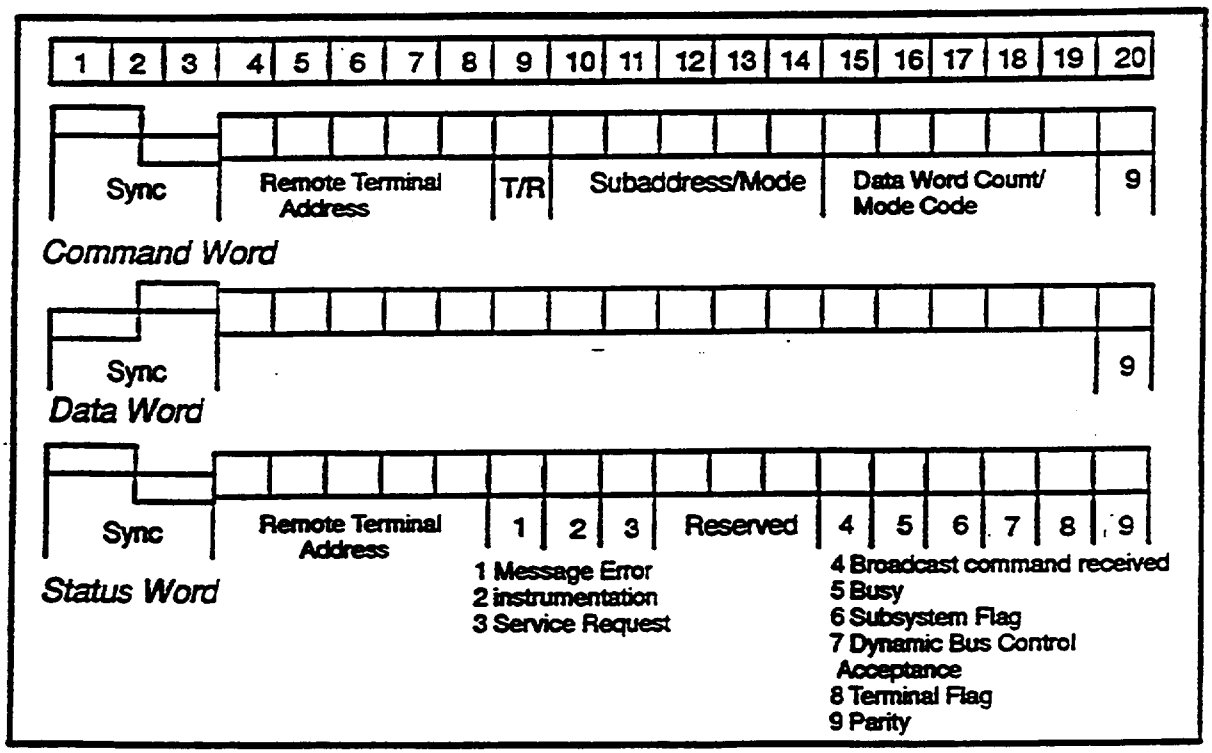


Figure 15. 1553B Bus Word Formats

6.2 S/C 1553 bus characteristics. The S/C 1553 bus controller (BC), is located within the Command & Telemetry Interface Unit (RTIU) of the Command and Data Handling (C&DH) subsystem. All instruments and other S/C subsystems are configured as remote terminals. Instrument commands are transported within a 1553 message by the combination of a 1553 command and data words with the general format indicated in Table 7. The specific formats, beginning with data word 1, used to transfer MODIS commands over the 1553 bus are described later in Appendix A. The Remote Terminal ID for MODIS is 12 (B#01100).

One particular 1553 bus use by the S/C, is to control its Bus Data Units (BDU), which provide the small set of point-to-point command and telemetry functions individually allocated to the instruments. Also, the S/C uses a separate 1553 bus as a low rate science link from some instruments (not applicable to MODIS).

TABLE 7. GENERAL MIL-STD-1553 GROUND MESSAGE FORMAT

MSB 0 — 4	5	6 — 10	11 — LSB 15
Remote Terminal ID	0	Subaddress	N=Word count (used by RT)
Data 1			
• • • •			
Data 32			

6.3 Bus message types. Table 8 lists the types of messages that can be transferred on the command and telemetry bus with their particular 1553B subaddresses.

TABLE 8. MIL-STD-1553B MESSAGE SUBADDRESSES

Subaddress	Message name	T/R bit 1/
1	Instrument Command	0
2	Load Data	0
2	Dump Data	1
4	Ancillary Data	0
5	IMOK	0
6	Time Code Data	0
7	Safe Mode Command	0
9	Loop Back	1 or 0
17	Normal Housekeeping telemetry	1
18	Critical Housekeeping telemetry	1
0 or 31	Mode Code	1 or 0

1/ 1 = Transmit, 0 = Receive.

6.4 EOS-AM 1553 bus frame and timing. A bus frame and timing structure has been defined by the EOS-AM project to implement transfer of data across the 1553 bus. It is based on minor cycles, major cycles and master cycles that have the following relation. A minor cycle will have a period of 8 ms ± 100 µs, a major cycle (1.024 seconds) will consist of 128 minor cycles, and a master cycle (65.536 seconds) will consist of 64 major cycles. Figure 16 provides an illustration of this structure with the projected reserve goal. As described below, a S/C bus utilization table has been established to control the flow of bidirectional data between the S/C BC and all RTs (S/C and instruments).

6.5 EOS-AM 1553 bus utilization table. Figure 17 illustrates the general schedule for major cycle task transfers on the 1553 bus. Five "Types" of activities have be designated to occur within each minor cycle. The Minor Cycle Tasks sub-table in Figure 17 further define what particular minor cycle tasks are to occur within the Type group, and are related by their list number. In the sub-table, Minor Cycle Tasks 1, 4, 6, 7, and 8 are required to be transferred every major cycle. Task 1 is transferred 4X and the others once per major cycle. Operational activity will determine if the other tasks in the sub-table are transferred. If they are, they will be per the general schedule shown in Figure 17.

Specific instrument and S/C subsystem transfer assignments for the general schedule in Figure 17 are contained in the S/C Bus Utilization Table (BUT). BUT details are described in design note EOS-DN-C&DH-048 Command and Telemetry Bus Utilization Table, and applicable parts are documented in each instrument Command and Telemetry ICD (20008847 for MODIS). BUT detail is not illustrated here.

Some of the specific 1553 bus assignments that pertain to MODIS are contained in Table 9 (Subaddress data is from Table 8).

TABLE 9. MODIS 1553 BUS MINOR CYCLE ASSIGNMENTS

Subaddress	Message	Minor Cycle
-	Sync-with-data-word	12,44,76,108
4	Ancillary Data	79
5	IMOK (SCC is Ok)	44
6	Time Code Data	92
17	Normal Housekeeping telemetry	72
18	Critical Housekeeping telemetry	12

1/ The 1553 bus MODIS RT address is 012.

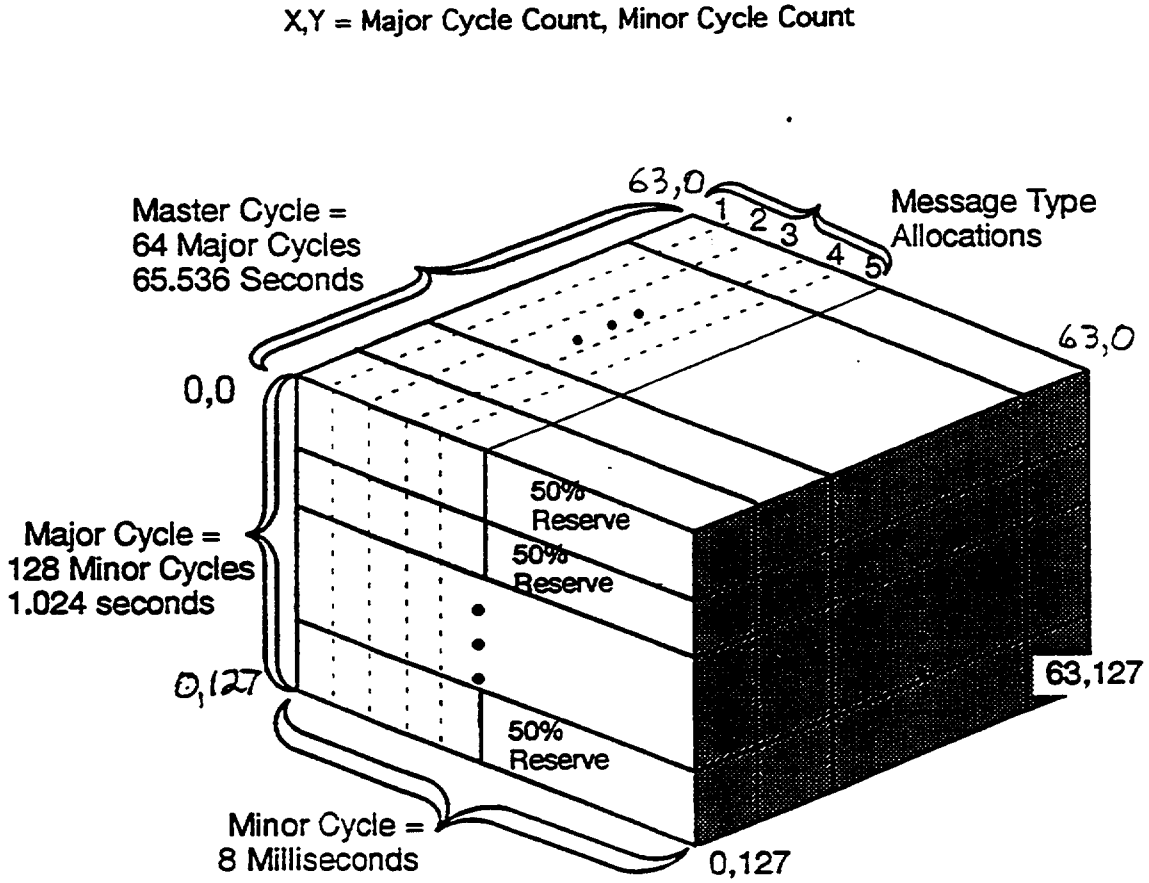


Figure 16. Spacecraft Bus Command and Telemetry Frame and Timing

Implies order within a minor cycle >

Minor Cycle Number	Type #1	Type #2		Type #3		Type #4		type #5	Reserve Bus Utilization
0	1	2	2	9	—	4	5		>50%
1	1	2	2	3	3	4	4		
2	1	2	2	3	3	4	4		
3	1	2	2	3	3	4	4		
4	1	2	2	9	—	4	4		
5	1	2	2	3	3	4	4		
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	
32	1	2	2	9	—	4	4	6	
33	1	2	2	3	3	4	4	6	
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	
64	1	2	2	9	—	4	4	7	
65	1	2	2	3	3	4	4	7	
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	
96	1	2	2	9	—	4	4	8	
97	1	2	2	3	3	4	4	8	
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	10	
126	1	2	2	3	3	4	4		
127	1	2	2	3	3	4	4		

1 Major Cycle

***NOTE: Types are not meant to show timing, only relative order!**

minor cycle = 8 msec,
major cycle =128 minor cycles
master cycle = 64 major cycles

1. Synchronize with Data Word. One issued per minor cycle to an individual remote terminal. Each remote terminal receives 4 per major cycle.
2. BDU sample schedule table.
3. All onboard issued commands (stored commands, FDIR, closed loop). In 4 minor cycles. 1–3 can contain up to 2 onboard commands while the 4th minor cycle can contain only 1 ground command
4. Gathering request for H&S telemetry, H/K telemetry and SCC closed loop data.
5. Diagnostic – Memory Dump. Minimum interval between gathers is 6 minor cycles. Note: A C&T bus loop back will use this task type upon command to the CTIU as long as there is no on–going memory dump or C&T mode code commanding.
6. IMOK message.
7. Ancillary Data.
8. Time Code.
9. Ground Commanding: 1 command every 4 minor cycles
10. Active CTIU Telemetry—This is telemetry from active CTIU which is incorporated in the Standby CTIU telemetry by the Standby CTIU.

Figure 17. Spacecraft 1553 Bus Major Cycle Task Schedule

7. COMMAND & TELEMETRY SUBSYSTEM ABBREVIATIONS

To facilitate the structure of mnemonic names in command and telemetry lists (which have 16 character limitations by the GIIS), a set of two-character subsystem abbreviations have been defined for MODIS subsystems. The brevity of these abbreviations coupled with the fact that many subsystems have the same leading and trailing characters, sometimes result in abbreviations that are not as intuitive as if more characters were available. These two-character abbreviations are generally shorter than other acronyms and abbreviations seen in other documents. Here, subsystem elements extend to low hardware level items, such as, circuit card assemblies. In general, the command and telemetry tabular lists within this document have a first sort by these two-character subsystem abbreviations.

The two-character subsystem abbreviations are listed in Table 10, and are related to the MODIS hardware in Figure 11 with their two-character code. This table is limited to subsystem abbreviations. See Table 11 for others.

TABLE 10. MODIS SUBSYSTEM ABBREVIATIONS

AO	Aft Optics (all major optical elements & VIS/NIR FPAs
BB	Blackbody
CE	Calibrator Electronics (controls all cal devices)
CP	Command & telemetry Processor
DR	Doors (Space View, Nadir Aperture, Solar Diffuser)
FI	FDDI Formatter & Output Driver
FO	FIFO Memory
FR	Formatter (Format Controller & Engine)
MC	Mechanism Controller
ME	Main Electronics Module (MEM)
MF	Mainframe
PC	PC FPA processing by Forward View Analog Module (FAM)
PS	Power Supply
PV	PV FPA processing by Space View Analog Module (SAM)
RC	Radiative Cooler (includes CFPAs)
SA	Scan Mirror Assembly (with motor & encoder)
SC	Spacecraft (S/C)
SD	Solar Diffuser
SE	Scan Electronics (scan motor driver/encoder processing)
SM	SD Stability Monitor (SDSM)
SR	Spectroradiometric Assy (SRCA)
SS	Sunshade
TC	Temperature Controller
TE	Telescope
TG	Timing Generator
TM	Telemetry Circuits

NOTE

Some end subsystems are of primary interest to the user versus its controlling subsystem. Thus, some parameters are designated to the subsystem of interest. For example, doors (DR) are controlled by the mechanism controller (MC). Door commands are given a DR code versus a MC code because of interest in doors. Another example, radiative cooler (RC) temperatures and outgas heater status states are of more interest than their temperature controller (TC). PV for the SAM and PC for the FAM, are used because of primary interest in the functional support of the PV and PC FPAs.

8. MODIS TELEMETRY, ENGINEERING & SCIENCE DATA

Any data that comes to the ground can be generically classified as "telemetry data". However, for MODIS a clear distinction is made between telemetry, engineering and science data.

Science data is simply all the FPA detector signals that are sent as CCSDS packets over the FDDI high rate data link. See Appendix C for details.

Engineering data provides information related to science operations, and is also sent as packets over the high rate data link. Engineering data can vary from FPA operating voltages, analog offset values, various calibrator parameters and S/C ancillary data. See Appendix C for details.

Telemetry data provides information on the general control, health and safety of MODIS, and is sent over two different paths to the S/C. A small number of housekeeping telemetry items are handled as direct point-to-point items processed by the S/C. A much larger number of telemetry items are processed over the 1553 command and telemetry bus. See Appendix B for details.

Critical housekeeping telemetry is defined as the small S/C point-to-point subset. It will be multiplexed with other instruments and S/C critical telemetry and sent over a low rate down link if contingency operations occur that won't support full telemetry operations.

A small amount of data appears in both telemetry and engineering data in order to provide control information needed for both housekeeping tasks and science calibrator configurations.

9. GENERAL ABBREVIATIONS & ACRONYMS

Table 11 defines abbreviations and acronyms used in this document and includes already listed Table 10 items.

TABLE 11. ABBREVIATIONS & ACRONYMS

AEM	Auxiliary Electronics Module
AO (2 ch)	Aft Optics (all major optical elements)
APID	Application Process ID
BB (2 ch)	Blackbody
BDU	Bus Data Unit
Cal	Calibration
CCSDS	Consultive Committee for Space Data Systems (standards by committee of international agencies)
CE (2 ch)	Calibrator Electronics
CFPA	Cold Focal Plane Array, or Assembly (SWIR, MWIR, LWIR)
CLAM	Cooler Located Analog Module (preamp part of FAM)
CP (2 ch)	Command and Telemetry Processor
CTP	Command and Telemetry Processor
DAC	Digital to Analog Converter
EOS	Earth Observing System
FAM	Forward Viewing Analog Electronics Module
FDDI	Fiber Distributed Data Interface
FI (2 ch)	FDDI Formatter & Output Driver
FIFO	First In First Out Memory
FO (2 ch)	FIFO Memory
FPA	Focal Plane Array, Assembly (clear by context)
FR (2 ch)	Formatter (Format Controller & Engine)
GIIS	General Instrument Interface Specification (GSFC)
GSFC	Goddard Spaceflight Center (NASA EOS Program Office)
H/K	Housekeeping
IFOV	Instantaneous Field of View
IMOK	Spacecraft computer 1.024 sec Ok health signal
ISR	Interrupt Service Routine
ITWK	I-TWEAK FPA current bias control
LWIR	Long wave infrared
MC (2 ch)	Mechanism Controller
ME (2 ch)	Main Electronics Module (MEM)
MEM	Main Electronics Module
MF (2 ch)	Mainframe (with KM mounts, doors, baffles, shrouds)
MUX	Multiplexer (digital or analog)
MWIR	Medium Wave infrared
NIR	Near infrared
PC (2 ch)	Photo Conductive (detector type)

CONTINUED

TABLE 11. ABBREVIATIONS & ACRONYMS (*CONTINUED*)

PIX	Pixel
PS (2 ch)	Power Supply
PV (2 ch)	Photo Voltaic (detector type)
RC (2 ch)	Radiative Cooler
RT	MIL-STD-1553B Remote Terminal on S/C
SA (2 ch)	Scan Mirror Assembly (includes encoder)
SAM	Space Viewing Analog Electronics Module
SBC	Single Board Computer (in CP and FR)
SBR	Spectral Band registration
SBRC	Santa Barbara Research Center (MODIS provider)
SC, S/C	Spacecraft
SD (2 ch)	Solar Diffuser
SDSM	Solar Diffuser Stability Monitor
SE (2 ch)	Scan Mirror Electronics & Encoder
SIPD,SiPd	Silicon Photodiode
SIS	Spherical Inegrating Source
SM (2 ch)	Solar Diffuser Stability Monitor
SNR	Signal to Noise ratio
SR (2 ch)	Spectroradiometric Assy (SRCA)
SRCA	Spectroradiometric Calibration Assembly
SWIR	Short wave infrared
TC (2 ch)	Temperature Controller
TG (2 ch)	Timing Generator
TM (2 ch)	Telemetry Circuits
VIS	Visible

1/ (2 ch) = 2 character MODIS subsystem abbreviation repeat from Table 9.

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10.1 SCOPE

This Appendix describes MODIS command implementation, command formats/structures, command lists, and command constraints. Appendix D describes command and telemetry relations.

As noted in Section 1.2, the multiple use of this document for development and test, ICD data definition and operations planning, results in the inclusion of material that is not of interest to all users. In general, the left half of the command list in Table 10-25 will be of interest to end users, while the right half will also be of interest to development designers, programmers, GSE, integration and test personnel.

Command constraints and restricted commands are addressed in 10.9.

The MODIS two-character subsystem abbreviations defined in Figure 11 and Table 10 are used throughout this Appendix along with full names.

10.2 COMMAND PHILOSOPHY

The general command and control philosophy for instruments on the EOS-AM spacecraft (S/C) is that they will generally be operated in an autonomous, non-real-time manner. Thus, most major and minor activity that the MODIS must perform to fulfill its intended mission objective must be controlled by stored high level commands and macro command sequences. This document defines MODIS commands. Command sequences are defined in CDRL 405 MODIS Command Operating Procedures.

10.3 COMMAND IMPLEMENTATION

As illustrated in Figure 10-1, MODIS is controlled by a combination of direct point-to-point and MIL-STD-1553 bus commands from the S/C. The MODIS Telemetry and Command Processor (CP) receives and decodes the 1553 bus commands, and issues internal controls or commands in response to the external command. The CP is the central control processor for MODIS, that controls and monitors all MODIS functions/subsystems directly (point-to-point) and indirectly (serial links).

10.4 S/C POINT-TO-POINT COMMANDS

All S/C point-to-point commands are implemented as +28V relay pulses per the GIIS. As shown in Figure 10-1 they are directed to three MODIS subsystems: the power supplies (PS), the CP's and the mechanism controller (MC). The S/C relay commands appear in the MODIS command list in Table 10-25A with shading on their subsystem items to more quickly spot S/C items. They are also designated as RS in the "Cmd Type" column. There is only one set of redundant S/C point-to-point command: TURN_OFF_PSA and TURN_OFF_PSB (either turns off both PS1 and PS2).

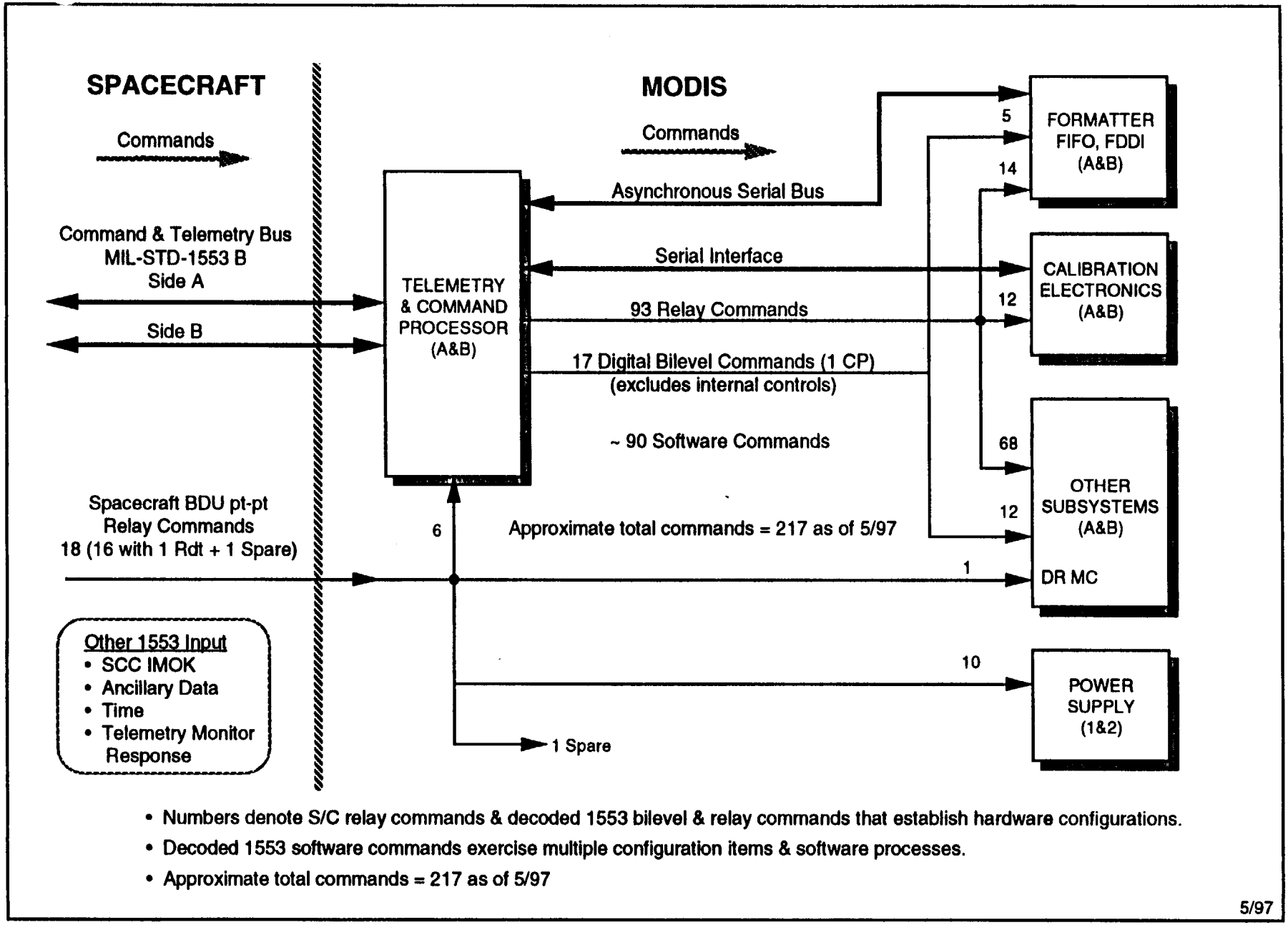

Figure 10-1. MODIS Command Flow Diagram

10.5 S/C MIL-STD-1553B BUS COMMANDS

The MIL-STD-1553B command and telemetry bus was described in Section 6, and is implemented as a redundant interface per the GIIS. Decoded bus commands result in various forms of internal controls to generate relay pulses, or send digital bilevel controls, or to send digital values, or to set logic levels, or to change software parameters. Some of these controls are executed by the address and data bus in Figure 10-2, a block diagram of the Telemetry and Command Processor. Other controls are implemented by the serial links to the formatter and calibration control electronics at the top of the figure.

10.5.1 MODIS relay controls. MODIS has 93 relay control outputs for each CP as shown in the middle of Figure 10-1. Some relay controls are common to both side A and side B of a given subsystem. For instance, most subsystems have a common OFF command. Most of the common OFF commands and some commands of the A_ON, B_OFF style are actually implemented by software control of separate relay drivers because of the number of relays and drive limits or for redundancy reasons. This implementation is transparent to the end user. Summary count numbers used in figures or at the bottom of lists reflect numbers that the external end user would relate to. In the command list of Table 10-25A, relay commands are designated in the "Cmd Type" column as R if a single driver is used, or as RD if dual drivers are used. Note, RD relay commands are implemented by a single address/data location in the CP, and not by coupling commands in a special 1553 bus structure.

All subsystems have relay controls for power. Most major hardware functions of the subsystems are also controlled by relays. All subsystems have an A_ON,B_OFF; B_ON,A_OFF and BOTH_OFF command structure. In addition, the scan mirror drive electronics (SA) and the FAM (PC) have a BOTH_ON command. The power supplies, controlled directly by the S/C, also have a BOTH_ON capability. Power commanding is presented as A_ON, B_OFF in order to present a consistent operations interface to the user. The hardware may have separate drivers to drive A_ON, B_OFF. These separate driver commands are transparent to the end user. They are designated as relay internal controls (RIC), and appear in Table 10-26 for hardware/software development use.

10.5.2 MODIS digital controls. MODIS has 18 external user digital command controls (bilevel and redundant) for each CP as shown in the middle of Figure 10-1. Some digital command controls are common to both side A and side B of a given subsystem. Or, stated another way, the active subsystem responds to the common command. This results in a lower command count to the end user. External digital commands in command list Table 10-25A are designated in the "Cmd Type" column by SWD. Digital commands are controlled by one bit of a 16-bit word. Care must be exercised to maintain the state integrity of the other 15 bits when changing the state of the item of interest.

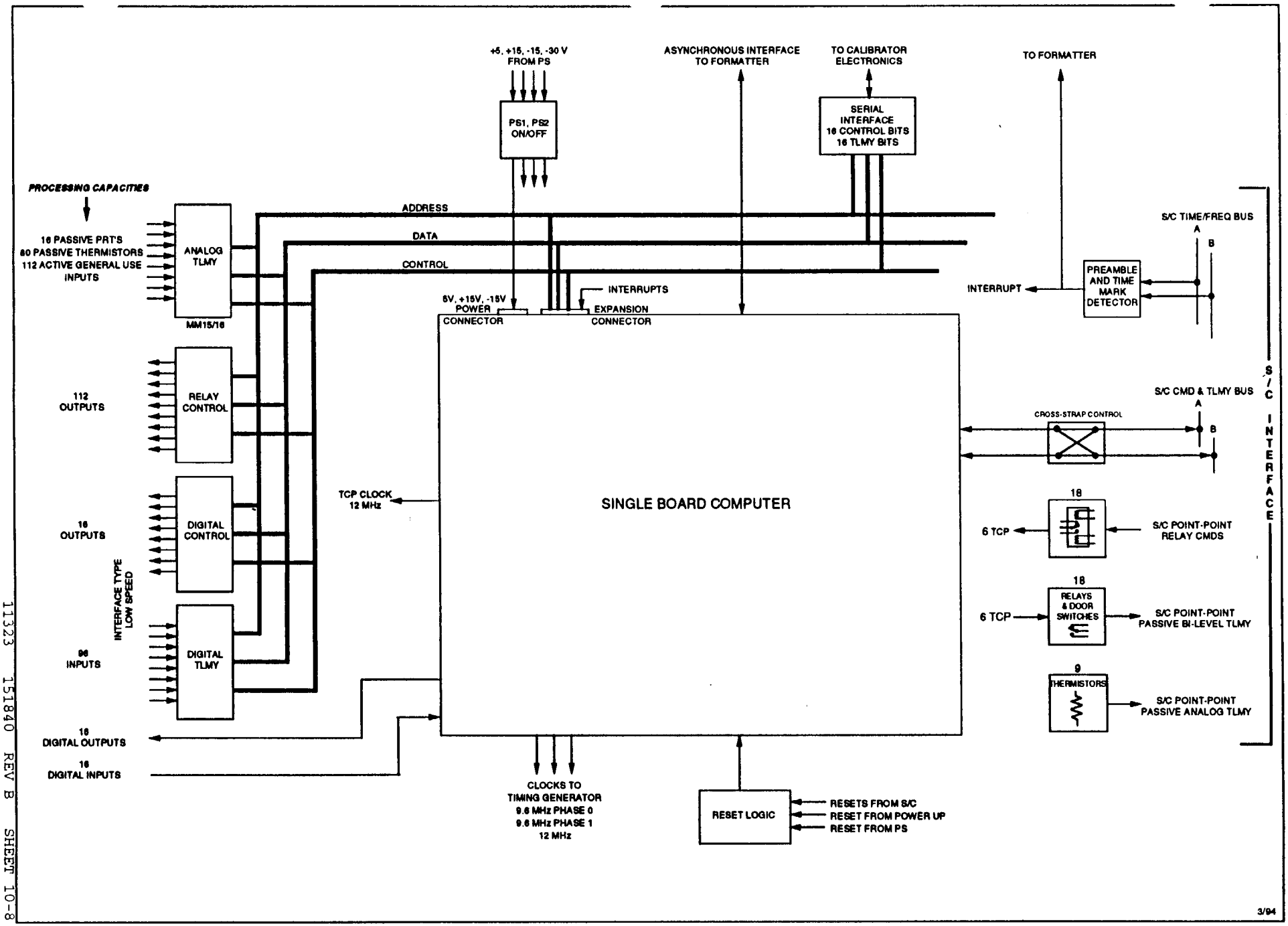

Figure 10-2. MODIS Command & Telemetry Processor Block Diagram

In addition to external user commands, digital internal controls are used to control a variety of functions transparent to the end user. For example, phased stepping patterns to door and calibration device motors, or reset and stepping controls to the SAM and FAM analog telemetry muxes, etc. Digital internal controls (DIC) appear in Table 10-26 for hardware/software development use.

10.5.3 Formatter interface. Each CP has an asynchronous bi-directional serial interface to the Formatter (FR) to control and monitor its functions. The CP and FR are used in a loosely coupled architecture to allow separation of major tasks. As indicated in Section 5, all internal MODIS functions are synchronized to the 1.477 seconds scan cycle, which is timed by the formatter from scan mirror index and encoder pulses.

10.5.4 Calibrator electronics interface. Each CP has a 16-bit serial interface with the calibrator electronics to configure, control and monitor its functions. The calibrator electronics are in the main electronics module, and communicate directly with each external calibration device: Solar Diffuser Stability Monitor (SM), SRCA (SR) and Blackbody (BB). ON/OFF power to the three calibrators is controlled directly by the CP. However, all other command and bilevel status telemetry functions must pass over the CP-CE serial link.

10.5.5 Fail safe control. Fail safe control consists of a series of interlocks used during the activation of a door mechanism fail safe device. It must be initiated by a direct S/C relay command, and be followed by at least two sequential relay commands. This completes the path for electrical current to pass through the fail safe device.

10.5.6 Command execution time. MODIS executes commands as they are received from the S/C. That is, it does not time-tag and store them for future execution. Thus, if any commands or command sequences need to be executed at particular times within an orbit as a part of normal scheduled operations (such as mode changes), the S/C must issue these to MODIS at the appropriate times.

10.5.7 Command receipt verification. MODIS verifies receipt of all commands. This consists of decoding and error checking commands received over the command and telemetry bus. If a bus error is detected, an event will be logged in the event log.

10.5.8 Command execution verification. Execution verification of commands is normally performed by ground processing of the related telemetry points. MODIS only performs on-board execution verification for high level commands as defined later. These require knowledge that particular steps of multiple action command sequences have been completed before proceeding with the next command.

10.5.9 Redundancy. Almost all MODIS subsystems are fully redundant. Redundant commands and subsystems are generally defined in terms of A and B, or, Side A and Side B and not in terms of primary and secondary, or one and two (PS1 and PS2 are an exception).

10.6 CONTROL PROCESSOR SOFTWARE

Ada is the operational language for the 1750A microprocessor. The MODIS CP software operates under the control of a Small System Executive (SSE), which is characterized by fixed, hard priorities and cooperative multitasking. The processes running underneath the executive are activated by interrupts or by other processes. Scheduling is invoked by the processes themselves. Figure 10-3 indicates the CP Software Architecture. For more details see SBRC 152929 MODIS Flight Software System Architecture Document (CDRL F306D) and SBRC 152930 MODIS Flight Software Detailed Design (CDRL F306E). The software shall support the primary CP functions summarized below.

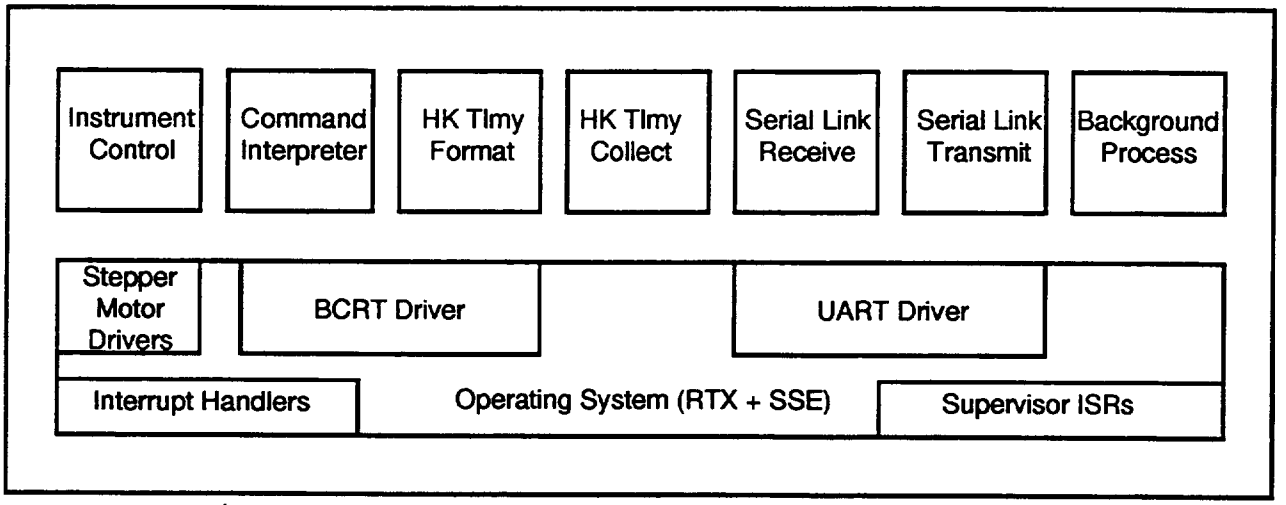

Figure 10-3. Control Processor Software Architecture

10.6.1 1553B interface. CP software shall support the interface to the 1553 bus to accept all messages addressed to valid subaddresses as listed in Table 8. This includes commands, S/C IMOK, S/C Ancillary Data, S/C Time and S/C Telemetry Monitor (TMON) Response. Also, housekeeping telemetry shall be provided periodically to the S/C on request.

10.6.2 Process commands and data. The CP validates and executes commands, synchronizes S/C time with the Time Mark and Frequency Bus and executes memory loads and dumps. Table 10-24 lists the various control tables that may be uploaded or dumped over the bus. Some tables are dumped as science engineering data over the high rate link during normal science operations as noted in Column 2.

10.6.3 Control and monitor. The CP controls and monitors the MODIS subsystems under software control. This includes monitoring S/C IMOK. Also, internal telemetry is monitored during execution of high level commands. The control and monitor function runs synchronously with the 1.477 second scan mirror cycle. The CP generates a pseudo scan cycle for timing, whenever the scan mirror is not running.

10.6.4 Sample and format telemetry. The CP samples housekeeping telemetry and formats it for transmission in synchronization with the 1.024 second major cycle of the 1553 Command and Telemetry Bus.

10.6.5 Interface with format processor. The software also supports the CP interface with the Format Processor to send it S/C time and commands, and also S/C ancillary and MODIS housekeeping data for inclusion in science engineering data. And, it receives scan mirror position information.

10.7 BUS COMMAND TYPES

MODIS external control by the 1553 bus is implemented by four types of bus commands that vary in their degree of sophistication and utilization. These commands are defined below.

10.7.1 Low level commands. Low level commands are unconditional commands that cause the Control Processor (CP) to generate relay pulses, send digital bilevel commands or change software parameters. Examples are power on, port selection, etc.

10.7.2 High level commands. High level commands require knowledge of the current state of the system. The MODIS CP must read the particular instrument status or telemetry information to carry out the command. Examples are operating any of the doors or calibrator mechanisms, or performing a SDSM calibration sequence.

10.7.3 Macro commands. Macro commands consist of a sequence of low and/or high level commands, which are stored in a CP lookup table and executed in order. Macro commands can not be called by another macro command.

10.7.4 Memory load/dump commands. Memory load/dump commands allow memory from either processor to be uploaded or dumped in blocks of up to 32 words. The addresses may be specified as absolute or relative. For memory dumps, the output channel can also be specified as the command and telemetry bus or the high data rate link

10.8 BUS COMMAND STRUCTURES

End users may not be interested in the details of bus command structures. However, many command parameter selections are addressed in the definition of bus structures, which provides insight to the subsystem operations. Column 7 in the Table 10-25A Command Lists will point to the particular operations code tables for the details of interest if the reader does not want to digest all the details at this time.

The general MIL-STD-1553B message format structure for EOS instrument commands was defined in Table 6 with 1553 subaddress listed in Table 8. The general form of the data fields structured for specific MODIS use are defined by Table 10-1. The MSB is transmitted first, which coincides with MIL-STD-1750A usage.

TABLE 10-1. MODIS GENERAL BUS COMMAND STRUCTURE

MSB 0	4	5	7	8	LSB 15
Operation Code		Word Count		Parameters	
Parameters (optional)					
Parameters (optional)					
• • • •					

Table 10-1 is the basis for defining particular MODIS bus command structures to implement a variety of the type commands defined in 10.7. The Operation Code field (bits 0-4) tells the CP what type or subtype of command is to be processed.

The Word Count field (bits 5-7) indicates the number of words following the first word (i.e. in a single word command, this field is set to zero).

The Parameters field (bits 8-15) identifies the particular parameter function, and if applicable, the value to set it to.

The use of this general bus command structure to process MODIS commands is described as follows.

If invalid values are received for any fields of the following command definitions, no command is executed, and a CP event is generated. If the invalid item is part of a macro command sequence, then the entire macro is aborted, and a CP event is posted.

10.8.1 Bus Relay command. Table 10-2 indicates the structure for MODIS relay pulse commands. Relay commands are low level commands.

TABLE 10-2. BUS RELAY COMMAND STRUCTURE

MSB 0	4	5	7	8	LSB 15
00011		000		relay ID	

The CP will generate a specific relay pulse when its particular relay address/data location is entered into the command structure.

Certain relays initiate nonreversible commands. These commands are normally inhibited, i.e. the flight software will discard them unless they are enabled. The general procedure to initiate failsafe actions is addressed in 10.9.

Certain relay commands are implemented by dual drivers either to extend drive capability or for reliability reasons. When a ground command is received to execute one of these commands, the single software ID shall drive both the primary and redundant systems. Relays in this category are so indicated in Table 10-25A by RD.

When any of the following commands are sent, at least three seconds should be allowed to pass before sending any of the other commands in this list. Commands not on this list may be sent during the 3 second period:

TURN ON MOD CEA (Relay commmand 4)

TURN ON MOD CEB (Relay commmand 5)

TURN ON MOD SRA (Relay commmand 78)

TURN ON MOD SRB (Relay commmand 79)

SET MOD SR_SIS_FB to RADIANCE/CURRENT (Parameter Command 72)

SET MOD SR_LOV_SHDN to ENABLE/DISABLE (Parameter Command 73)

SET MOD SR_LAMPS to OFF/W1/W10/W20/W30 (Parameter Command 75)

10.8.2 Bus Set Parameter command. Table 10-3 indicates the structure for bus set parameter type commands.

TABLE 10-3. BUS SET PARAMETER COMMAND STRUCTURE

MSB 0 4	5 7	8 LSB 15
01100	001	parameter #
value		

The MODIS CP contains a "configuration parameter table" that controls software algorithms or operational modes. This command allows any single 16 bit entry in that table to be modified. Table 10-22 lists the parameters stored in that table.

The same command list constraints at the end of 10.8.1 apply to 10.8.2.

10.8.3 Bus Actuate Door command. Table 10-4 indicates the structure for the high level Actuate Door command.

TABLE 10-4. BUS ACTUATE DOOR COMMAND STRUCTURE

MSB 0 4	5 7	8	9 10 14	LSB 15
11111	000	DS	00000	DP

This command causes the stepper motor for one of the three doors to step to one of several predefined positions. Predefined positions are defined in terms of absolute step count, but are overridden by telemetry readings if available. Telemetry readings are available for all predefined positions of all doors, except the OUTGAS position of the Space View Door. Motor features are provided below Table 10-6. Bits 8-9 are the Door Select field, which is defined as follows:

00: INVALID.

01: Nadir Aperture Door (NAD).

10: Space View Door (SVD).

11: Solar Diffuser Door (SDD).

Bits 14-15 are the Door Position field, defined as follows

00: Closed (NAD;SVD;SDD&SCREEN).

01: Open (NAD; SVD; SDD&SCREEN).

10: Screen Closed (SDD Open).

11: Outgas (SVD open approximately 5°).

Some door positions are legal for all doors. Other positions are legal only for certain doors, as described in Table 10-5. For the Solar Diffuser Door, the OPEN position indicates that both the Solar Diffuser Door and the Solar Diffuser Screen are open.

TABLE 10-5. BUS DOOR POSITION DEFINITIONS

Door Position	Nadir Aperture Door	Space View Door	Solar Diffuser Door
CLOSED	LEGAL	LEGAL	LEGAL
OPEN	LEGAL	LEGAL	LEGAL
SCREEN CLOSED	ILLEGAL	ILLEGAL	LEGAL
OUTGAS	ILLEGAL	LEGAL	ILLEGAL

10.8.4 Bus Step Motor Relative command. Table 10-6 indicates the structure for the high level Step Motor Relative command.

TABLE 10-6. BUS STEP MOTOR RELATIVE COMMAND STRUCTURE

MSB 0	4	5	7	8	9	13	LSB 15
10111		001		D	0000		MTR
Step Count							

This command causes the selected stepper motor to be stepped in the direction specified by the D bit, 0 = decreasing position, 1 = increasing position (other direction terms may also be used), by the number of steps in the second word of the command. The 3-bit MTR parameter selects the motor as follows:

000: INVALID.

001: Nadir Aperture Door Motor.

010: Space View Door Motor.

011: Solar Diffuser Door Motor.

100: SDSM Motor.

Door motors do not have encoders.

Doors have position switches.

OBC motors have single position encoder.

101: SRCA Filter Wheel Motor. *OBC encoders do not control motors.*

110: SRCA Entrance/Exit Slit Motor. *OBC motors have no other telemetry.*

111: SRCA Grating/Mirror Motor. - - - - - - - - - - - - - - - - -

The step count variable is limited to the maximum number of stepper motor positions for the specified motor. If the provided step count is greater than the number of step positions, the step count is reduced to the maximum, and a warning event is issued. For motors with hard stops, if the commanded number of steps would drive the motor into the hard stops, the step count is reduced further so that the motor will step to the hard stop without being driven into it. If the motor can rotate freely throughout 360 degrees, the motor is allowed to step through the zero position, and its motor position is wrapped around into the proper range. Electrical phase drive characteristics are defined in the 151785 MEM Spec. Note travel direction conventions vary.

NAD Door/Motor Features: (Closed/Open is in absolute step count)

1) Closed = Home = Step 0; Open direction = increased step count = Mtr CW.

2)* Open = 90° ±1° = Step 3700/3741 nom/max [3750]; repeat = ±0.25°.

3) Step size = 90°/3700 = 0.0243°/step.

4) Step rate = 130 steps/second with pulse width = 7.7 mS.
For sequential pulses, ending pulse width = 60 mS.

SVD Door/Motor Features: (Closed/Open is in absolute step count)

1) Closed = Home = Step 0; Open direction = increased step count = Mtr CCW.

2)* Open = 93.5° ±0.5° = Step 3844/3864 nom/max [4060]; repeat = ±0.25°.

3)* Outgas open = 5° ±1° = Step 206 nom [350].

4) Step size = 90°/3700 = 0.0243°/step.

5) Step rate = 130 steps/second with pulse width = 7.7 mS.
For sequential pulses, ending pulse width = 60 mS.

SDD Door/Motor Features: (particular positionis in absolute step count)

1) Closed = Home = Step 0; Open direction = increased step count = Mtr CCW

2)* Door Open = 95° ±0.5° = Step 993/998nom/max [1027]; repeat=±0.25°.

3)* Screen Open = 95° ±0.5° = Step 1986/1991 [2145].

4) Step size = 90°/940.6 = 0.0957°/step.

5) Step rate = 40 steps/second with pulse width = 25 mS.
For sequential pulses, ending pulse width = 60 mS.

SDSM Mirror/Motor Features: (Closed/Open is in absolute step count)

1) DCR = Home = Step 29; Sun direction = increased step count = Mtr CCW.
Although DCR is telemetry Home, SD is stowed resting place.

2) Other views: SD = Step 0 (initial position), Sun = Step 58.

3) View displacement: SD-DCR or DCR-Sun = ±108.75° (±29 steps).

4) Step size = 3.75°/step (can rotate 360° continuously; max step input = 95).

5) Step rate = 80 steps/second with pulse width = 12.5 mS.

For sequential pulses, ending pulse width = 60 mS.

SRCA Motor Features: See data below Table 10-11.

* Listed open door step counts are theoretical mechanical design values. Subsequent Flight Software used [values] from MFI-28 test. Added steps account for motor backlash and linkage freeplay.

Generally, if any door or calibrator motor is in operation, further operations for that motor should not be attempted for that motor (except for the Stop Motor Command) until the current operation is complete.

10.8.5 Bus Stop Motor command. Table 10-7 indicates the structure for the high level Stop Motor command.

TABLE 10-7. BUS STOP MOTOR COMMAND STRUCTURE

MSB 0 4	5 7	8 13	LSB 15
10110	000	00000	MTR

This command causes the selected stepper motor to be halted at its current position. The 3-bit MTR parameter selects the motor as follows:

000: INVALID.

001: Nadir Aperture Door Motor.

010: Space View Door Motor

011: Solar Diffuser Door Motor.

100: SDSM Motor.

101: INVALID (was SRCA Filter Wheel Motor.)

110: INVALID (was SRCA Entrance/Exit Slit Motor.)

111: SRCA Grating Motor.

When received, the indicated motor will be halted, aborting any previous command in process. If the specified motor is not currently in use, this command will have no effect. In the case of the SDSM Motor, any Trigger SDSM command partially completed will be abandoned.

10.8.6 Bus Trigger SDSM command. Table 10-8 indicates the structure for the high level Trigger SDSM command. If a Stop Motor command for the SDSM motor is received while a Trigger SDSM command is active, the motor will be halted in its current position, and the Trigger SDSM command will be abandoned.

TABLE 10-8. BUS TRIGGER SDSM COMMAND STRUCTURE

MSB 0 4	5 7	8 13	14 15 LSB
10101	001	000000	Mode
00000000		N	

This command causes the Solar Diffuser Stability Monitor (SDSM) pointing mirror to be stepped between 2 or 3 view positions, over the next N number of scans.

The SDSM motor is stepped during the "inactive" portion of the scan mirror following the Earth Sector. The stopping view positions (and consequently, the data collected by the SDSM sensors) are determined by the two-bit Mode field as follows:

00: INVALID.

01: Solar Diffuser - DC Restore (2 views).

10: Sun - DC Restore (2 views).

11: Solar Diffuser - DC Restore - Sun (3 views).

In each case, the SDSM motor is stepped to a new viewing location each scan. Data is collected from the SDSM sensors in three locations in the scan, after each of the Solar Diffuser, SRCA, and Space sectors. If the Mode is 01, the view alternates between the Solar Diffuser and the internal restore surface. If the Mode is 10, the view alternates between the Sun and the internal restore surface. If the Mode is 11, the view goes from the Solar Diffuser, to the Restore surface, to the Sun, to the restore surface, and back to the Solar Diffuser, and so on.

Bits 8 through 13 of the first word should always be zero. Bits 0 through 7 of the second word should always be zero.

Bits 8 through 15 of the second word specify the number of scans that this stepping sequence takes place. Thus, this command may specify from 1 to 255 scans. After the specified number of scans, the SDSM is stepped (or left) in the Solar Diffuser view position.

This command may take up to 378 seconds to complete. If received from the Command and Telemetry Bus interface, other commands can be received and executed while the SDSM is being stepped. If executed from a macro command, a delay command can be inserted after this command to prevent the next command in the macro from being executed until the SDSM operation has been completed. If, while this command is being executed, the same command is attempted again (through the command and telemetry interface or a macro command) the second command will be discarded.

The three sets of nine spectral samples are down linked in the science engineering packet.

10.8.7 Deleted. TABLE 10-9. DELETED (OP Code 10000)

10.8.8 Deleted. TABLE 10-10. DELETED (OP Code 01111)

10.8.9 Bus Set SRCA Motor command. Table 10-11 indicates the structure for the high level Set SRCA Motor command.

TABLE 10-11. BUS SET SRCA MOTOR COMMAND STRUCTURE

MSB						LSB
0 4	5 6	7 8	10	11 13	14	15
10001	001	000		FW	Slits	
Grating/Mirror Position						

This command sets the three SRCA motors to specific positions as defined by the fields described below.

a. FW: Bits 11-13 of the first word select one of the six positions of the SRCA Filter Wheel (1). The filter wheel has no mechanical stops and could rotate 360°, but it is stepped CW-increasing or CCW-decreasing in terms of absolute-step count. Its positions are:

   000: Position 0 = Neutral Density Filter = Step 0.

   001: Position 1 = Open & Home Telemetry = Step 20.

   010: Position 2 = Order Filter #1 = Step 40.

   011: Position 3 = Order Filter #2 = Step 60.

   100: Position 4 = Order Filter #3 = Step 80.

   101: Position 5 = Dichroic Beam Combiner = Step 100.

   110: Unused code - INVALID.

   111: Unused code - INVALID.

b. Slits: Bits 14 and 15 select one of three positions of the Entrance/Exit Slits (2). Entrance/Exit features serve dual functions according to the SRCA mode of operations. Here, the three positions are defined only in terms of "Exit Reticles". Home is the middle position with the other two at ±90° from it. Hard stops occur at less than one step beyond the ±90° limits. Increased step count equals CCW motor motion. The Exit positions with absolute-step count are:

   00: Position 0 = Along Track Reticle = Step 0.

   01: Position 1 = Along Scan Reticle & Home Telemetry =Step 24.

   10: Position 2 = Slit Reticle (also SiPd) = Step 48.

   11: Unused code - INVALID.

   The Exit Slit Reticle has a related Entrance Slit Reticle, but the other two Exit Reticles have open entrance features.

c. Grating/Mirror: The 16-bit field specifies one of 61,200 positions of the SRCA Grating/Mirror assembly (3). It is used at the Mirror Home position (step count = 0) for radiometric and spatial SRCA calibrations. For spectral calibration, the grating is moved CW (increasing step count) about 186° to get to the useful grating spectral region. Then Table 10-12 is used to step and take data collections across several zones covering a total range of -9.5° (to 195.5° CW). The grating motor has no mechanical stops, and can move Forward or Backward. Data collection points would normally be approached from the same direction to eliminate backlash effects. The grating motor has a harmonic drive reduction ratio of 255 to provide an output step size of -0.006°/step. Two encoder outputs are provided, the motor input to the driver and the driver output. The driver output Home position only occurs once per revolution, while the motor encoder input will produce 255 pulses for each driver output pulse. Home position for the Grating/Mirror corresponds to the coincident condition of reduction input Home and reduction output Home, and is the only direct hardware telemetry reference.

(1) Filter Wheel Motor Features: (see 10.8.9.a for specific positions)

1) Step size = 3°/step, Increasing steps = Mtr CW.
2) Adjacent position step = 60°/3° = 20 steps (max input = 119).
3) Step rate = 6.6666 steps/second with pulse width = 150 mS.

(2) Slit Motor Features: (see 10.8.9.b for specific positions)

1) Step size = 3.75°/step, Increasing steps = Mtr CCW.
2) Adjacent position step = 90°/3.75 = 24 steps (max input = 48).
3) Hard stops are less than 1 step beyond 90° limit positions.
4) Step rate = 5.3333 steps/second with pulse width = 187.5 mS.

(3) Grating/Mirror Motor Features: (numerous positions)

1) Reduction input step size = -1.5°/step; reduction ratio = 255.
2) Output average step size = 1.5°/255 = 0.00589°/step.
   Forward direction = Increasing steps = Mtr CW.
3) Total input steps = 360°/1.5°/step = 240 steps.
4) Total output steps = 240x255 = 61,200 (max input = 61199).
5) Step rate = 150 steps/second with pulse width = 6.667 mS.
   For sequential pulses, ending pulse width = 60 mS.

10.8.10 Bus Step SRCA Grating command. Table 10-12 indicates the structure for the high level Step SRCA Grating command.

TABLE 10-12. BUS STEP SRCA GRATING COMMAND STRUCTURE

MSB								LSB
0	1	2	3	4	5	6	7	8 ... 15
10010					001			Total Bursts
0	D	Steps/Burst						Scans/Burst

This command causes the SRCA grating position to be incremented in a controlled fashion. Bits 8-15 of the first word in the command are an unsigned integer value equal to the total number of bursts to be sent to the SRCA Grating/Mirror stepper motor. A burst is a set of step pulses sent as rapidly as possible, without stopping for data collection. This command allows for up to 255 bursts in a single command.

Bit 0 of the second word is always zero. Bit 1 (D) of the second word is a flag indicating the direction of stepping: 1 increases (forwards) the position of the grating motor, 0 decreases (backwards) the position of the grating motor. Bits 2-7 of the second word in the command are an unsigned integer value equal to the number of steps per burst, allowing for up to 63 grating steps per burst. A burst of step pulses to the SRCA causes the grating to be moved in increments larger than a single step between stops for data collection. Bits 8-15 of the second word in the command are an unsigned integer value equal to the number of scans/per burst, giving a possible value of up to 255 scans per burst. This field allows the user to control how long the grating remains in a particular position before moving on to the next position.

In summary, the total bursts field defines how many stepper transitions are desired. The steps per burst field specifies how large a movement is made for each burst. The scans per burst specifies the spacing between the bursts. As an example, the command 9120/0A04 (hexadecimal) corresponds to 32 bursts (20 hexadecimal = 32 decimal), in bursts of 10 steps (0A hex = 10 decimal), with a delay of 4 scans between each burst (04 hex = 4 decimal), with the direction of stepping toward the lowest position. This results in 32 bursts, at 1.477 * 4 = 5.908 seconds per burst, for a total of 189.056 seconds to complete the command. In practice, the Grating would be moved by another command to the starting point for this step/scan collect/burst process.

This command may take several minutes to complete. If executed from a macro command list, a delay command can be inserted after this command to prevent the next command in the list from being executed until all grating steps have been taken. If received from the Command and Telemetry Bus interface, other commands will be received and executed while the grating is being stepped. If, while this command is being executed, the same command is attempted again (through the command and telemetry interface or a macro command) the second command will be discarded.

Additionally, if there is a Step SRCA Grating command active and a Set SRCA Motors command is attempted, the Step SRCA Grating command will be abandoned, and the Set SRCA Motors command will be executed. If a Stop Motor command for the SDSM motor is received while a Step SRCA Grating command is active, the motor will be halted in its current position, and the Step SRCA Grating command will be abandoned.

10.8.11 Bus Execute macro command. Table 10-13 indicates the structure for the Execute Macro command.

TABLE 10-13. BUS EXECUTE MACRO COMMAND STRUCTURE

MSB			LSB
0 4	5 7	8 10	11 15
11000	000	000	macro cmd #

This command causes the control processor to perform a sequence of commands stored in the instrument. There are 32 different macros. Each macro can up to 1024 command words long.

The command sequences which make up the macros may include any of the instrument commands with the expception of the following:

a. Relay or Parameter commands causing non-reversible actions.

b. Memory Load Initiate.

c. Memory Dump Initiate.

d. Memory Transfer Clear.

e. Macro Commands

f. Macro Abort commands

When a macro command is received, the instrument loads the 1024 command words which comprise the macro into a RAM-based table. The source for the data to go into the table is selected by the macro number. Macros 0-30 are loaded from EEPROM locations in the control processor. These macros are installed as part of the flight software. Macro number 31 is loaded from another RAM-based table. This table can be loaded by external command, giving the users the ability to modify existing macros or create new ones for use without having to release or install the flight software.

Commands are executed by the control processor each scan after the EARTH sector. Commands sent over the 1553 are executed first. After these commands (if any) have been executed, command words are read from the macro data table and executed as if they had been received over the 1553 bus. If a Macro Delay command is read, execution of commands out of the macro table will be suspended until the number of scans specified in the command have passed.

Table 10-23 lists the instrument functions that will be implemented with macro commands.

10.8.12 Bus Delay Macro command. Table 10-14 indicates the structure for the Delay Macro command.

TABLE 10-14. BUS DELAY MACRO COMMAND STRUCTURE

MSB 0 — 4	5 — 7	8 — LSB 15
11010	000	N-1

This causes a pause of N scans in the execution of a macro command. If the command is received directly from the ground, it is accepted as a valid command, but ignored. When contained in a macro command sequence, only that macro is suspended. All other macros may continue execution, and commands received from the ground will continue to be processed.

10.8.13 Bus Abort Macro command. Table 10-15 indicates the structure for the Abort Macro command.

TABLE 10-15. BUS ABORT MACRO COMMAND STRUCTURE

MSB 0 — 4	5 — 7	8 — 10	11 — LSB 15
10100	000	000	macro cmd #

This command causes the control processor to abort a currently executing macro command.

10.8.14 Bus Break command. Table 10-16 indicates the structure for the Break command.

TABLE 10-16. BUS BREAK COMMAND STRUCTURE

MSB 0 — 4	5 — 7	8 — LSB 15
11001	000	00000000

This command is used to indicate the end of a macro command in the macro expansion list. If received over the 1553, it is accepted as legal but has no effect other than generating the proper response.

10.8.15 Bus memory load commands. Table 10-17 indicates the 8 word structure for the Memory Load Initiate command.

TABLE 10-17. BUS MEMORY LOAD INITIATE COMMAND STRUCTURE

MSB 0 1 2 3 4 5 7 8 LSB 15			
11011	111	Table	
P	CLS	00000 0000000	A
load start address (most significant word)			
load start address (least significant word)			
word count (most significant word)			
word count (least significant word)			
verification code (most significant word)			
verification code (least significant word)			

This command is defined in the GIIS section 6.1.3.2. The command is sent to subaddress 1 and is followed by the actual load data, sent to subaddress 2. The load initiate command should be separated from the subsequent data transfer by at least 500 milliseconds, and from the next load initiate command by 1 second.

MODIS limits the maximum length of memory loads to 32 words. The uploaded data is first stored in a temporary buffer, the verification code is validated and only then are the contents of the destination address updated.

Bits 8 through 15 of the first word specify which table is being edited. This value should always be zero unless the memory class (defined below) is equal to TABLE. Tables that may be edited are listed in Table 10-24. In memory loads to tables, the "load start address" parameter contains the offset from the beginning of the indicated table.

Bit 0 (P) of the second word identifies the processor memory being loaded as the Control Processor (0), or the Format Processor (1).

Bits 1-2 (CLS) of the second word contain the memory class, defined as follows:

00: Table

01: Instruction Logical

10: Operand Logical

11: Physical

The Table class allows certain predefined tables to be loaded with new values. The remaining three classes access the processor memory space directly. Physical memory loads access the 20-bit physical address space of the CPU. This class of load can be used to access memory which is not ordinarily present in the processors logical address space (e.g. the Format Engine Writable Control Store). The Instruction Logical and Operand Logical classes are used to access 16-bit logical addresses in the processor. These

two classes each assume that the specified address is the same address state as the main program. These classes can be used for loading small patches during normal operation, or loading new executable code while in the memory upload mode.

Bits 3-14 of the second word are always zero.

Bit 15 of the second word determines the type of access for this load. A value of zero implies a memory load. A value of one implies an I/O load. In the case of an I/O load, the Class of the load (bits 1-2 of this word) must be either Instruction Logical or Operand Logical, and the address must be in the range 0000-7FFF. I/O loads are used to execute XIO Write instructions in the 1750 microprocessor.

Words 3-4 contain the address of the load. If the memory class is physical, word 3 must be in the range 0-15. If the memory class is not physical, word 3 must be zero. If the memory class is Table, the address plus the length (defined below), must be within the total size of the table.

Words 5-6 contain the size of the data to be loaded. Word 5 must always be zero. Word 6 must be in the range 1-32.

Words 7-8 contain the verification code for the load. Word 7 is always zero. Word 8 contains a 16-bit CRC computed over the data words to be uploaded as described in 152930 MODIS Flight Software Detailed Design.

See related reference information in Appendix E, 50.2 for resets/loads, 50.3 for memory types, 50.4 for flight software component checksums, and 50.5 for the CRC checksum algorithm.

10.8.16 Deleted.

TABLE 10-18. DELETED

MSB 0	4	5	7	8	LSB 15
00110					

10.8.17 Bus Restart command. Table 10-19 indicates the structure for the Restart command.

TABLE 10-19. BUS RESTART COMMAND STRUCTURE

MSB 0	4	5	7	8	9	11	12	LSB 15
01001		000		P	000		New AS	

The Restart command is used to transfer execution control to a new address in either of the two MODIS Processors. Bit 8 identifies the processor to be restarted as the Control Processor (0), or the Format Processor (1). Bits 9-11 are unused and must always be zero. Bits 12-15 specify the new address state. The new Instruction Counter and new Interrupt Mask are both always 0000.

10.8.18 Bus Memory Transfer clear command. Table 10-20 indicates the structure for the Memory Transfer Reset command.

TABLE 10-20. BUS MEMORY TRANSFER CLEAR COMMAND STRUCTURE

MSB 0 4	5 7	8 9 10 11 LSB 15
11100	000	00000000

This command is used to reset the internal state machine controlling the memory load and dump commands. Receipt of this command will cause the instrument to cancel any loads or dumps currently in progress.

10.8.19 Bus Memory Dump commands. Table 10-21 indicates the 6 word structure for the Memory Dump Initiate command.

TABLE 10-21. BUS MEMORY DUMP INITIATE COMMAND STRUCTURE

MSB 0 4	5 7	8 9 10 11 LSB 15
11110	101	Table
P	CLS	00000 0000000 A
dump start address (most significant word)		
dump start address (least significant word)		
word count (most significant word)		
word count (least significant word)		

This command is defined in the GIIS section 6.1.3.2. A memory dump consists of a dump initiate command sent to receive subaddress 1, followed by a read of the dump data from transmit subaddress 2. The dump initiate command should be separated from the subsequent data transfer by at least 500 milliseconds, and from the next dump initiate command by 1 second. The maximum dump size is 32 words.

Bits 8 through 15 of the first word specify which table is being dumped. This value should always be zero unless the memory class (defined below) is equal to TABLE. Tables that may be dumped are listed in Table 10-24. In memory dumps from tables, the "Dump Start address" parameter contains the offset from the beginning of the indicated table.

Bit 0 (P) of the second word identifies the processor memory being dumped as the Control Processor (0), or the Format Processor (1).

Bits 1-2 (CLS) of the second word contain the memory class, defined as in the Memory Load Initiate Command (Table 10-17).

Bits 3-14 of the second word are always zero.

Bit 15 of the second word determines the type of access for this dump. A value of zero implies a memory dump. A value of one implies an I/O dump. In the case of an I/O dump, the Class of the dump (bits 1-2 of this word) must be either Instruction Logical or Operand Logical, and the address must be in the range 8000-FFFF. I/O dumps are used to execute XIO Read instructions in the 1750 microprocessor.

Words 3-4 contain the start address of the dump, as defined in the Memory Load Initiate Command (Table 10-17).

Words 5-6 contain the size of the data to be dumped, defined as in the Memory Load Initiate Command (Table 10-17).

See related reference information in Appendix E, 50.3 for a brief description of MODIS memory types.

10.8.19a Bus Set AEM Parameter command. Table 10-21A indicates structure for the Set AEM Parameter command.

TABLE 10-21A. BUS SET AEM PARAMETER COMMAND STRUCTURE

MSB										LSB
0	1			4	5		7	8	9	10					15
01011					001			Value							
G	P	00			Band						Channel				

This command is used to set an individual AEM Gain or offset parameter. The Gain and Offset tables are loaded into the AEM electronics once per scan. This command will have the effect of loading the specified parameter after any other offset computation has been performed for the specified channel.

Bits 8 through 15 of the first word specify the 8-bit value which is to be loaded.

Bit 0 (G) of the second word is the Gain/Offset select bit. G=1 indicates the Value is a Gain value. G=0 indicates the Value is an Offset value.

Bit 1 (P) of the second word is the Preamp/Postamp select bit. P=1 indicates the Value is a Preamp value. P=0 indicates the Value is a Postamp values. This bit applies only to the offset table for bands 31-36. If the band is 1-30, or if the value is a Gain (G=1), this value must be zero.

Bits 2-3 of the second word is unused and must always be zero.

Bits 4-9 of the second word specify the band of the parameter to be modified. This field must be in the range 1-36.

Bits 10-15 of the second word specify the channel of the parameter to be modified. For Bands 1 and 2, this field must be in the range 1-40. For Bands 3-7, this field must be in the range 1-20. For Bands 8-12, and 15-36, this field must be in the range 1-10. If the Band is 13-14, this field must be in the range 1-20. For bands 13 and 14, channels 1-10 represent the Low Gain sampling of detectors 1-10, and channels 11-20 represent the High Gain sampling of detectors 1-10.

10.8.19b Bus Find Motor Home command. Table 10-21b indicates structure for the Find Motor Home command.

TABLE 10-21B. BUS FIND MOTOR HOME COMMAND STRUCTURE

MSB				LSB
0 4	5 7	8	9 12	13 15
00100	000	D	0000	MTR

This command will cause the specified motor to step until its home position is reached. The 3-bit MTR parameter in bits 13-15 selects the motor as follows:

000: INVALID.

001: Nadir Aperture Door Motor.

010: Space View Door Motor

011: Solar Diffuser Door Motor.

100: SDSM Motor.

101: SRCA Filter Wheel Motor.

110: SRCA Entrance/Exit Slit Motor.

111: SRCA Grating Motor.

For the calibrator motors (SDSM Motor, SRCA Filter Wheel Motor, SRCA Entrance/Exit Slit Motor and the SRCA Grating Motor), the direction of stepping is determined by bit 8 (0 = decreasing position, 1 = increasing position). For the three Door motors, the direction of stepping is always toward the CLOSED position. The motor will be stopped when it reaches its home position, but in no case will be stepped more than the total number of steps between minimum and maximum. Because the SRCA Entrance/Exit Slit Motor has its home positions in the middle of its range of motion, the motor will be stepped in the specified direction for 24 steps. When the motor reaches its home positions, then current position entry in the software data structures will be updated to the Home position. If for any reason Home was not found, a warning error event will be issued.

Note: The SRCA Entrance/Exit Slit Motor is the only calibrator motor that has hard stops. These are within a step of its ± limits from home. Because of this, no further automatic find home trials are attempted beyond what is defined above. Test/operations personnel should examine the prior and current telemetry for evaluation of additional corrective action.

10.8.19c Bus Set Motor Position command. Table 10-21c indicates structure for the Set Motor Position command.

TABLE 10-21C. BUS SET MOTOR POSITION COMMAND STRUCTURE

MSB			LSB
0 4	5 7	8 12	13 15
00111	001	00000	MTR
Value			

This command causes the value in the second word to be loaded into the Motor Data table in the flight software. This value becomes the new "Current Position" for the specified motor. The 3-bit MTR parameter in bits 13-15 is defined as follows:

000: INVALID.

001: Nadir Aperture Door Motor.

010: Space View Door Motor

011: Solar Diffuser Door Motor.

100: SDSM Motor.

101: SRCA Filter Wheel Motor.

110: SRCA Entrance/Exit Slit Motor.

111: SRCA Grating Motor.

The Value parameter in the second word is restricted to the range of legal step positions listed in sections 10.8.4 and 10.8.9. Any value outside the range of a particular motor is rejected, and no change is made to the Motor Data table.

10.8.20 Software support tables. Tables 10-22, 23 and 24 provide support data for command structures and operating processes.

TABLE 10-22. PARAMETERS CONTROLLED BY BUS PARAMETER COMMAND

See Table 10-3 for Set Parameter Command Structure.

Param ID#	Command Mnemonic	Parameter Description	SW Range HEX, unless noted
1 BB04	SET_BB_HTR_TEMP TO D#XXXX	BB Heater Temp Set Point, nominal T=315K:A=147DN,B=143DN	005F-0F44 (DN≥95)
2 CP06	SET_CP_TMF_BUS TO A/B	Select CP TMF Bus 0=A, 1=B	0000=A 0001=B
3 TG04	RESET_TG	Reset Timing Generator (Reset=0; negative transition created by Flt SW stepping 1, then 0; no gnd Set cmd)	0000=RESET
4	SPARE	na	na
5 FR08	SET_FR_SCI_APID TO D#XXX	Science Data Packet APID 11 bits	0040-007F
6 FR09	SET_FR_SCI_QLK RESET_FR_SCI_QLK	Science Data Packet QL bit	0001=SET 0000=RESET
7 FR11	SET_FR_ENG_APID TO D#XXX	Engineering Packet APID 11 bits	0040-007F
8 FR12	SET_FR_ENG_QLK RESET_FR_ENG_QLK	Engineering Packet QL bit	0001=SET 0000=RESET
9 FR14	SPARE	(Was Memory Data Packet APID) 11 bits	na
10 FR16	SET_FR_SCIABNORM TO ABNORM/NORM	0=ABNORM, 1=NORM (Flag for abnormal Sci other than MODIS)	0000=ABNORM 0001=NORM
11 FR17	SET_FR_SD_DELAY TO D#XXX	SD Sector Delay (1=6.66us) 7-bit operational test delay	0000-0032
12 FR18	SET_FR_SR_DELAY TO D#XXX	SR Sector Delay (1=6.66us) 7-bit operational test delay	0000-0032
13 FR19	SET_FR_BB_DELAY TO D#XXX	BB Sector Delay (1=6.66us) 7-bit operational test delay	0000-0032
14 FR20	SET_FR_SP_DELAY TO D#XXX	SPACE Sector Delay (1=6.66us) 7-bit operational test delay	0000-0032
15 FR21	SET_FR_EA_DELAY TO D#XXX	EARTH Sector Delay (1=6.66us) 7-bit operational test delay	0000-0032
16 CP07	SET_CP_OPER_MODE TO SRV/SAF/STBY/ OG/SCI	MODIS Operating MODE 3 bits	0001=SURVIVAL 0002=SAFE 0003=STANDBY 0004=OUTGAS 0005=SCIENCE
17 CP04,05	ENABLE_CP_IMOK DISABLE_CP_IMOK	Enable Autonomous Safe Mode (monitor S/C IMOK over 1553)	0001=ENABLED 0000=DISABLED

TABLE 10-22. PARAMETERS CONTINUED

18 SR05	SET_SR_L10WX3 TO B#ABCD	Set 3x10W Lamp Config (selects 3 particular lamps) 4 bits	B#1110=Lamps 1,2,3 B#1101=Lamps 1,2,4 B#1011=Lamps 1,3,4 B#0111=Lamps 2,3,4
19 SR06	SET_SR_L10WX2 TO B#ABCD	Set 2x10W Lamp Config (selects 2 particular lamps) 4 bits	B#1100=Lamps 1,2 B#1010=Lamps 1,3 B#1001=Lamps 1,4 B#0110=Lamps 2,3 B#0101=Lamps 2,4 B#0011=Lamps 3,4
20 SR07	SET_SR_L10WX1 TO B#ABCD	Set 1x10W Lamp Config (selects 1 particular lamp) 4 bits	B#1000=Lamp 1 B#0100=Lamp 2 B#0010=Lamp 3 B#0001=Lamp 4
21 FR08	SET_SR_L1WX1 TO B#AB	Set 1x 1W Lamp Config (selects 1 particular lamp)	B#10=Lamp 5 B#01=Lamp 6
22 CP21	CP_SPARE, (was SET_CP_PK_PWR)	Peak Power Limit by Current (initial I=2042 mA = 245W/120)	0000-0BB8 07FA=2042 mA
23 FR07	SET_FR_RATE TO DAY/NIGHT	Formatter Day/Night Rate	0001=Day 0000=Night
24 FR04	TOGGLE_FR_INT02	Formatter Interrupt02 Toggle FLT SW toggles B#0,1,0 for test	0000=TOGGLE
25 FR05	RESET_FR_STD	Reset Formatter Standard (Reset=0; negative transition created by Flt SW stepping 1, then 0; no gnd Set cmd)	0000=RESET
26 FR22	RESET_FR_UPLD	Reset Formatter Upload (Reset=0; negative transition created by Flt SW stepping 1, then 0; no gnd Set cmd)	0000=RESET
27 FO06	SPARE	(Was Reset FIFO)	na
28 FI04	RESET_FI	Reset FDDI (Reset=0; negative transition created by Flt SW stepping 1, then 0; no gnd Set cmd)	0000=RESET
29 DR03	OPEN_DR_UL_LOCK	Must be issued prior to param#30,#31 & #32; SW cancels cmd automatically after 10 sec	0001=OPEN

TABLE 10-22. PARAMETERS CONTINUED

30 DR04	SET_DR_SVD_UL TO ON/OFF	SVD paraffin htr: 0=ON, 1=OFF (irreversible; must occur within 10 sec of param#29; SW timer OFF at 3 min.	0000=ON 3 min 0001=OFF
31 DR05	SET_DR_NAD_UL TO ON/OFF	NAD paraffin htr: 0=ON, 1=OFF (irreversible; must occur within 10 sec of param#29; SW timer OFF at 6 min.	0000=ON 6 min 0001=OFF
32 DR06	SET_DR_SDD_UL TO ON/OFF	SDD paraffin htr: 0=ON, 1=OFF (irreversible; must occur within 10 sec of param#29; SW timer OFF at 6 min.	0000=ON 6 min 0001=OFF
33 DR27	SET_DR_SDD_FS TO ON/OFF	SDD FS parafin htr: 0=ON,1=OFF (irreversible; must occur within 10 min of SDD FS circuit turn ON; SW timer OFF at 3 min.	0000=ON 3 min 0001=OFF
34 PV04	SET_PVVIS_ECAL TO ON/OFF	PV VIS ECAL ON/OFF Electronic Calibation	0000=OFF 0001=ON
35 PV05	SET_PVVIS_VCAL	PV VIS VCAL Volts -8V to +1V over 8 bits	0000=+1V 00FF=-8V
36 PV06	SET_PVVIS_ITWK_V	PV VIS ITWK Volts -2.5V to -4.5V over 8 bits	0000=-2.5V 00FF=-4.5V
37 PV10	SET_PVNIR_ECAL TO ON/OFF	PV NIR ECAL ON/OFF Electronic Calibation	0000=OFF 0001=ON
38 PV11	SET_PVNIR_VCAL	PV NIR VCAL Volts -8V to +1V over 8 bits	0000=+1V 00FF=-8V
39 PV12	SET_PVNIR_ITWK_V	PV NIR ITWK Volts -2.5V to -4.5V over 8 bits	0000=-2.5V 00FF=-4.5V
40 PV16	SET_PVSMIR_ECAL TO ON/OFF	PV SWIR/MWIR ECAL ON/OFF Electronic Calibation	0000=OFF 0001=ON
41 PV17	SET_PVSM_VCAL	PV SWIR/MWIR VCAL Volts -8V to +1V over 8 bits	0000=+1V 00FF=-8V
42 PV19	SET_PVSM_ITWK_V	PV SWIR/MWIR ITWK Volts -2.5V to -4.5V over 8 bits	0000=-2.5V 00FF=-4.5V
43 PV20	SET_PVSM_VDET_V	PV SMIR/MWIR VDET Volts 0V to -8V over 8 bits	0000=-8V 00FF=0V
44 PV24	SET_PVLW_ECAL TO ON/OFF	PV LWIR ECAL ON/OFF Electronic Calibation	0000=OFF 0001=ON
45 PV25	SET_PVLW_VCAL	LWIR VCAL Volts -8V to +1V over 8 bits	0000=+1V 00FF=-8V
46 PV27	SET_PVLW_ITWK_V	PV LWIR ITWK Volts -2.5V to -4.5V over 8 bits	0000=-2.5V 00FF=-4.5V

TABLE 10-22. PARAMETERS CONTINUED

47 PV28	SET_PVLW_VDET_V	PV LWIR VDET Volts 0V to -8V over 8 bits	0000=-8V 00FF=0V
48 PV18	SET_PVSMIR_CSUB TO ON/OFF	SWIR/MWIR Chrg Subtraction ON/OFF, uses ECAL_V for volts	0000=OFF 0001=ON
49 PV26	SET_PVLW_CSUB TO ON/OFF	LWIR Chrg Subtraction ON/OFF, uses ECAL_V for volts	0000=OFF 0001=ON
50 PV31	SET_PV_MEM TO ROM/RAM	PV Memory ROM/RAM normal:RAM; test only:ROM	0000=ROM 0001=RAM
51 FR26	SET_FR_PKT_TYPE TO NORMAL/TEST	FR Packet, Normal is Science, Test creates a fixed CCSDS test packet to check link	0000=NORMAL 0001=TEST
52 FR29	SET_FR_PV_DCRCMP TO ON/OFF	PV DCR computation: 1=ON,0=OFF	0000=OFF 0001=ON
53 FR27	SET_FR_PC_DCRCMP TO ON/OFF	PC DCR computation: 1=ON,0=OFF	0000=OFF 0001=ON
54 FR30	SPARE	(Was PV DCR threshold of BB) 8 bits	na
55 FR28	SPARE	(Was PC DCR threshold of BB) 8 bits	na
56 FR44	FR_SPARE (was SET_FR_PCDCRPRE)	Compute PC Preamp Offsets when PC DCR Debug Mode is ON	0000=OFF 0001=ON
57 FR45	FR_SPARE (was SET_FR_PCDCRPOST)	Compute PC Postamp Offsets when PC DCR Debug Mode is ON	0000=OFF 0001=ON
58 FR43	FR_SPARE (was SET_FR_PCDCRDBG)	PC DCR Debug Mode	0000=OFF 0001=ON
59 FR31	SET_FR_ENC_DELTA	Delta rotates all 5 MODIS views by fixed encoder count	E000=MIN (-8192) 1FFF=MAX (+8191)
60 FR32	SET_FR_BBRADTAB TO NORMAL/TEST	Uses value fixed by FR35 for all ideal BBDY values	0000=TEST 0001=NORMAL
61 FR33	SET_FR_OFFSETTAB TO NORMAL/TEST	Uses value fixed by FR36 and FR37 for offset loading	0000=TEST 0001=NORMAL
62 FR34	SET_FR_GAINTAB TO NORMAL/TEST	Uses value fixed by FR38 for gain loading	0000=TEST 0001=NORMAL
63 FR35	TEST_FR_BBRAD	Specifies 8 bit value for use by FR32	0000=MIN 00FF=MAX
64 FR36	TEST_FR_PVOFFSET	Specifies 8 bit value for use by FR33	0000=MIN 00FF=MAX
65 FR37	TEST_FR_PCOFFSET	Specifies 16-bit value for use by FR33	0000=MIN 3FFF=MAX
66 FR38	TEST_FR_PVGAIN	Specifies 8 bit value for use by FR34	0000=MIN 00FF=MAX
67 PV32	SET_PVVIS_NSTEP	Sets PV VIS FPA step count for ECAL/CSUB mode.	0001=MIN 0028=MAX

TABLE 10-22. PARAMETERS CONTINUED

68 PV33	SET_PVNIR_NSTEP	Sets PV VIS FPA step count for ECAL/CSUB mode.	0001=MIN 0028=MAX
69 PV34	SET_PVSM_NSTEP	Sets PV VIS FPA step count for ECAL/CSUB mode.	0001=MIN 0028=MAX
70 PV35	SET_PVLW_NSTEP	Sets PV VIS FPA step count for ECAL/CSUB mode.	0001=MIN 0028=MAX
71 SR04	SET_SR_SIPD_HTR TO ON/OFF	Turns SRCA SIS RAD SiPD Heater to ON or OFF	0000=OFF 0001=ON
72 SR09	SET_SR_SIS_FB TO RADIANCE/CURRENT	Turns SIS Feedback Control to RADIANCE or CURRENT	0000=CURRENT 0001=RADIANCE
73 SR10	SET_SR_LOV_SHDN TO ENABLE/DISABLE	Set SIS Lamp Overvoltage Shutdown to ENABLE or DISABLE.	0000=ENABLE 0001=DISABLE
74 SR11	SET_SR_LAMPLEVEL TO HIGH/LOW	Set SRCA Lamp Level to HIGH or LOW.	0000=LOW 0001=HIGH
75 SR12	SET_SR_LAMPS TO OFF/1W/10W/ 20W/30W	Sets SRCA Lamps to the configuration set by this command and SR05-SR08	0000=OFF 0001=1W 0010=10W 0011=20W 0100=30W
76 SR21	SET_SR_IR_SRC TO ON/OFF	Turns SRCA IR Source ON or OFF	0000=OFF 0001=ON
77 CP26	SET_CP_LOG_STATE TO D#XX	Sets Operand & Instruction class of loads & dumps	0000=00 000F=15
78 FR46	SET_CP_LOG_STATE TO D#XX	Sets Operand & Instruction class of loads & dumps	0000=00 000F=15

1/ The current status of Table 10-22 is routinely provided in Engineering Packet Segment 2 as indicated in Figure 30-10b and listed in Table 30-5E.

TABLE 10-23. MACRO COMMAND LIST

See Table 10-13 for Macro Command Bus Structure.

Macro #	Title/Function	Remarks
0	All_Off	Executes on active CP 4/
1	Science_B	4/
2	Science_Outgas_B	4/
3	BB_Heated_315K_A	Off by manual command
4	BB_Heated_315K_B (Xstrap in Side_A)	Off by manual command
5	NAD_Close_A	
6	NAD_Open_A	
7	SVD_Close_A	
8	SVD_Open_A	
9	SDD_Close_A	
10	SDD_Open_A	
11	SDD_Screen_Open_A	
12	SDSM_Full_A	Run with Macros 9 & 10 or 11
13	SDSM_SD_A	Run with Macros 9 & 10 or 11
14	SDSM_Sun_A	Run with Macros 9 & 10 or 11
15	OA-19_SRCA_Full_Radiometric_A	
16	OA-20_SRCA_10W_Radiometric_cont_A	Need Macro 27 to turn lamp Off
17	OA-21_SRCA_1W_Radiometric_cont_A	Need Macro 27 to turn lamp Off
18	OA-22.1.1_SRCA_Spectral_30W_A	Need Macro 19 for total spectral
19	OA-22.1.2_SRCA_Spectral_30W_A	Sequel to complete Macro 18
20	OA-22.2.1_SRCA_Spectral_10W_A	Need Macro 21 for total spectral
21	OA-22.2.2_SRCA_Spectral_10W_A	Sequel to complete Macro 20
22	OA-24_SRCA_Along_Scan_Spatial_A	
23	OA-23_SRCA_Full_Spatial_A	
24	SRCA_1W_Spatial_A	
25	OA-27_PV_ECAL_A	
26	Initial_Outgas_A	Need later manual turn OFF
27	SRCA_Off	Needed to close Macro 16 or 17
28	OA-28_PC_ECAL_A	
29		
30		
31	RAM Utility (loaded to RAM)	Upload new sequence of interest

1/ Macros are in EEPROM (except #31) and contents may be dumped via the 1553 bus

2/ Title suffix _A or _B indicates total or major subsystem support sides.

3/ Macros are generally defined by Side_A subsystems without cross strapped subsystems.

4/ Side_B Macros 0, 1 & 2 require S/C BDU commands to switch CP's and PS's.

5/ Some subsystems have full redundancy, some have limited redundancy, see Table 40-1.

6/ OA prefixes relate to Operational Activities in the MODIS Operations Concept Document by GSFC MCST/MODSOT.

TABLE 10-24. MEMORY LOAD/DUMP COMMAND TABLE LIST

See Table 10-17 & 10-22 for Memory Load/Dump Command Structure.

Memory Table #	Subsystem 1/	# of Words	Memory Table Description, 2/
1	FR-E	550	FPA Offset Table (B13/14 by Lo/Hi, not TDI)
2	N/A	0	SPARE
3	FR	2048	Detector Location Table
4	FR-E	550	FPA Gain Table (B13/14 by Lo/Hi, not TDI)
5	FR	1800	Ideal BB Output Table (36 bands x 50 temps)
6	N/A	0	SPARE
7	FR	5	Sector Size Table (# of 333.33µs FD per sector)
8	FR	40	Sector Definition Table (5 sectors x 2 variables x 2 mirror sides x 2 encoder sides)
9	CP	13	Control Processor Power Up Diagnostic Table
10	FR	13	Format Processor Power Up Diagnostic Table
11	CP	250	Command CP07 Modes
12	N/A	0	SPARE
13	CP	12	Blackbody Temperature Weights - Heater Control
14	CP	12	Blackbody Temperature Weights - ACE Control
15	CP	1024	Macro 31 Command List
16	N/A	0	SPARE
17	N/A	0	SPARE
18	N/A	0	SPARE
19	FR	6	PC Band Sample Clock Delays

1/ Data for Subsystems with suffix -E are provided each scan cycle in the engineering packet. Remaining tables are available upon request via 1553 bus.

2/ See 151840 reference Appendix E, 50.3, for a description of individual memory table contents.

10.9 COMMAND HAZARDS AND CONSTRAINTS

The MODIS design is such that there are a minimal number of command hazards and constraints for on-orbit operations. Prior to door unlatch events, most orbit and ground test hazards relate to door motion. The ground test hazards also include scan mirror motion. In either case, the motion aspect creates a personnel test hazard, and for the doors only, a hardware hazard, if the doors were commanded open without first unlatching them.

Other on-orbit hazards are disabling the IMOK monitor, and enabling the control processor EEPROMS in an unsafe state, and without a verified process for loading them.

Table 10-25A Command List has a Safe/Use column that codes Hazards = H and Constraints = C. Table 10-25B provides remarks on the nature of the hazard or constraint. See Note 2 of Table 40-1 MODIS Subsystem Redundancies & Dependencies for 2 subsystems that have dependencies not classified as constraints.

Although there is a logical order to issue commands, almost all commands can be issued at any time and not cause permanent damage. However, there may be a temporary loss of science data until subsystems are appropriately configured. In this regard, the Timing Generator should be turned on early in command sequences to assure 1) proper scan mirror operation, and 2) to prevent PS shutdown if heavy loads are switched. As will be described below, there are a few commands that can result in an irreversible condition. Even these may not result in a loss of science data. A description of the constraints and their impact are as follows.

10.9.1 Thermal constraints. MODIS should not be operated outside its normal minimum and maximum temperature extremes, listed as Alarm Limits for each subsystem in the MODIS Telemetry List in Appendix B. This is just a normal common sense operating constraint. Specific thermal constraints are 1) not to operate the SRCA if the lamp ring temperature exceeds 95°C, and 2) to wait 5 minutes for further SDD operations if the SDD has been run continuously for 1 minute.

10.9.2 Power constraints. MODIS should not normally be operated with more than one side of a subsystem on at a time. Optional configuration choices in any mode should not be selected such that MODIS would exceed its UIID power limits of 225 W average for one orbit, or 225 W average for two orbits, and 285 W peak power.

MODIS flight software does not contain a power-limit checking process. However, the MODIS command structure is such that it is inherently self limiting for mode configurations, and for most other utility configurations. That is, except for three subsystems, the redundant subsystem command structure is A_Side_ON/B_Side_OFF, and vice versa, with a common A/B_OFF. The modes are defined to include commands to turn OFF the three both-sides-on subsystems (power supplies, scan mirror and FAM), and also high power items like the radiative cooler outgas heaters, BB, SDSM and SRCA.

10.9.3 Launch door latches. MODIS has mechanical latches on all doors (SVD, NAD and SDD) to keep them closed without power during launch. All doors utilize paraffin actuators to release the latches. With MODIS power on, two sequential commands (unlatch circuit power-on and the particular unlatch command) probably provides sufficient procedural restraints to preclude inadvertent unlatch conditions, such as sitting on the launch pad. However, to provide additional restraint margin, a flight software interlock command (DR03) has been defined that must be received within 10 seconds prior to receiving each individual door unlatch command. The Flight Software provides timed paraffin actuator heating for each door, one at a time, as listed in Table 10-25A.

The ground test and operations command equipment should employ a halt-and-verify operation on the command pair for each door.

In orbit, the latches are irreversible. In ground test, the latches can be reset with a manual assist.

10.9.4 Door failsafe mechanism. MODIS employs a paraffin actuated failsafe mechanism on each of its doors to permanently move the Solar View Door (SVD) and Nadir Aperture Door (NAD) to an open position and the Solar Diffuser door open and its screen closed, in the event that their normal motor/mechanisms fail. There is a set of relay commands (3 minimum) that must be received in a particular sequence to activate a failsafe mechanism. The Solar Diffuser door/screen requires a series of 4 commands. The sequence is as follows:

1. Select primary/redundant path for NAD and SVD failsafe.
2. Enable first failsafe switch by S/C point-to-point command.
3. Close second failsafe switch by 1553 command.
4. Fire NAD or SVD failsafe as final third step for them.
5. Turn on SDD circuit, third step for SDD.
6. Fire SDD failsafe as final SDD step.

The Flight Software provides timed paraffin actuator heating for each door, one at a time, as listed in Table 10-25A. The automatic timer is started/restarted at each step, beginning at step 1 with a window of 3 minutes. The final heater time (1 min & 40 sec or 3 min) is as listed in the table. If no further commands are received after each step, the timer will time out and execute the common command that opens all sequential failsafe relays.

The ground test and operations command equipment should also employ a halt and confirm operation on each command for steps 2 through 6.

10.10 S/C TMON COMMANDS

There is a limited set of commands that can be issued by the S/C as a result of its Telemetry Monitor (TMON) capability, which is dependent upon the state of the selected MODIS telemetry items. Selected MODIS TMON telemetry and command detail is TBD.

10.11 COMMAND LISTS

Two tables provide specific MODIS command information. Table 10-25A provides the overall MODIS command list sorted by subsystem (Column 1), and Table 10-25B provides remarks about commands designated as a hazard or constraint in Table 10-25A.

Table 10-25A also contains information for hardware/software/GSE development use in columns 5 through 10.

Appendix D addresses command and telemetry relations in subsystem sequence per Table 10-25A. Appendix D also addresses subsystem redundancies and side dependancies (See 40.3 and Table 40-1).

For command implementation completeness and hardware/software development use, Table 10-26 provides a list of digital internal controls (DIC) and relay internal controls (RIC), which also includes spares.

Notes at the bottom of each table explain the contents of the table.

For convenient access, a copy of Figure 11 MODIS Exploded View/Subsystem Abbreviations is repeated and enclosed as the last page of this appendix.

TABLE 10-25A. MODIS COMMAND LIST

Sort by Subsystem - - See Notes - - General User Interest extends through Column 4 - - Shaded area indicates S/C pt-pt cmds to MODIS. *4/97*

PF Chg#	1 Subsys	2 OASIS Command Name	3 Qualifier or Value	4a Safe/ Use	4b Remarks	5 Cmd Type	6 Op Code Table	7 R/P ID#	8 CP HW Address	9 CP HW Data Loc	10 HW Unique ID
	BB01	TURN_ON_BBA		C	BB A_ON, B_OFF (pwr only; CP-CE cntls bang-bang htr on/off)	R	T10-2	01	CXX00	XX25	MM05Q500F
	BB02	TURN_ON_BBB		C	BB B_ON, A_OFF (pwr only; CP-CE cntls bang-bang htr on/off)	R	T10-2	02	CXX00	XX26	MM05Q501F
	BB03	TURN_OFF_BB			BB A&B_OFF	R	T10-2	03	CXX00	XX18	MM05Q502F
22,33, 45	BB04	SET_BB_HTR_TEMP	TO D#XXXX	A	Sets BB heater temp; 12 bits as D#XXXX, integer DN. Values: DN=692=300K, DN=204=313K, DN=151=315K, DN=098=317K. DN range =98 to 3908 (DN3908=270K may be marginal tlmy limit)	SW	T10-3	01	na	na	na
	CE01	TURN_ON_CEA			CE A_ON, B_OFF	R	T10-2	04	CXX00	XX28	MM05Q400F
	CE02	TURN_ON_CEB			CE B_ON, A_OFF	R	T10-2	05	CXX00	XX29	MM05Q401F
	CE03	TURN_OFF_CE			CE A&B_OFF	R	T10-2	06	CXX00	XX2A	MM05Q402F
	CP01	TURN_ON_CPA			CP A_ON, B_OFF	RS	na	na	na	na	MM05R900T
	CP02	TURN_ON_CPB			CP B_ON, A_OFF	RS	na	na	na	na	MM06R900T
	CP03	RESET_CP_STD			CP A&B standard reset (relay-like load; no S/C pt-pt tlmy)	RS	na	na	na	na	MM05/06R903T
	CP04	ENABLE_CP_IMOK			Enable=1 (Disable=0) for CP 5 sec monitor of SCC IMOK/sec	SW	T10-3	17	na	na	na
	CP05	DISABLE_CP_IMOK		H	Disable=0 (Enable=1) for CP 5 sec monitor of SCC IMOK/sec	SW	T10-3	17	na	na	na
	CP06	SET_CP_TMF_BUS	TO A/B		Set CP TMF Bus to B#X=1/0: 1=B, 0=A	SWD	T10-3	02	CXX0B	0	on same PWB
	CP07	SET_CP_OPER_MODE	TO SRV/SAF/STBY/OG/SCI	H	Set Oper Mode to: Survival, Safe, Standby, OG, Science	SW	T10-3	16	na	na	na
44	CP08	PERFORM_CP_MACRO	WITH NUMBER X	H	Gnd cmd Macro D#X (0-31), can't call from another macro	SW	T10-13	na	na	na	na
44	CP09	SET_CP_MACRDELAY	WITH SCANS X		Set CP Macro delay to D#X for 0-255 1.477sec scan delays; only used inside a Flt macro, not as an external cmd; no action if received over 1553	SW	T10-14	na	na	na	na
44	CP10	CLOSE_CP_MACRO			Should be last cmd of any macro to close or end it; not used as an external cmd, no action if received over 1553	SW	T10-16	na	na	na	na
44	CP11	HALT_CP_MACRO	WITH NUMBER X		CP halts or aborts macro with number D#X	SW	T10-15	na	na	na	na
	CP12	DUMP_MEM	(select 9 items, see Op Code)		CP or FR general memory dump cmd, see op code table	SW	T10-21	na	na	na	na
	CP13	RESET_CP_UPLD		A	CP A&B upload reset (opto-isolator, no S/C pt-pt tlmy)	RS	na	na	na	na	MM05/06R905T
	CP14	LOAD_CP_RAM	(select 11 items, see Op Code)		CP or FR(via CP) general memory load, see op code table	SW	T10-17	na	na	na	na
31	CP15	SET_CP_RESTART	WITH ASTATE X#X	C	Restarts CP after major RAM upload affecting operating sys or algorithms; not needed for simple uploads	SW	T10-19	na	na	na	na
	CP16	ENABLE_CPA_EPWRT		H	CPA EEPROM write enable, need to xfer RAM to EEPROM	RS	na	na	na	na	MM05R907T
	CP17	ENABLE_CPB_EPWRT		H	CPB EEPROM write enable, need to xfer RAM to EEPROM	RS	na	na	na	na	MM06R907T
19	CP18	CP_SPARE			Was SET_CP_RAM_XFER	na	na	na	na	na	na
	CP19	HALT_CP_RAM_XFER			Global, halts any CP or FR memory load or dump in process	SW	T10-20	na	na	na	na
	CP20	DISABLE_CP_EPWRT			Global, disable all CP/FR EEPROM A/B write	RD	T10-2	84	CXX00	5AE2	MM05Q302,03F
37	CP21	CP_SPARE			Was SET_CP_PK_PWR	na	T10-3	22	na	na	na
32,44	CP22	SET_SAFE_MODE			S/C initiated go Safe cmd to 1553 Subaddress 7 vs normal cmd Subaddress 1 (not in total cmd count); triggers CP07 SAF	SW	na	na	na	na	na
2	CP23	SET_CP_SC_SPARE	***S/C SPARE***		Wired S/C spare relay cmd (not in bottom total cmd count)	RS	na	na	na	na	MM05,06T
26	CP24	GET_CP_MTR_HOME	WITH MTR D#X, DIR B#X	A	Find tlmy HW Home; Mtr D#X: 0=Invalid, 1=NAD, 2=SVD, 3=SDD, 4=SDSM, 5=Wheel, 6=Slit, 7=Grating. DIR B#X for OBCs: 0=decreasing/1=increasing; doors: don't care 0 or 1	SW	T10-21B	na	na	na	na
26	CP25	SET_CP_MTR_SWPOS	WITH MTR D#X, STEP X#XXXX	A	Set CP SW step position to match known tlmy; Mtr D#X: 0=Invalid, 1=NAD, 2=SVD, 3=SDD, 4=SDSM, 5=Wheel, 6=Slit, 7=Grating. Step X#XXXX useful range is 0 to 61200	SW	T10-21C	na	na	na	na
27	CP26	SET_CP_LOG_STATE	TO D#XX (0 TO 15)		Sets OPERAND & INSTRUCTION class of loads (& dumps)	SW	T10-3	77	na	na	na
	DR01	TURN_ON_DR_ULA			Unlatch drive circuit A_ON, B_OFF, DR_DRVR_OFF	R	T10-2	07	CXX00	XX43	MM05Q896F
	DR02	TURN_ON_DR_ULB			Unlatch drive circuit B_ON, A_OFF, DR_DRVR_OFF	R	T10-2	08	CXX00	XX4B	MM05Q897F

TABLE 10-25A. MODIS COMMAND LIST

Sort by Subsystem - - See Notes - - General User Interest extends through Column 4 - - Shaded area indicates S/C pt-pt cmds to MODIS. *4/97*

PF Chg#	1 Subsys	2 OASIS Command Name	3 Qualifier or Value	4a Safe/ Use	4b Remarks	5 Cmd Type	6 Op Code Table	7 R/P ID#	8 CP HW Address	9 CP HW Data Loc	10 HW Unique ID
39	DR03	OPEN_DR_UL_LOCK			SW unlock to any DR unlatch cmd; provides 10sec open=1 for DR04, 05, 06.	SW	T10-3	29	na	na	na
42	DR04	SET_DR_SVD_UL	TO ON/OFF	H	SVD unlatch paraffin htr: 0=ON, 1=OFF; DR03 must be prior by 10sec; Flt SW timer has 3 min OFF, or OFF by this cmd	SWD	T10-3	30	4XX04	0	MM05D816T
42	DR05	SET_DR_NAD_UL	TO ON/OFF	H	NAD unlatch paraffin htr: 0=ON, 1=OFF; DR03 must be prior by 10sec; Flt SW timer has 6 min OFF, or OFF by this cmd	SWD	T10-3	31	4XX04	1	MM05D817T
42	DR06	SET_DR_SDD_UL	TO ON/OFF	H	SDD unlatch paraffin htr: 0=ON, 1=OFF; DR03 must be prior by 10sec; Flt SW timer has 6 min OFF, or OFF by this cmd	SWD	T10-3	32	4XX04	2	MM05D818T
	DR07	TURN_OFF_DR_PWR			Turns off DR driver & unlatch ckts, 3 sigs to verify pwr off	R	T10-2	09	CXX00	XX49	MM05Q892F
	DR08	TURN_ON_DR_DRV			Turns on door driver power, turns off unlatch ckt power	R	T10-2	10	CXX00	XX3F	MM05Q895F
	DR09	MOVE_DR_SVD	TO CLOSED/OG/OPEN	H	Move SVD to Closed/OG/Open; internal status sets step count	SW	T10-4	na	T10-26	<-	na
	DR10	MOVE_DR_NAD	TO CLOSED/OPEN	H	Move NAD to Closed/Open; internal status sets step count	SW	T10-4	na	T10-26	<-	na
	DR11	SET_DR_SDD_DRVA			Select SDD drive A	R	T10-2	11	CXX00	XX46	MM05Q898F
	DR12	SET_DR_SDD_DRVB			Select SDD drive B	R	T10-2	12	CXX00	XX3C	MM05Q899F
	DR13	MOVE_DR_SDD	TO CLOSED/SCREEN CLOSED/OPEN	H	Move by CP step count to: both SDD-SDS closed/ or only SDD open/or both SDD-SDS open. SDD thermal constraint is to wait 5 minutes if run continuoulsy for one minute.	SW	T10-4	na	T10-26	<-	na
34,47	DR14	STEP_DR_SVD	BY D#XXXX IN/OUT	H	Step SVD by D#XXXX steps IN/OUT (=close/open = mtr CW/CCW = step decrease/increase); max steps=4060	SW	T10-6	na	T10-26	<-	na
34,47	DR15	STEP_DR_NAD	BY D#XXXX IN/OUT	H	Step NAD by D#XXXX steps IN/OUT (=close/open = mtr CCW/CW= step decrease/increase); max steps=3750	SW	T10-6	na	T10-26	<-	na
34,44, 47	DR16	STEP_DR_SDD	BY D#XXXX IN/OUT	H	Step SDD by D#XXXX steps IN/OUT (=close/open = mtr CW/CCW = step decrease/increase); see 10.8.6 for screen. SDD thermal constraint is to wait 5 minutes if run continuoulsy for one minute; max steps=2145	SW	T10-6	na	T10-26	<-	na
	DR17	HALT_DR_STEP_SVD			Halt DR SVD in process stepping	SW	T10-7	na	na	na	na
	DR18	HALT_DR_STEP_NAD			Halt DR NAD in process stepping	SW	T10-7	na	na	na	na
	DR19	HALT_DR_STEP_SDD			Halt DR SDD (includes screen) in process stepping	SW	T10-7	na	na	na	na
	DR20	SELECT_DR_PRI_FS			Select PRI FS for only NAD & SVD	R	T10-2	13	CXX00	XX4A	MM05Q893F
	DR21	SELECT_DR_RDT_FS			Select RDT FS for only NAD & SVD	R	T10-2	14	CXX00	XX4E	MM05Q894F
	DR22	ENABLE_DR_FS		H	Global DR cmd for 1st FS step; disable by 1553 cmd DR28	RS	na	na	na	na	MM12R01T
	DR23	CLOSE_DR_FS_SW2		H	Global DR (NAD,SDD,SVD) 2nd FS step	R	T10-2	15	CXX00	XX48	MM05Q890F
42,44	DR24	FIRE_DR_SVD_FS		H	Final 3rd step to activate SVD FS; Flt SW has 1 min & 40 sec Off; send cmd DR28 after 2 min	R	T10-2	16	CXX00	XX22	MM05Q857F
42,44	DR25	FIRE_DR_NAD_FS		H	Final 3rd step to activate NAD FS; Flt SW has 1 min & 40 sec Off; send cmd DR28 after 2 min		T10-2	17	CXX00	XX2C	MM05Q860F
	DR26	TURN_ON_DR_SDDFS		H	Turn on SDD FS ckt; 3 of 4 FS steps for SDD	R	T10-2	18	CXX00	XX2D	MM05Q863F
42	DR27	SET_DR_SDD_FS	TO ON/OFF	H	4th & final step, SDD FS paraffin htr: 0=ON, 1=OFF; OFF by this cmd or cmd DR28; Flt SW timer has 3 min OFF	SWD	T10-3	33	4XX04	3	MM05D820T
	DR28	OPEN_DR_FS_SWS			Global, opens all FS relay SWs (5)	R	T10-2	19	CXX00	XX33	MM05Q864F
	FI01	TURN_ON_FIA			FDDI A_ON, B_OFF	R	T10-2	20	CXX00	XX5B	MM05Q950F
	FI02	TURN_ON_FIB			FDDI B_ON, A_OFF	R	T10-2	21	CXX00	XX5F	MM05Q951F
	FI03	TURN_OFF_FI			FDDI A&B_OFF	R	T10-2	22	CXX00	XX63	MM05Q952F
	FI04	RESET_FI			Active FI Reset=0, No Set cmd, SW steps 1, 0 for chg	SWD	T10-3	28	CXX13	6	MM05D955T,6T
	FI05	SELECT_FI_PORTA			Sets active FDDI to I/F port A	R	T10-2	23	CXX00	XX56	MM05Q953F
	FI06	SELECT_FI_PORTB			Sets active FDDI to I/F port B	R	T10-2	24	CXX00	XX51	MM05Q954F
	FO01	TURN_ON_FO_BLK1			2 of 4 FIFO blocks needed	R	T10-2	25	CXX00	XX14	MM05Q201F

TABLE 10-25A. MODIS COMMAND LIST

Sort by Subsystem - - See Notes - - General User Interest extends through Column 4 - - Shaded area indicates S/C pt-pt cmds to MODIS. *4/97*

PF Chg#	1 Subsys	2 OASIS Command Name	3 Qualifier or Value	4a Safe/ Use	4b Remarks	5 Cmd Type	6 Op Code Table	7 R/P ID#	8 CP HW Address	9 CP HW Data Loc	10 HW Unique ID
	FO02	TURN_ON_FO_BLK2			2 of 4 FIFO blocks needed	R	T10-2	26	CXX00	XX15	MM05Q202F
	FO03	TURN_ON_FO_BLK3			2 of 4 FIFO blocks needed	R	T10-2	27	CXX00	XX16	MM05Q203F
	FO04	TURN_ON_FO_BLK4			2 of 4 FIFO blocks needed	R	T10-2	28	CXX00	XX10	MM05Q205F
	FO05	TURN_OFF_FO			All 4 FIFO blocks to OFF	R	T10-2	29	CXX00	XX27	MM05Q204F
3	FO06	FO_SPARE			FO_Spare - was Rest FO blocks 1,2,3,4	SWD	T10-3	27	CXX13	4	MM05D206T
	FR01	TURN_ON_FRA			FR A_ON, B_OFF	R	T10-2	30	CXX00	XX1B	MM05Q101F
	FR02	TURN_ON_FRB			FR B_ON, A_OFF	R	T10-2	31	CXX00	XX1F	MM05Q102F
	FR03	TURN_OFF_FR			FR A&B_OFF	R	T10-2	32	CXX00	XX13	MM05Q103F
20	FR04	TOGGLE_FR_INT02		T	Interrupt 02 of Active FR toggled from 0, to 1, to 0 by Flt SW ; also accelerates PV DCR for test CSUB ops	SWD	T10-3	24	CXX13	2	MM05D123,27T
	FR05	RESET_FR_STD			Active FR Reset=0, No Set cmd, SW steps 1, 0 for chg	SWD	T10-3	25	CXX13	0	MM05D121,25T
	FR06	FR_SPARE			FR Spare (was On/Off DCR comp or all FPAs,see FR27-30)	na	na	na	na	na	na
	FR07	SET_FR_RATE	TO DAY/NIGHT	C	Sets FR rate to B#X=1/0: 1=DAY. 0=NIGHT	SW	T10-3	23	na	na	na
	FR08	SET_FR_SCI_APID	TO D#XXX	C	Set Sci FPA APID D# 064-127 in science packet header	SW	T10-3	05	na	na	na
	FR09	SET_FR_SCI_QLK			Sets FPA quick look flag to 1 in science packet header	SW	T10-3	06	na	na	na
	FR10	RESET_FR_SCI_QLK			Resets FPA quick look flag to 0 in science packet header	SW	T10-3	06	na	na	na
	FR11	SET_FR_ENG_APID	TO D#XXX	C	Set Sci Eng APID D# 064-127 in engineering packet header	SW	T10-3	07	na	na	na
	FR12	SET_FR_ENG_QLK			Sets Sci Eng quick look flag to 1 in eng packet header	SW	T10-3	08	na	na	na
	FR13	RESET_FR_ENG_QLK			Resets Sci Eng quick look flag to 0 in eng packet header	SW	T10-3	08	na	na	na
18	FR14	FR_SPARE			Was SET_FR_MEM_APID	SW	T10-3	09	na	na	na
31	FR15	SET_FR_RESTART	WITH ASTATE X#X	C	Restarts FR after major RAM upload affecting operating sys or algorithms; not needed for simple uploads	SW	T10-19	na	na	na	na
18,41	FR16	SET_FR_SCIABNORM	TO ABNORM/NORM		Gnd flag to ID abnormal SCI other than MODIS,e.g., manuevers, data link, etc; 0=ABNORM, 1=NORM	SW	T10-3	10	na	na	na
7	FR17	SET_FR_SD_DELAY	TO D#XX	T	Set SD view FPA delay to D#XX(0-50) 0.02IFOVs,1km	SW	T10-3	11	na	na	na
7	FR18	SET_FR_SR_DELAY	TO D#XX	T	Set SRCA view FPA delay to D#XX(0-50) 0.02IFOVs,1km	SW	T10-3	12	na	na	na
7	FR19	SET_FR_BB_DELAY	TO D#XX	T	Set BB view FPA delay to D#XX(0-50) 0.02IFOVs,1km	SW	T10-3	13	na	na	na
7	FR20	SET_FR_SP_DELAY	TO D#XX	T	Set Space view FPA delay to D#XX(0-50) 0.02IFOVs,1km	SW	T10-3	14	na	na	na
7	FR21	SET_FR_EA_DELAY	TO D#XX	T	Set Earth view FPA delay to D#XX(0-50) 0.02IFOVs,1km	SW	T10-3	15	na	na	na
	FR22	RESET_FR_UPLD			Active FR Reset=0, No Set cmd, SW steps 1, 0 for chg	SWD	T10-3	26	CXX13	1	MM05D122,26T
	FR23	ENABLE_FRA_EPWRT		C	Enable FRA EEPROM write, has global CP&FR disable	R	T10-2	33	CXX00	XX5D	MM05Q104F
	FR24	ENABLE_FRB_EPWRT		C	Enable FRB EEPROM write, has global CP&FR disable	R	T10-2	34	CXX00	XX5E	MM05Q105F
19	FR25	FR_SPARE			Was SET_FR_RAM_XFER	na	na	na	na	na	na
21,28	FR26	SET_FR_PKT_TYPE	TO NORMAL/TEST	T	Sets Sci Pkt to Normal=0/Test=1; fixed CCSDS pkt to ck link	SW	T10-3	51	na	na	na
	FR27	SET_FR_PC_DCRCMP	TO ON/OFF		PC FPA DCR offset comp & application On/Off: 1=ON, 0=OFF	SW	T10-3	53	na	na	na
4	FR28	FR_SPARE			FR_SPARE; was: SET_FR_PC_DCR_TH	SW	T10-3	55	na	na	na
	FR29	SET_FR_PV_DCRCMP	TO ON/OFF		PV FPA DCR offset comp & application On/Off: 1=ON, 0=OFF	SW	T10-3	52	na	na	na
4	FR30	FR_SPARE			FR_SPARE; was: SET_FR_PV_DCR_TH	SW	T10-3	54	na	na	na
12	FR31	SET_FR_ENC_DELTA	TO 0, -8192,+8191	T	Delta rotates all view collects, D# to 14-bit X# by 2sC	SW	T10-3	59	na	na	na
15	FR32	SET_FR_BBRADTAB	TO NORMAL/TEST	T	FR BB radiation-vs-temp table to Normal/Test=1/0	SW	T10-3	60	na	na	na
15	FR33	SET_FR_OFFSETTAB	TO NORMAL/TEST	T	FR Offset table to Normal/Test=1/0	SW	T10-3	61	na	na	na
15	FR34	SET_FR_GAINTAB	TO NORMAL/TEST	T	FR gain table to Normal/Test=1/0	SW	T10-3	62	na	na	na
15,35	FR35	TEST_FR_BBRAD	WITH OS X#XXX	T	Sets fixed BB radiation value=X#XXX; no HK tlmy	SW	T10-3	63	na	na	na
15,35	FR36	TEST_FR_PVOFFSET	WITH OS X#XX	T	Sets fixed PV offset value=X#XX; no HK tlmy	SW	T10-3	64	na	na	na
15,35	FR37	TEST_FR_PCOFFSET	WITH OS X#XXXX	T	Sets fixed PC offset value=X#XXXX, where leading XX=preamp offset, trailing XX=postamp offset; no HK tlmy	SW	T10-3	65	na	na	na

TABLE 10-25A. MODIS COMMAND LIST

Sort by Subsystem - - See Notes - - General User Interest extends through Column 4 - - Shaded area indicates S/C pt-pt cmds to MODIS.

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PF Chg#	1 Subsys	2 OASIS Command Name	3 Qualifier or Value	4a Safe/ Use	4b Remarks	5 Cmd Type	6 Op Code Table	7 R/P ID#	8 CP HW Address	9 CP HW Data Loc	10 HW Unique ID
15,35	FR38	TEST_FR_PVGAIN	WITH GN X#XX	T	Sets fixed PV gain value=X#XX; no HK tlmy	SW	T10-3	66	na	na	na
25	FR39	SET_FR_PVGN1C	WITH B D#XX, C D#XX, V X#XX	T	Sets single chan PV gain with Band D#XX, Chan D#XX, ValueX#XX; no HK tlmy	SW	T10-21A	na	na	na	na
25	FR40	SET_FR_PVOS1C	WITH B D#XX, C D#XX, V X#XX	T	Sets single chan PV offset with Band D#XX, Chan D#XX, ValueX#XX; no HK tlmy	SW	T10-21A	na	na	na	na
25	FR41	SET_FR_PCPREOS1C	WITH B D#XX, C D#XX, V X#XX	T	Sets single chan PC preamp offset with Band D#XX, Chan D#XX, ValueX#XX; no HK tlmy	SW	T10-21A	na	na	na	na
25	FR42	SET_FR_PCPSTOS1C	WITH B D#XX, C D#XX, V X#XX	T	Sets single chan PC postamp offset with Band D#XX, Chan D#XX, ValueX#XX; no HK tlmy	SW	T10-21A	na	na	na	na
24,37	FR43	FR_SPARE			Was SET_FR_PCDCRDBG	na	T10-3	58	na	na	na
24,37	FR44	FR_SPARE			Was SET_FR_PCDCRPOST	na	T10-3	57	na	na	na
24,37	FR45	FR_SPARE			Was SET_FR_PCDCRPRE	na	T10-3	56	na	na	na
27	FR46	SET_FR_LOG_STATE	TO D#XX (0 TO 15)		Sets OPERAND & INSTRUCTION class of loads (& dumps)	SW	T10-3	78	na	na	na
	PC01	TURN_ON_PCLWA		C	PC A_ON, B_OFF	RD	T10-2	85	CXX00	0797	MM05Q016,19F
	PC02	TURN_ON_PCLWB		C	PC B_ON, A_OFF	RD	T10-2	86	CXX00	0F8B	MM05Q017,18F
	PC03	TURN_ON_PCLW_AB		C	PC A&B_ON	RD	T10-2	87	CXX00	0F87	MM05Q016,17F
	PC04	TURN_OFF_PCLW			PC A&B_OFF	RD	T10-2	88	CXX00	178B	MM05Q018,19F
	PC05	TURN_ON_PC_ECAL		T	Turns ON PC A&B elex calibration	R	T10-2	35	CXX00	54D0	MM05Q020,22F
	PC06	TURN_OFF_PC_ECAL			Turns OFF PC A&B elex calibration	R	T10-2	36	CXX00	58D5	MM05Q021,23F
	PS01	TURN_ON_PS1		C	Turn ON PS1	RS	na	na	na	na	PS01R01T
	PS02	TURN_ON_PS2		C	Turn ON PS2	RS	na	na	na	na	PS02R01T
	PS03	TURN_ON_PS1_PS2		C	Turn ON both PS1 & PS2	RS	na	na	na	na	PS01/02R01T
	PS04	TURN_OFF_PS1PS2A			Turns OFF both PS1 & PS2; Only Rdt S/C cmd	RS	na	na	na	na	PS01/02R03T
	PS05	TURN_OFF_PS1PS2B			Turns OFF both PS1 & PS2; Only Rdt S/C cmd	RS	na	na	na	na	PS01/02R05T
	PS06	ENABLE_PS12SHDN		A	Enables PS1 & PS2 automatic shutdown	RS	na	na	na	na	PS01/02R06T
	PS07	DISABLE_PS12SHDN			Disables PS1 & PS2 automatic shutdown	RS	na	na	na	na	PS01/02R04T
	PS08	ENABLE_PS1_SVHTR		A	Enables PS1 SrvHtrA cntl, turn on by thermostat sw	RS	na	na	na	na	PS01R02T
	PS09	ENABLE_PS2_SVHTR		A	Enables PS2 SrvHtrB cntl, turn on by thermostat sw	RS	na	na	na	na	PS02R02T
	PS10	DISABLE_PS_SVHTR			Disables A/B SrvHtr	RS	na	na	na	na	PS01/02R07T
	PV01	TURN_ON_PVVISA			PV VIS A_ON, B_OFF	R	T10-2	37	CXX00	XX00	MM05Q001F
	PV02	TURN_ON_PVVISB			PV VIS B_ON, A_OFF	R	T10-2	38	CXX00	XX01	MM05Q002F
	PV03	TURN_OFF_PVVIS			PV VIS A&B_OFF	R	T10-2	39	CXX00	XX02	MM05Q004F
	PV04	SET_PVVIS_ECAL	TO ON/OFF	T	PV VIS A or B elex calibration, B# 1=ON, 0=OFF	SWD	T10-3	34	CXX13	9	MM05D003,04T
6,44	PV05	SET_PVVIS_VCAL	TO X#XX	T	Set PV VIS VCAL, 8bits, +1V=X#00 to -8V=X#FF; soft saturation occurs at D#173 = X#AD = -5.7V	SW	T10-3	35	na	na	na
	PV06	SET_PVVIS_ITWK_V	TO X#XX	C	Sets VIS ITWK, 8bits, -2.5V=X#00 to -4.5V=X#FF	SW	T10-3	36	na	na	na
	PV07	TURN_ON_PVNIRA			PV NIR A_ON, B_OFF	R	T10-2	40	CXX00	XX0A	MM05Q005F
	PV08	TURN_ON_PVNIRB			PV NIR B_ON, A_OFF	R	T10-2	41	CXX00	XX04	MM05Q006F
	PV09	TURN_OFF_PVNIR			PV NIR A&B_OFF	R	T10-2	42	CXX00	XX05	MM05Q008F
	PV10	SET_PVNIR_ECAL	TO ON/OFF	T	PV NIR A or B elex calibration, B# 1=ON, 0=OFF	SWD	T10-3	37	CXX13	C	MM05D016,18T
6,44	PV11	SET_PVNIR_VCAL	TO X#XX	T	Set PV NIR VCAL , 8bits, +1V=X#00 to -8V=X#FF; soft saturation occurs at D#173 = X#AD = -5.7V	SW	T10-3	38	na	na	na
	PV12	SET_PVNIR_ITWK_V	TO X#XX	C	Set PV NIR ITWK, 8bits, -2.5V=X#00 to -4.5V=X#FF	SW	T10-3	39	na	na	na
	PV13	TURN_ON_PVSMIRA			PV SMIR A_ON, B_OFF	R	T10-2	43	CXX00	XX64	MM05Q013F
	PV14	TURN_ON_PVSMIRB			PV SMIR B_ON, A_OFF	R	T10-2	44	CXX00	XX0C	MM05Q014F
	PV15	TURN_OFF_PVSMIR			PV SMIR A&B_OFF	R	T10-2	45	CXX00	XX0D	MM05Q015F

TABLE 10-25A. MODIS COMMAND LIST

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PF Chg#	1 Subsys	2 OASIS Command Name	3 Qualifier or Value	4a Safe/ Use	4b Remarks	5 Cmd Type	6 Op Code Table	7 R/P ID#	8 CP HW Address	9 CP HW Data Loc	10 HW Unique ID
	PV16	SET_PVSMIR_ECAL	TO ON/OFF	T	PV SMIR A or B elex calibration, B# 1=ON, 0=OFF	SWD	T10-3	40	CXX13	B	MM05D015,17T
6,44	PV17	SET_PVSM_VCAL	TO X#XX	T	Set PV SMIR VCAL, 8bits, +1V=X#00 to -8V=X#FF; soft saturation occurs at D#173 = X#AD = -5.7V	SW	T10-3	41	na	na	na
	PV18	SET_PVSMIR_CSUB	TO ON/OFF	T	Active SMIR test only chrg subtraction to 1=ON, 0=OFF	SWD	T10-3	48	CXX13	7	MM05D007,08T
	PV19	SET_PVSM_ITWK_V	TO X#XX	C	Set PV SMIR ITWK, 8bits, -2.5V=X#00 to -4.5V=X#FF	SW	T10-3	42	na	na	na
	PV20	SET_PVSM_VDET_V	TO X#XX	C	Set PV SMIR VDET, 8bits, -8V=X#00 to 0V=X#FF	SW	T10-3	43	na	na	na
	PV21	TURN_ON_PVLWA			PV LWIR A_ON, B_OFF	R	T10-2	46	CXX00	XX06	MM05Q009T
	PV22	TURN_ON_PVLWB			PV LWIR B_ON, A_OFF	R	T10-2	47	CXX00	XX0E	MM05Q010F
	PV23	TURN_OFF_PVLW			PV LWIR A&B_OFF	R	T10-2	48	CXX00	XX08	MM05Q012F
	PV24	SET_PVLW_ECAL	TO ON/OFF	T	PV LWIR A or B elex calibration, B# 1=ON, 0=OFF	SWD	T10-3	44	CXX13	A	MM05D011,12T
6,44	PV25	SET_PVLW_VCAL	TO X#XX	T	Set PV LWIR VCAL, 8bits, +1V=X#00 to -8V=X#FF; soft saturation occurs at D#173 = X#AD = -5.7V	SW	T10-3	45	na	na	na
	PV26	SET_PVLW_CSUB	TO ON/OFF	T	Active LWIR test only chrg subtraction to 1=ON, 0=OFF	SWD	T10-3	49	CXX13	3	MM05D005,06T
	PV27	SET_PVLW_ITWK_V	TO X#XX	C	Set PV LWIR ITWK, 8bits, -2.5V=X#00 to -4.5V=X#FF	SW	T10-3	46	na	na	na
	PV28	SET_PVLW_VDET_V	TO X#XX	C	Set PV LWIR VDET, 8 bits, -8V=X#00 to 0V=X#FF	SW	T10-3	47	na	na	na
	PV29	ENABLE_PV_ECAL		A	Global all PV FPA A&B enable elex cal & chrg subtraction	R	T10-2	49	CXX00	5C89	MM05Q000,07F
	PV30	DISABLE_PV_ECAL			Global all PV FPA A&B disable elex cal & chrg subtraction	R	T10-2	50	CXX00	XX03	MM05Q003F
	PV31	SET_PV_MEM	TO ROM/RAM	T	Set PV active side MEM to ROM/RAM, B# 0=ROM, 1=RAM	SWD	T10-3	50	CXX13	8	MM05D000,02T
14	PV32	SET_PVVIS_NSTEP	TO D#XX	T	Sets VIS FPA step cycles of chrg injection, D#XX ≤ 40, no tlmy	SW	T10-3	67	na	na	na
14	PV33	SET_PVNIR_NSTEP	TO D#XX	T	Sets NIR FPA step cycles of chrg injection, D#XX ≤ 40, no tlmy	SW	T10-3	68	na	na	na
14	PV34	SET_PVSM_NSTEP	TO D#XX	T	Sets SM FPA step cycles of chrg injection, D#XX ≤ 40, no tlmy	SW	T10-3	69	na	na	na
14	PV35	SET_PVLW_NSTEP	TO D#XX	T	Sets LW FPA step cycles of chrg injection, D#XX ≤ 10, no tlmy	SW	T10-3	70	na	na	na
	RC01	TURN_ON_RCLWTLM			Turns ON RC LWIR ckt pwr with only temp tlmy info, no htr	R	T10-2	51	CXX00	XX41	MM05Q882F
	RC02	TURN_ON_RCLWHTR		C	Turns ON RC LWIR FPA htr, separate cmd for temp set point	R	T10-2	52	CXX00	XX4D	MM05Q884F
	RC03	TURN_OFF_RCLWHTR			Turns OFF RC LWIR FPA htr, temp tlmy still on	R	T10-2	53	CXX00	XX44	MM05Q885F
	RC04	TURN_OFF_RCLWTLM			Turns OFF all RC LWIR FPA pwr (htr & tlmy)	R	T10-2	54	CXX00	XX42	MM05Q883F
	RC05	TURN_ON_RCSMTLM			Turns ON RC SMIR ckt pwr with only temp tlmy info, no htr	R	T10-2	55	CXX00	XX3D	MM05Q878F
	RC06	TURN_ON_RCSMHTR		C	Turns ON RC SMIR FPA htr, separate cmd for temp set point	R	T10-2	56	CXX00	XX4C	MM05Q880F
	RC07	TURN_OFF_RCSMHTR			Turns OFF RC SMIR FPA htr, temp tlmy still on	R	T10-2	57	CXX00	XX40	MM05Q881F
	RC08	TURN_OFF_RCSMTLM			Turns OFF all RC SMIR FPA pwr (htr & tlmy)	R	T10-2	58	CXX00	XX3E	MM05Q879F
43	RC09	SET_RC_CFPA_TEMP	TO T1/T2/T3	A	Sets LWIR/SMIR CFPA htrs to T1=83K/T2=85K/T3=88K HW setpoint	RRR	T10-2	89 90 91	CXX00 CXX00 CXX00	XX37 XX3B XX67	MM05Q886F MM05Q887F MM05Q888F
	RC10	TURN_ON_RCCSTLM			Turns ON RC coldstage pwr with only temp tlmy, no OG htr	R	T10-2	59	CXX00	XX2E	MM05Q874F
	RC11	TURN_ON_RCCSHTR		C	Turns ON RC coldstage OG htr with T=318K fixed HW point	R	T10-2	60	CXX00	XX35	MM05Q876F
	RC12	TURN_OFF_RCCSHTR			Turns OFF RC coldstage OG htr; temp tlmy still on	R	T10-2	61	CXX00	XX36	MM05Q877F
	RC13	TURN_OFF_RCCSTLM			Turns OFF all RC coldstage pwr (OG & tlmy)	R	T10-2	62	CXX00	XX34	MM05Q875F
	RC14	TURN_ON_RCISTLM			Turns ON RC interstage pwr with only temp tlmy, no OG htr	R	T10-2	63	CXX00	XX24	MM05Q870F
	RC15	TURN_ON_RCISHTR		C	Turns ON RC interstage OG htr with T=318K fixed HW point	R	T10-2	64	CXX00	XX31	MM05Q872F
	RC16	TURN_OFF_RCISHTR			Turns OFF RC interstage OG htr; temp tlmy still on	R	T10-2	65	CXX00	XX32	MM05Q873F
	RC17	TURN_OFF_RCISTLM			Turns OFF all RC interstage pwr (OG & tlmy)	R	T10-2	66	CXX00	XX30	MM05Q871F
	RC18	TURN_ON_RCOSTLM			Turns ON RC outerstage pwr with only temp tlmy, no OG htr	R	T10-2	67	CXX00	XX45	MM05Q866F
	RC19	TURN_ON_RCOSHTR		C	Turns ON RC outerstage OG htr with T=318K fixed HW point	R	T10-2	68	CXX00	XX39	MM05Q868F
	RC20	TURN_OFF_RCOSHTR			Turns OFF RC outerstage OG htr; temp tlmy still on	R	T10-2	69	CXX00	XX3A	MM05Q869F
	RC21	TURN_OFF_RCOSTLM			Turns OFF all RC outerstage pwr (OG & tlmy)	R	T10-2	70	CXX00	XX38	MM05Q867F
44	SA01	TURN_ON_SAA		H	Scan Assy A_ON, B_OFF	RD	T10-2	92	CXX00	199C	MM05Q701,04F

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	SA02	TURN_ON_SAB		H	Scan Assy B_ON, A_OFF	RD	T10-2	93	CXX00	1A91	MM05Q702,03F
	SA03	TURN_ON_SA_AB		H	Scan Assy A&B_ON	RD	T10-2	94	CXX00	1A99	MM05Q701,02F
	SA04	TURN_OFF_SA			Scan Assy A&B_OFF	RD	T10-2	95	CXX00	1C91	MM05Q703,04F
	SA05	SET_SA_HIGAIN			Sets Scan Assy A to high gain (normal)	R	T10-2	71	CXX00	XX1D	MM05Q705F
	SA06	SET_SA_LOGAIN			Sets Scan Assy A to low gain (normal selection is high gain)	R	T10-2	72	CXX00	XX1E	MM05Q706F
	SA07	SET_SB_HIGAIN			Sets Scan Assy B to high gain (normal)	R	T10-2	73	CXX00	XX60	MM05Q707F
	SA08	SET_SB_LOGAIN			Sets Scan Assy B to low gain (normal selection is high gain)	R	T10-2	74	CXX00	XX61	MM05Q708F
	SM01	TURN_ON_SMA			SDSM A_ON, B_OFF	R	T10-2	75	CXX00	XX12	MM05Q570F
	SM02	TURN_ON_SMB			SDSM B_ON, A_OFF	R	T10-2	76	CXX00	XX20	MM05Q571F
	SM03	TURN_OFF_SM			SDSM A&B_OFF	R	T10-2	77	CXX00	XX21	MM05Q572F
9,30	SM04	SET_SM _FULL_CAL	WITH SCANS D#XXX		Sets SDSM full cal of SD-DCR-SUN with 8-bit D#XXX scans (1-255 valid range); sun window~81 scans	SW	T10-8	na	na	na	na
9,30	SM05	SET_SM _SD_CAL	WITH SCANS D#XXX		Sets SDSM cal SD-DCR with 8-bit D#XXX scans (1-255 valid range); sun window~81 scans	SW	T10-8	na	na	na	na
9,30	SM06	SET_SM _SUN_CAL	WITH SCANS D#XXX		Sets SDSM cal Sun-DCR with 8-bit D#XXX scans (1-255 valid range); sun window~81 scans	SW	T10-8	na	na	na	na
10,46	SM07	STEP_SM_MIR	BY D#XX FORWARD/BACKWARD	A	Step SDSM mirror D#XX steps (95 MAX) Forward/Backward (=mtr CW/CCW= step increas/decrease), ~3.75°/step	SW	T10-6	na	na	na	na
	SM08	HALT_SM_MIR_MTR			Halt stepping SM mirror motor	SW	T10-7	na	na	na	na
	SR01	TURN_ON_SRA			SRCA A_ON, B_OFF	R	T10-2	78	CXX00	XX2B	MM05Q600F
	SR02	TURN_ON_SRB			SRCA B_ON, A_OFF	R	T10-2	79	CXX00	XX23	MM05Q601F
	SR03	TURN_OFF_SR			SRCA A&B_OFF	R	T10-2	80	CXX00	XX2F	MM05Q602F
13	SR04	SET_SR_SIPD_HTR	TO ON/OFF		Turns SRCA SIS RAD SIPD Htr ON/OFF = 1/0	SW	T10-3	71	CXX01	Note 9	na
16	SR05	SET_SR_L10WX3	TO B#ABCD (4 items)	A	Set initial 3x10W lamps to B#1/0 ea ABCD from lamps 1,2,3,4	SW	T10-3	18	CXX01	Note 9	na
16	SR06	SET_SR_L10WX2	TO B#ABCD (4 items)	A	Set initial 2x10W lamps to B#1/0 ea ABCD from lamps 1,2,3,4	SW	T10-3	19	CXX01	Note 9	na
16	SR07	SET_SR_L10WX1	TO B#ABCD (4 items)	A	Set initial 1x10W lamps to B#1/0 ea ABCD from lamps 1,2,3,4	SW	T10-3	20	CXX01	Note 9	na
16	SR08	SET_SR_L1WX1	TO B#AB (2 items)	A	Set initial 1x1W lamps to B#1/0 ea AB from lamps 5,6	SW	T10-3	21	CXX01	Note 9	na
13	SR09	SET_SR_SIS_FB	TO RADIANCE/CURRENT	A	Set SRCA SIS Feedback control to Radiance/Current = 1/0	SW	T10-3	72	CXX01	Note 9	na
13	SR10	SET_SR_LOV_SHDN	TO ENABLE/DISABLE	A	Set SRCA Lamp OverVoltage Shutdown to Enable/Disable=0/1	SW	T10-3	73	CXX01	Note 9	na
13,44	SR11	SET_SR_LAMPLEVEL	TO HIGH/LOW	A	Set SRCA Lamp Level to High/Low = 1/0; High is normal; Low might be used near end of life	SW	T10-3	74	CXX01	Note 9	na
13,35	SR12	SET_SR_LAMPS	TO OFF/W1/W10/W20/W30	C	Set SRCA lamps to OFF/W1/W10/W20/W30 = B# 000/001/010 /011/100. SR05-SR08 selects lamp set. Flt SW auto toggles OFF for sequential SR12 use (see T10-22 logic)	SW	T10-3	75	CXX01	Note 9	na
29,36	SR13	SET_SR_MTR_GRP	WITH WH D#X, SL D#X, GR D#XXXXX	A	Set SRCA 3 mtr config - - Filter Wheel positions: #1=step 0=ND Filter, #2=step 20=Open (tiny Home), #3=step 40=Order Filt#1, #4=step 60=Order Flt#2, #5=step 80=Order Flr#3, #6=step 100 =Beamcombiner.	SW	T10-11	na	CXX01	Note 9	na
29,36 40	SR13	*Continued*			Slit mtr positions: #1=step 0=Along Track Reticle, #2=step 24=Along Scan Reticle (tiny Home), #3=step 48=Slit Reticle (hard stops just before step 0 & beyond step 48; Grating mtr steps to D#XXXXX (0-61199); GR step increase/decrease = mtr CW/CCW.						
	SR14	STEP_SR_WHEEL	BY D#XXX FORWARD/BACKWARD	A	Step SRCA Filter wheel D#XXX steps (120 max) Forward/ Backward (=mtr CW/CCW=step increase/decrease;	SW	T10-6	na	CXX01	Note 9	na
23	SR15	SR_SPARE		A	Was HALT_SR_WHL_MTR	SW	T10-7	na	CXX01	Note 9	na

TABLE 10-25A. MODIS COMMAND LIST

Sort by Subsystem - - See Notes - - General User Interest extends through Column 4 - - Shaded area indicates S/C pt-pt cmds to MODIS. *4/97*

PF Chg#	1 Subsys	2 OASIS Command Name	3 Qualifier or Value	4a Safe/ Use	4b Remarks	5 Cmd Type	6 Op Code Table	7 R/P ID#	8 CP HW Address	9 CP HW Data Loc	10 HW Unique ID
	SR16	STEP_SR_SLIT	BY D#XX FORWARD/BACKWARD	A	Step SRCA entrance/exit slit D#XX steps (48 max) Forward/backward (=mtr Cw/CCW=step increase/decrease)	SW	T10-6	na	CXX01	Note 9	na
23	SR17	SR_SPARE			Was HALT_SR_SLT_MTR	SW	T10-7	na	CXX01	Note 9	na
38	SR18	STEP_SR_GRT	BY D#XXXXX FORWARD/BACKWARD	A	Step SRCA grating/mirror D#XXXXX steps (61,199 max) Forward/Backward (= mtr CW/CCW=step increas/decrease)	SW	T10-6	na	CXX01	Note 9	na
	SR19	STEP_SR_GR_BSS	WITH BURST D#XXX, STEPS D#XX, SCANS D#XXX, FORWARD/ BACKWARD	A	Burst step SRCA grating: D#XXX bursts (255 max), D#XX steps (63 max) Forward/Backward, D#XXX scan pause (255 max)	SW	T10-12	na	CXX01	Note 9	na
	SR20	HALT_SR_GRT_MTR			Halt stepping SRCA grating motor	SW	T10-7	na	CXX01	Note 9	na
13	SR21	SET_SR_IR_SRC	TO ON/OFF		Turns SRCA IR source ON/OFF = 1/0	SW	T10-3	76	CXX01	Note 9	na
44	TG01	TURN_ON_TGA			TG A_ON, B_OFF; should be early in command sequence to assure proper scan mirror ops & prevent PS shutdown if switched with heavy load	R	T10-2	81	CXX00	XX4F	MM05Q900F
44	TG02	TURN_ON_TGB			TG B_ON, A_OFF; should be early in command sequence to assure proper scan mirror ops & prevent PS shutdown if switched with heavy load	R	T10-2	82	CXX00	XX53	MM05Q901F
	TG03	TURN_OFF_TG			TG A&B_OFF	R	T10-2	83	CXX00	XX57	MM05Q902F
	TG04	RESET_TG			Active TG Reset=0, No Set cmd, SW steps 1, 0 for chg	SWD	T10-3	03	CXX13	5	MM05D907,11T
	217	***<--Total w/o CP22 & CP23 & Spares***									

NOTES: (PF Change History from EM follows Notes.)

1. Column 1 is Subsystem 2-alpha code, defined by Table 10 or Figure 11, with sequential subsystem cmd identification for short form reference.

2. Column 2 is OASIS Command Name (16 character limit). CSTOL command consists of 1) directive or verb, then space, 2) object or external element, not shown, is "MOD", then space, 3) attribute or noun with underscores if needed, then space, and 4) if present, qualifier or value (Column 3).

3. Column 3 is command qualifier and/or value. For qualifiers of slash form X/X/X, select only one. All items must be specified for comma separated qualifiers. Oasis values may be binary = B#X, decimal = D#X or hexidecimal = X#X. Multiple bit items partitioned as individual bit values, use ABCD versus XXXX form.

4. Column 4a contains Safe/Use codes H = Hazard, C = Constraint, A = Advisory (significant extension of Col 4b) & T = Test. H, C, A descriptions appear in Table 10-25B. Column 4b provides cmd logic/parameter definitions & remarks. A few T codes are primarily I&T aides, but may be used on-orbit.

5. Column 5 is Cmd Type, all via 1553 bus except RS (RS = relay cmd direct by S/C); R = relay cmd; RD = dual relay cmd; SW = software, high level, or macro cmd; SWD = SW controlled HW digital command (has a related Unique ID).

6. Column 6 identifies 1553 bus structure operation code by table number. Column 7 identifies Relay # for Op Code T10-2, or Parameter # for Op Code T10-3. Parameter cmd #s are summarized in Table 10-22 for Flt SW use. Text related to Op Code tables generally provide more detail to Col 4b Remarks.

7. Columns 8 & 9 contain CP hardware hexidecimal address/data locations (MSB left, LSB right). SWD cmds are controlled by a single bit of a 16-bit word (see 10.5.2).

TABLE 10-25A. MODIS COMMAND LIST

Sort by Subsystem - - See Notes - - General User Interest extends through Column 4 - - Shaded area indicates S/C pt-pt cmds to MODIS. *4/97*

PF Chg#	1 Subsys	2 OASIS Command Name	3 Qualifier or Value	4a Safe/ Use	4b Remarks	5 Cmd Type	6 Op Code Table	7 R/P ID#	8 CP HW Address	9 CP HW Data Loc	10 HW Unique ID

8. Column 10 is hardware Unique ID for the listed function. SW items do not have an unique ID.

9. See Appendix E for PL3095-N02646A MODIS Software Commands for On Board Calibrator Control (addresses internal CP-CE bi-directional serial link protocol for commands & telemetry that flow across it). These cmds are DCE type in Column 5.

T10-25A PF Change History. Left column Chg #s relate to these #s. [#s] are general notes.

[1] 8/10/95 34 Col4 chgs to reduce character count. No functional chgs.
2. 8/10/95 Col2 chged CP_SC_SPARE to SET_CP_SC_SPARE (C.Wilda old rqst).
3. 10/8/95 Chg FO06 RESET_FO to FO_SPARE to eliminate potential SPF. Gets automatically reset by FR ea scan.
4. 11/4 /95 Chg FR28 SET_FR_PC_DCR_TH & FR30 SET_FR_PV_DCR_TH to FR_SPAREs.
[5] 11/4/95 Delete unused Column 5, then renumber columns.
6. 11/4/95 Chg ECAL to VCAL 4pl for ea PV FPA, e.g., PV05 SET_PVVIS_ECAL_V to SET_PVVIS_VCAL, also PV11, PV17, PV25
7. 11/24/95 Chg Remarks on FR17-FR21 (e.g.SET_FR_SD_DELAY) to note unit delay=6.66µs (not 3.33µs) and range=0-50 vs 100 units.
[8] 12/2/95 Chg Footer E151840 to 151840.
9. 1/5/96 SM04, 05, 06: increase scan count to D#XXX (1 to 128) scans from D#XX (1 to 64) scans. Chg Col 8&9 to na.
10. 1/5/96 SM07: Add "~3.75°/srep" to Remarks Column
[11] 1/5/96 Chg Column 4 title to Remarks from General Remarks.
12. 2/27/96 Add new FR31 SET_FR_ENC_DELTA to 0 to ±8191 to facilitate testing.
13. 2/27/96 Revise SR04 to SET_SR_SIPD_HTR TO ON/OFF as part of SR04 decomposition from 6 items to indivdual cmds. Related chgs are SR09 to SET_SR_SIS_FB to Radiance/Current, SR10 to SET_SR_LOV_SHDN to Enable/Disable, SR11 to SET_SR_LAMPLEVEL to High/Low, SR12 to SET_SR_LAMPS to Off/1W/10W/20W/30W. Note SR12 establishes lamps sets to use previousl defined by SR09-SR12.
14. 2/28/96 Add 4 new NSTEP cmds to facilitate test ops: SET_PVVIS_NSTEP, SET_PVNIR_NSTEP, SET_PVSM_NSTEP, SET_PVLW_NSTEP.
15. 2/29/96 Add 3 new FR cmds to facilitate test ops: SET_FR_BBRADTAB, SET_FR_OFFSETTAB,SET_FR_GAINTAB, TEST_FR_BBRAD with X#XX, TEST_FR_PVOFFSET with X#XX, TEST_FR_PCOFFSET with X#XXXX, TEST_FR_PVGAIN with X#XX,.
16. 3/3/96 slight name chg to SR05 to SET_SR_L10WX3 from SET_SR_3L10W, SR06 to SET_SR_L10WX2 from SET_SR_2L10W, SR07 to SET_SR_L10WX1 from SET_SR_1L10W, SR08 to SET_SR_L1WX1 from SET_SR_1L1W.
[17] 3/11/96 Parse T10-25 into T10-25A & T10-25B and insert T10-25A new Col 4a H=Hazard, C=Constraint, A=Advisory, T=Test. Add code defintions to Note 4. Since these codes are evident in Col 4a, the effected items are not highlighted in PF Chg# col. Also, revise Col 7 to be R/P ID# & add codes.
18. 3/11/96 Chg to FR_Spares: FR14 SET_FR_MEM_APID, FR15 SET_FR_MEM_QLK & FR16 RESET_FR_MEM_QLK since Memory Pks will be redefined to be additinal Eng Pkts.
19. 3/11/96 Chg to Spares: CP18 CP_SPARE & FR25 FR_Spare; no longer needed due to revised Flt SW upload process.
20. 3/11/96 Chg FR04 to TOGGLE_FR_INT02 from TEST_FR_SELF. Flt SW test aide.
21. 3/11/96 minor name chg to qualifier: to NORMAL/TEST from TEST/OPERATE; same logic.
22. 3/13/96 Clarify BB04 Remarks to be D#DN with typical values. (Later, when typical 5th order poly Eqs are available, qualifier could be expressed in EUs.
23. 3/15/96 Chg SR15 & SR17 Halt WHL_MTR & SLT_MTR to SR_SPARE. Step rate & short range of these mtrs precludes practical use of cmd.
24. 3/15/96 Add 3 new test cmds SET_FR_PCDCRDBG, SET_FR_PCDCRPRE TO ON/OFF, & SET_FR_PCDCRPOST.
25. 3/16/96 Add 4 new test cmds SET_FR_PVGN1C, SET_FR_PVOS1C, SET_FR_PCPREOS1C, & SET_FR_PCPSTOS1C. Sets individual PV gain/offset and PC preamp/postamp offset.

TABLE 10-25A. MODIS COMMAND LIST

Sort by Subsystem - - See Notes - - General User Interest extends through Column 4 - - Shaded area indicates S/C pt-pt cmds to MODIS. *4/97*

PF Chg#	1 Subsys	2 OASIS Command Name	3 Qualifier or Value	4a Safe/ Use	4b Remarks	5 Cmd Type	6 Op Code Table	7 R/P ID#	8 CP HW Address	9 CP HW Data Loc	10 HW Unique ID

26. 3/16/96 Add 2 new mtr cmds GET_CP_MTR_HOME WITH MTR D#X, DIR B#X & SET_CP_MTR_SWPOS WITH MTR D#X, STEP X#XXXX.
27. 3/25/96 Add 2 new SW load cmds, CP26 SET_CP_LOG_STATE & FR46 SET_FR_LOG_STATE.
28. 4/6/96 Chg FR26 name to SET_FR_PKT_TYPE from SET_FR_SCI_PKT to be compatible with other new cmds/tlmy.
29. 4/24/96 added SR13 parametric details to Remarks Column.
30. 4/24/96 Clarified valid range of 8-bit D#XXX range
31. 4/24/96 marked CP15 as a chg to prior Qualifier from WITH ADDR X#XXXXX to WITH ASTATE X#X (did not get Chg# at time of update). Also, created a a similar cmd for FR15 by revising it from Chg#18 FR_SPARE to SET_FR_RESTART WITH ASTATE X#X.
32. 5/9/96 Correct name on CP from SET_CP_SAFE_MODE to SET_SAFE_MODE.

----------Chgs since 5/8/96 151840 Initial Release----------

33. 6/17/96 Clarify limits as DN=98-3908 (T=317K-270K inverse function) & add fourth digit to selectable value.
34. 8/12/96 Correct Col 4b direction remarks for DR14 and further clarify direction remarks in DR14,15,16 by adding close/open.
35. 8/12/96 Correct Col 3 syntax on FR 35,36,37,38 & SR12 to match OASIS rqmts.
36. 8/12/96 Add mtr position #s per T10-11 to SR13 Col 4b to match syntax variables of Col 3.
37. 8/15/9Chg folowing cmds to spares as listed: CP21 was SET_CP_PK_PWR, FR43 was SET_FR_PCDCRDBG, FR44 was SET_FR_PCDCRPOST, & FR45 was SET_FR_PCDCRPRE.
38. 8/19/96 On SR18, correct CW/CCW direction on GR mtr.
39. 9/16/96 Remove Hazard designation on DR03 OPEN_DR_UL_LOCK.
40. 9/26/96 In SR13 Remarks, interchg Along Track Reticle and Slit Reticle position# & step #s.
41. 10/17/96 Re-activate FR16 as SET_FR_SCIABNORM TO ABNORM/NORM for gnd flag of known abnormalities other than MODIS.
42. 12/9/96 Changed door unlatch and failafe parrafin actuation times to 3 minutes except NAD & SDD unlatch times to be 6 minutes.
43. 12/9/96 Typo correction to RC09: T1=83K, not 82K.
44. 4/97 Multiple EO1122D Incorporations for Rev B. See EO1122D (released 970305) for details.
45. 4/97 Direct Rev B chg to revise last part of Remarks on BB04.
46. 4/97 Direct Rev B chg to revise SM07 max step to be 95.
47. 5/97 Direct Rev B chg to add max step counts.

TABLE 10-25B. MODIS COMMAND HAZARDS, CONSTRAINTS & ADVISORIES

Sort by Col 4a, then Col 1 - - See Notes - - Shaded area indicates S/C pt-pt cmds to MODIS. ***5/97***

PF Chg#	1 Subsys	2 OASIS Command Name	3 Qualifier or Value	4a Safe/ Use	4b Description of Hazard, Constraint or Advisory Cited in Table 10-25A
	CP05	DISABLE_CP_IMOK		H	Disabled state creates on-orbit risk for MODIS not to go Safe by missing SCC IMOK/5sec (1 of 3 Safe cmd paths).
	CP07	SET_CP_OPER_MODE	TO SRV/SAF/STBY/OG/SCI	H	Modes SRV/SAF/STBY/OG/SCI cmd sequences contain door/scan mirror test motion hazards & on-orbit door motion HW hazard if door unlatch has not been activated.
	CP08	PERFORM_CP_MACRO	WITH NUMBER D#XX	H	Macro cmd sequences might contain door/scan mirror test motion hazards & on-orbit door motion HW hazard if door unlatch has not been activated. Each will have to be idividually idetified.
	CP16	ENABLE_CPA_EPWRT		H	Verfiy intent & organization of uploads. Mismanagment could create major HW hazard with loss of operational control.
	CP17	ENABLE_CPB_EPWRT		H	Verfiy intent & organization of uploads. Mismanagment could create major HW hazard with loss of operational control.
	DR04	SET_DR_SVD_UL	TO ON/OFF	H	Premature door unlatch can create a HW integrity hazard during S/C preship or prelaunch activities.
	DR05	SET_DR_NAD_UL	TO ON/OFF	H	Premature door unlatch can create a HW integrity hazard during S/C preship or prelaunch activities.
	DR06	SET_DR_SDD_UL	TO ON/OFF	H	Premature door unlatch can create a HW integrity hazard during S/C preship or prelaunch activities.
	DR09	MOVE_DR_SVD	TO CLOSED/OG/OPEN	H	Can create a test motion hazard & test/on-orbit HW hazard if door unlatch has not been activated.
	DR10	MOVE_DR_NAD	TO CLOSED/OPEN	H	Can create a test motion hazard & test/on-orbit HW hazard if door unlatch has not been activated.
5	DR13	MOVE_DR_SDD	TO CLOSED/SDD OPEN/SCREEN OPEN	H,C	Can create a test motion hazard & test/on-orbit HW hazard if door unlatch has not been activated. SDD thermal constraint is to wait 5 minutes for further SDD ops if the SDD has been run continuoulsy for one minute.
	DR14	STEP_DR_SVD	BY D#XXXX IN/OUT	H	Can create a test motion hazard & test/on-orbit HW hazard if door unlatch has not been activated.
	DR15	STEP_DR_NAD	BY D#XXXX IN/OUT	H	Can create a test motion hazard & test/on-orbit HW hazard if door unlatch has not been activated.
5	DR16	STEP_DR_SDD	BY D#XXXX IN/OUT	H,C	Can create a test motion hazard & test/on-orbit HW hazard if door unlatch has not been activated. SDD thermal constraint is to wait 5 minutes for further SDD ops if the SDD has been run continuoulsy for one minute.
	DR22	ENABLE_DR_FS		H	Can result in irreversable on-orbit HW hazard as 1st of 3 or 4 sequential commom FS cmds to force door(s) open.
	DR23	CLOSE_DR_FS_SW2		H	Can result in irreversable on-orbit HW hazard as 2nd of 3 or 4 sequential common FS cmds to force door(s) open.
	DR24	FIRE_DR_SVD_FS		H	Can result in irreversable on-orbit HW hazard as final of 3 sequential NAD FS cmds to force door open.
	DR25	FIRE_DR_NAD_FS		H	Can result in irreversable on-orbit HW hazard as final of 3 sequential SVD FS cmds to force door open.
	DR26	TURN_ON_DR_SDDFS		H	Can result in irreversable on-orbit HW hazard as final of 3 sequential SVD FS cmds to force door open.
	DR27	SET_DR_SDD_FS	TO ON/OFF	H	Can result in irreversable on-orbit HW hazard as final of 4 sequential SDS FS cmds to force screen closed & door open.
	SA01	TURN_ON_SAA		H	Can create test motion hazard. Also, verify constraint that only one side is normally On. SAA & SAB can both be ON.
	SA02	TURN_ON_SAB		H	Can create test motion hazard. Also, verify constraint that only one side is normally On. SAA & SAB can both be ON.
	SA03	TURN_ON_SA_AB		H	Can create test motion hazard. Also, verify constraint that only one side is normally On. SAA & SAB can both be ON.
	BB01	TURN_ON_BBA		C	Should be preceded by CE01 or CE02, otherwise heated BB has no bang-bang CP control & is ON at full current.
	BB02	TURN_ON_BBB		C	Should be preceded by CE01 or CE02, otherwise heated BB has no bang-bang CP control & is ON at full current.
	CP15	SET_CP_RESTART	WITH ASTATE X#X	C	Verfiy proper CP address state otherwise new RAM load could result in significant amount of nonfunctional subsystems.
	FR07	SET_FR_RATE	TO DAY/NIGHT	C	Concurrence of FOT is required for any data rate chg, otherwise S/C data resources may be exceeded.
	FR08	SET_FR_SCI_APID	TO D#XXX	C	Concurrence of FOT & EDOS is required for any APID chg.
	FR11	SET_FR_ENG_APID	TO D#XXX	C	Concurrence of FOT & EDOS is required for any APID chg.
	FR15	SET_FR_RESTART	WITH ASTATE X#X	C	Verfiy proper CP address state otherwise new RAM load could result in significant amount of nonfunctional subsystems.
	FR23	ENABLE_FRA_EPWRT		C	Verfiy intent & organization of uploads. Mismanagment could result in cumbersome recovery process.
	FR24	ENABLE_FRB_EPWRT		C	Verfiy intent & organization of uploads. Mismanagment could result in cumbersome recovery process.
	PC01	TURN_ON_PCLWA		C	Verify constraint that only one side is normally On. PCLWA & PCLWB can both simultaneously be ON.
	PC02	TURN_ON_PCLWB		C	Verify constraint that only one side is normally On. PCLWA & PCLWB can both simultaneously be ON.
	PC03	TURN_ON_PCLW_AB		C	Verify constraint that only one side is normally On. PCLWA & PCLWB can both simultaneously be ON.
	PS01	TURN_ON_PS1		C	Verify constraint that only one side is normally On. PS1 & PS2 can both simultaneously be ON.

TABLE 10-25B. MODIS COMMAND HAZARDS, CONSTRAINTS & ADVISORIES

Sort by Col 4a, then Col 1 -- See Notes -- Shaded area indicates S/C pt-pt cmds to MODIS. ***5/97***

PF Chg#	1 Subsys	2 OASIS Command Name	3 Qualifier or Value	4a Safe/ Use	4b Description of Hazard, Constraint or Advisory Cited in Table 10-25A
	PS02	TURN_ON_PS2		C	Verify constraint that only one side is normally On. PS1 & PS2 can both simultaneously be ON.
	PS03	TURN_ON_PS1_PS2		C	Verify constraint that only one side is normally On. PS1 & PS2 can both simultaneously be ON.
	PV06	SET_PVVIS_ITWK_V	TO X#XX	C	Verify intent to chg FPA bias either for test or on-orbit tweak. Proper bias is needed for normal operation.
	PV12	SET_PVNIR_ITWK_V	TO X#XX	C	Verify intent to chg FPA bias either for test or on-orbit tweak. Proper bias is needed for normal operation.
	PV19	SET_PVSM_ITWK_V	TO X#XX	C	Verify intent to chg FPA bias either for test or on-orbit tweak. Proper bias is needed for normal operation.
	PV20	SET_PVSM_VDET_V	TO X#XX	C	Verify intent to chg FPA bias either for test or on-orbit tweak. Proper bias is needed for normal operation.
	PV27	SET_PVLW_ITWK_V	TO X#XX	C	Verify intent to chg FPA bias either for test or on-orbit tweak. Proper bias is needed for normal operation.
	PV28	SET_PVLW_VDET_V	TO X#XX	C	Verify intent to chg FPA bias either for test or on-orbit tweak. Proper bias is needed for normal operation.
	RC02	TURN_ON_RCLWHTR		C	RC01 related tlmy must be turned On prior to RC02, otherwise there will be no heater function.
	RC06	TURN_ON_RCSMHTR		C	RC05 related tlmy must be turned On prior to RC06, otherwise there will be no heater function.
	RC11	TURN_ON_RCCSHTR		C	RC10 related tlmy must be turned On prior to RC11, otherwise there will be no heater function.
	RC15	TURN_ON_RCISHTR		C	RC14 related tlmy must be turned On prior to RC15, otherwise there will be no heater function.
	RC19	TURN_ON_RCOSHTR		C	RC18 related tlmy must be turned On prior to RC19, otherwise there will be no heater function.
5	SR12	SET_SR_LAMPS	TO OFF/1W/10W/20W/30W	C	Do not turn on lamps if lamp ring temperature exceeds 95°C. Constrain operating time to minimum needed to conserve lamp life. SW & HW logic rejects invalid lamp combos.
5	TG01	TURN_ON_TGA		C	TG A_ON, B_OFF; should be early in command sequence to assure proper scan mirror ops & prevent PS shutdown if switched with heavy load.
5	TG02	TURN_ON_TGB		C	TG B_ON, A_OFF; should be early in command sequence to assure proper scan mirror ops & prevent PS shutdown if switched with heavy load.
	BB04	SET_BB_HTR_TEMP	TO D#XXX	A	Max temp s/b ≤ 317K. Normal heated pt is 315K in TV, about 312K in ambient. Coarse cmd data may not yield exact desired pt, but tlmy s/b uniform. TK-vs-DN has inverse relation, e.g., 300K=D#692DN, 313K=D#204DN & 315K=D#151DN.
	CP13	RESET_CP_UPLD		A	Places CP in upload mode with minimum Flt SW C&T resources. No tlmy is generated & only cmds related to memory load, dump & restart are processed, after the load is complete.
	CP24	GET_CP_MTR_HOME	WITH MTR D#X, DIR B#X	A	Absolute mtr positions are SW step count from Home, which can be at limit or a midpt of range. If any Reset occurs while mtr is away from Home & position is unknown, CP24 is used for recovery. For OBCs, best direction is needed, doors don't
	CP25	SET_CP_MTR_SWPOS	WITH MTR D#X, STEP X#XXXX	A	If there's been a Reset, and known position doesn't match tlmy, CP SW step count can be reset by CP25. See 10.8.4, 10.8.19b & 10.8.19C.
	PS06	ENABLE_PS12SHDN		A	This should normally be enabled.
	PS08	ENABLE_PS1_SVHTR		A	Both survival heaters are normaly enabled.
	PS09	ENABLE_PS2_SVHTR		A	Both survival heaters are normaly enabled.
	PV29	ENABLE_PV_ECAL		A	Normally enabled to allow all PV FPA sides to invoke ecal or chrg subtraction process. If problems, allows global PV disable.
	RC09	SET_RC_CFPA_TEMP	TO T1/T2/T3	A	Sets LWIR/SMIR CFPA htrs to T1=82K/T2=85K/T3=88K HW setpoint. Normally, only one CFPA htr is on at a time.
	SM07	STEP_SM_MIR	BY D#XX FORWARD/ BACKWARD	A	Individual step cmds should not be attempted if higher level combined mtr stepping is in process.
	SR05	SET_SR_L10Wx3	TO B#ABCD (4 items)	A	10W lamp IDs are 1,2,3,4 & 1Ws are 5&6. 1,2,3 rotate as 10W,20W,30W sets. 4&6 are small use/spares. Log lamp hrs.
	SR06	SET_SR_L10WX2	TO B#ABCD (4 items)	A	10W lamp IDs are 1,2,3,4 & 1Ws are 5&6. 1,2,3 rotate as 10W,20W,30W sets. 4&6 are small use/spares. Log lamp hrs.
	SR07	SET_SR_L10WX1	TO B#ABCD (4 items)	A	10W lamp IDs are 1,2,3,4 & 1Ws are 5&6. 1,2,3 rotate as 10W,20W,30W sets. 4&6 are small use/spares. Log lamp hrs.
	SR08	SET_SR_L1WX1	TO B#AB (2 items)	A	10W lamp IDs are 1,2,3,4 & 1Ws are 5&6. 1,2,3 rotate as 10W,20W,30W sets. 4&6 are small use/spares. Log lamp hrs.
	SR09	SET_SR_SIS_FB	TO RADIANCE/ CURRENT	A	SRCA SIS lamp output has feedback control by SiPd Radiance or by lamp Current. Radiance control is normal selection.
	SR10	SET_SR_LOV_SHDN	TO ENABLE/DISABLE	A	Set SRCA Lamp OverVoltage Shutdown to Enable/Disable=1/0
5	SR11	SET_SR_LAMPLEVEL	TO HIGH/LOW	A	SRCA Lamp Levels have a High/Low selection; High is normal selection for beginning of life.

TABLE 10-25B. MODIS COMMAND HAZARDS, CONSTRAINTS & ADVISORIES

Sort by Col 4a, then Col 1 - - See Notes - - Shaded area indicates S/C pt-pt cmds to MODIS. ***5/97***

PF Chg#	1 Subsys	2 OASIS Command Name	3 Qualifier or Value	4a Safe/ Use	4b Description of Hazard, Constraint or Advisory Cited in Table 10-25A
	SR13	SET_SR_MTR_GRP	WITH WH D#X, SL D#X, GR D#XXXXX	A	Establishs a particular position for each SRCA mtr. Generally, only 1 of 3, mtrs would chg positions in sucessive test steps.
	SR14	STEP_SR_WHEEL	BY D#XXX FORWARD/BACKWARD	A	Individual step cmds should not be attempted if higher level combined mtr stepping is in process.
	SR16	STEP_SR_SLIT	BY D#XX FORWARD/BACKWARD	A	Individual step cmds should not be attempted if higher level combined mtr stepping is in process.
	SR18	STEP_SR_GRT	BY D#XXXXX FORWARD/BACKWARD	A	Individual step cmds should not be attempted if higher level combined mtr stepping is in process.
	SR19	STEP_SR_GR_BSS	WITH BURST D#XXX, STEPS D#XX FORWARD/ BACKWARD, SCANS D#XXX	A	Used after grating is in area to start collects. Sets periodic step interval, # of scan collects per pt, & total # of pts. Step interval should be subtracted from initial pt as the 1st step pt will occur before taking collects.
	FR04	TOGGLE_FR_INT02		T	
	FR17	SET_FR_SD_DELAY	TO D#XXX	T	Cmd will also result in tlmy word FR_CS_SCI_NORMAL chg from YES to NO
	FR18	SET_FR_SR_DELAY	TO D#XXX	T	Cmd will also result in tlmy word FR_CS_SCI_NORMAL chg from YES to NO
	FR19	SET_FR_BB_DELAY	TO D#XXX	T	Cmd will also result in tlmy word FR_CS_SCI_NORMAL chg from YES to NO
	FR20	SET_FR_SP_DELAY	TO D#XXX	T	Cmd will also result in tlmy word FR_CS_SCI_NORMAL chg from YES to NO
	FR21	SET_FR_EA_DELAY	TO D#XXX	T	Cmd will also result in tlmy word FR_CS_SCI_NORMAL chg from YES to NO
	FR26	SET_FR_PKT_TYPE	TO NORMAL/TEST	T	Cmd will also result in tlmy word FR_CS_SCI_NORMAL chg from YES to NO
	FR31	SET_FR_ENC_DELTA	TO 0, -8192,+8191	T	Cmd will also result in tlmy word FR_CS_SCI_NORMAL chg from YES to NO
	FR32	SET_FR_BBRADTAB	TO NORMAL/TEST	T	Cmd will also result in tlmy word FR_CS_SCI_NORMAL chg from YES to NO
	FR33	SET_FR_OFFSETTAB	TO NORMAL/TEST	T	Cmd will also result in tlmy word FR_CS_SCI_NORMAL chg from YES to NO
	FR34	SET_FR_GAINTAB	TO NORMAL/TEST	T	Cmd will also result in tlmy word FR_CS_SCI_NORMAL chg from YES to NO
	FR35	TEST_FR_BBRAD	WITH X#XXX	T	
	FR36	TEST_FR_PVOFFSET	WITH X#XX	T	
	FR37	TEST_FR_PCOFFSET	WITH X#XXXX	T	
	FR38	TEST_FR_PVGAIN	WITH X#XX	T	
	FR39	SET_FR_PVGN1C	WITH B D#XX, C D#XX, V X#XX	T	
	FR40	SET_FR_PVOS1C	WITH B D#XX, C D#XX, V X#XX	T	
	FR41	SET_FR_PCPREOS1C	WITH B D#XX, C D#XX, V X#XX	T	
	FR42	SET_FR_PCPSTOS1C	WITH B D#XX, C D#XX, V X#XX	T	
	PC05	TURN_ON_PC_ECAL		T	Cmd will also result in tlmy word FR_CS_SCI_NORMAL chg from YES to NO
	PV04	SET_PVVIS_ECAL	TO ON/OFF	T	Cmd will also result in tlmy word FR_CS_SCI_NORMAL chg from YES to NO
	PV05	SET_PVVIS_VCAL	TO X#XX	T	
	PV10	SET_PVNIR_ECAL	TO ON/OFF	T	Cmd will also result in tlmy word FR_CS_SCI_NORMAL chg from YES to NO
	PV11	SET_PVNIR_VCAL	TO X#XX	T	
	PV16	SET_PVSMIR_ECAL	TO ON/OFF	T	Cmd will also result in tlmy word FR_CS_SCI_NORMAL chg from YES to NO
	PV17	SET_PVSM_VCAL	TO X#XX	T	
	PV18	SET_PVSMIR_CSUB	TO ON/OFF	T	Cmd will also result in tlmy word FR_CS_SCI_NORMAL chg from YES to NO
	PV24	SET_PVLW_ECAL	TO ON/OFF	T	Cmd will also result in tlmy word FR_CS_SCI_NORMAL chg from YES to NO
	PV25	SET_PVLW_VCAL	TO X#XX	T	
	PV26	SET_PVLW_CSUB	TO ON/OFF	T	Cmd will also result in tlmy word FR_CS_SCI_NORMAL chg from YES to NO

TABLE 10-25B. MODIS COMMAND HAZARDS, CONSTRAINTS & ADVISORIES

Sort by Col 4a, then Col 1 -- See Notes -- Shaded area indicates S/C pt-pt cmds to MODIS. ***5/97***

PF Chg#	1 Subsys	2 OASIS Command Name	3 Qualifier or Value	4a Safe/ Use	4b Description of Hazard, Constraint or Advisory Cited In Table 10-25A
	PV31	SET_PV_MEM	TO ROM/RAM	T	Cmd will also result in tlmy word FR_CS_SCI_NORMAL chg from YES to NO
	PV32	SET_PVVIS_NSTEP	TO D#XX	T	
	PV33	SET_PVNIR_NSTEP	TO D#XX	T	
	PV34	SET_PVSM_NSTEP	TO D#XX	T	
	PV35	SET_PVLW_NSTEP	TO D#XX	T	
	102	*<--Total*			

4/6/96

NOTES: (No PF Chgs as Table 10-25B is new for initial release.)

1. This table provides a brief description of the H = Hazard, C = Constraints, & A = Advisory codes in Table 10-125A Commands List. No remarks are provided for T = Test Codes. The table serves as a vehicle to group these in one place.

2. Flt SW macros or ground test cmd sequence macros, that contain a hazardous cmd(s) should have a ground operational halt applied external to the macro/cmd sequence before it is executed. It is not necessary to place additional halts to the interior of the macro/cmd sequence prior to each cmd that poses a hazard.

T10-25B PF Change History

[1] 4/7/96 Changed table title to MODIS COMMAND HAZARDS, CONSTRAINTS & ADVISORIES from MODIS COMMAND LIST - BY TYPE.

2. 4/6/96 Chg FR26 name to SET_FR_PKT_TYPE from SET_FR_SCI_PKT to be compatible with other new cmds/tlmy.

----------Changes since 5/8/96 Initial Release----------

[3] 8/15/96 Delete FR43, FR44 & FR45. These became spares in T10-25A. See T10-25A for prior names.

[4] 9/16/96 Removed DR03 OPEN_DR_UL_LOCK from list.

5. 4/97 Multiple EO1122D Incorporations for Rev B. See EO1122D (released 970305) for details.

TABLE 10-26. MODIS CP INTERNAL CONTROLS

5/97

pf chg	1 Subsys	2 Name	3 (Not Used)	4 General Remarks	5 (Not Used)	6 Cntl Type	7 (Not Used)	8 HW Address	9 HW Data Loc	10 HW Unique ID
	Not of Interest to General End User - - See Notes at table bottom for description of columns.									
	Digital Internal Controls		*CP digital internal controls are similar to Table 10-25 SWD commands.*							
	CPIC	CMD_NAD_BIT_0		NAD door motor control		DIC		4XX02	0	MM05D803T
	CPIC	CMD_NAD_BIT_1		NAD door motor control		DIC		4XX02	1	MM05D804T
	CPIC	CMD_NAD_CLK_PLS		NAD door motor control		DIC		4XX02	2	MM05D805T
	CPIC	CMD_SDD_A_CLK_PLS		SDD door motor control A		DIC		4XX02	3	MM05D808T
	CPIC	CMD_SDD_A_PH_1		SDD door motor control A		DIC		4XX02	4	MM05D806T
	CPIC	CMD_SDD_A_PH_2		SDD door motor control A		DIC		4XX02	5	MM05D807T
	CPIC	CMD_SDD_A_PH_3		SDD door motor control A		DIC		4XX02	6	MM05D812T
	CPIC	CMD_SDD_A_PH_4		SDD door motor control A		DIC		4XX02	7	MM05D813T
	CPIC	CMD_SDD_B_CLK_PLS		SDD door motor control B		DIC		4XX02	8	MM05D811T
	CPIC	CMD_SDD_B_PH_1		SDD door motor control B		DIC		4XX02	9	MM05D809T
	CPIC	CMD_SDD_B_PH_2		SDD door motor control B		DIC		4XX02	A	MM05D810T
	CPIC	CMD_SDD_B_PH_3		SDD door motor control B		DIC		4XX02	B	MM05D814T
	CPIC	CMD_SDD_B_PH_4		SDD door motor control B		DIC		4XX02	C	MM05D815T
	CPIC	CMD_SVD_BIT_0		SVD door motor control		DIC		4XX02	D	MM05D800T
	CPIC	CMD_SVD_BIT_1		SVD door motor control		DIC		4XX02	E	MM05D801T
	CPIC	CMD_SVD_CLK_PLS		SVD door motor control		DIC		4XX02	F	MM05D802T
	CPIC	SPARE_D_CMD_4		CP spare internal control		DIC		4XX04	4	MM05DXXXT
	CPIC	SPARE_D_CMD_5		CP spare internal control		DIC		4XX04	5	MM05DXXXT
	CPIC	SPARE_D_CMD_6		CP spare internal control		DIC		4XX04	6	MM05DXXXT
	CPIC	SPARE_D_CMD_7		CP spare internal control		DIC		4XX04	7	MM05DXXXT
	CPIC	CMD_A/B_SAM_TM_CLK		SAM mux control		DIC		4XX04	8	MM05D026,28T
	CPIC	CMD_A/B_SAM_TM_RST		SAM mux control		DIC		4XX04	9	MM05D027,29T
	CPIC	SPARE_D_CMD_A/B10		CP spare internal control		DIC		4XX04	A	MM05DXXXT
	CPIC	SPARE_D_CMD_A/B11		CP spare internal control		DIC		4XX04	B	MM05DXXXT
	CPIC	SPARE_D_CMD_A/B12		CP spare internal control		DIC		4XX04	C	MM05DXXXT
	CPIC	SPARE_D_CMD_A/B13		CP spare internal control		DIC		4XX04	D	MM05DXXXT
	CPIC	SPARE_D_CMD_A/B14		CP spare internal control		DIC		4XX04	E	MM05DXXXT
	CPIC	SPARE_D_CMD_A/B15		CP spare internal control		DIC		4XX04	F	MM05DXXXT
	CPIC	SPARE_CMD_26&27		CP spare internal control		DIC		CXX13	D	spare
2	CPIC	CMD_A&B_FAM_TM_CLK		FAM mux control		DIC		CXX13	E	MM05D022,24T
2	CPIC	CMD_A&B_FAM_TM_RST		FAM mux control		DIC		CXX13	F	MM05D023,25T
	31	*<--Total digital internal controls*								

TABLE 10-26. MODIS CP INTERNAL CONTROLS

5/97

pf chg	1 Subsys	2 Name	3 (Not Used)	4 General Remarks	5 (Not Used)	6 Cntl Type	7 (Not Used)	8 HW Address	9 HW Data Loc	10 HW Unique ID
	Not of Interest to End User - - See Notes at table bottom for description of Columns									
	Relay Internal Controls			*Individual controls are needed in some cases to build coupled commands in Table 10-25.*						
	CPIC	CMD_ROM_WRN_A_DISABLE		Not used individually		RIC		CXX00	XX62	MM05Q302F
	CPIC	CMD_ROM_WRN_B_DISABLE		Not used individually		RIC		CXX00	XX5A	MM05Q303F
	CPIC	SPARE		Relay 08_OUT_9		RIC		CXX00	XX47	spare
	CPIC	SPARE		Relay 11_OUT_3		RIC		CXX00	XX52	spare
	CPIC	SPARE		Relay 12_OUT_2		RIC		CXX00	XX59	spare
	CPIC	SPARE		Relay 13_OUT_6		RIC		CXX00	XX65	spare
	CPIC	SPARE		Relay 13_OUT_7		RIC		CXX00	XX66	spare
	PCIC	TURN_OFF_PCA_ECAL		Turns OFF PC A elex calibration		RIC		CXX00	XX55	MM05Q021F
	PCIC	TURN_OFF_PCB_ECAL		Turns OFF PC B elex calibration		RIC		CXX00	XX58	MM05Q023F
1	PCIC	TURN_OFF_PCLWA		PC A_OFF, A&B have individual On/Off cmds		RIC		CXX00	XX0B	MM05Q018F
	PCIC	TURN_OFF_PCLWB		PC B_OFF, A&B have individual On/Off cmds		RIC		CXX00	XX17	MM05Q019F
	PCIC	TURN_ON_PCA_ECAL		Turns ON PC A elex calibration		RIC		CXX00	XX50	MM05Q020F
	PCIC	TURN_ON_PCB_ECAL		Turns ON PC B elex calibration		RIC		CXX00	XX54	MM05Q022F
	PCIC	TURN_ON_PCLWA		PC A_ON, A&B have individual On/Off cmds		RIC		CXX00	XX07	MM05Q016F
	PCIC	TURN_ON_PCLWB		PC B_ON, A&B have individual On/Off cmds		RIC		CXX00	XX0F	MM05Q017F
	PVIC	ENABLE_PVA_ECAL		PVA enable elex cal & chrg subtraction		RIC		CXX00	XX09	MM05Q000F
	PVIC	ENABLE_PVB_ECAL		PVB enable elex cal & chrg subtraction		RIC		CXX00	XX5C	MM05Q007F
	SAIC	SET_SA_HIGAIN		Sets Scan Assy A to high gain		RIC		CXX00	XX1D	MM05Q705F
	SAIC	SET_SA_LOGAIN		Sets Scan Assy A to low gain (normal selection)		RIC		CXX00	XX1E	MM05Q706F
	SAIC	SET_SB_HIGAIN		Sets Scan Assy B to high gain		RIC		CXX00	XX60	MM05Q707F
	SAIC	SET_SB_LOGAIN		Sets Scan Assy B to low gain (normal selection)		RIC		CXX00	XX61	MM05Q708F
	SAIC	TURN_OFF_SAA		Scan Assy B_ON, individual A, B cmds		RIC		CXX00	XX11	MM05Q703F
	SAIC	TURN_OFF_SAB		Scan Assy B_OFF, individual A, B cmds		RIC		CXX00	XX1C	MM05Q704F
	SAIC	TURN_ON_SAA		Scan Assy A_ON, individual A, B cmds		RIC		CXX00	XX19	MM05Q701F
	SAIC	TURN_ON_SAB		Scan Assy B_ON, individual A, B cmds		RIC		CXX00	XX1A	MM05Q702F
	25	*<--Total relay internal controls*								
	56	*<--Total includes HW & SW cmds (HW=direct wires; SW=general form & specific)*								

TABLE 10-26. MODIS CP INTERNAL CONTROLS

5/97

pf chg	1 Subsys	2 Name	3 (Not Used)	4 General Remarks	5 (Not Used)	6 Cntl Type	7 (Not Used)	8 HW Address	9 HW Data Loc	10 HW Unique ID

NOTES:

1. Column 1 is Subsystem 2-alpha code, defined by Table 10 or Figure 11 with an IC internal control suffix.
2. Column 2 is name
3. Columns 3, 5 & 7 are not used.
4. Column 4 contains general remarks.
5. Column 6 is CP Control Type: DIC = digital internal control; RIC = relay internal control.
6. Columns 8 & 9 contain CP hardware hexidecimal address/data locations. Data location entry for DIC cntl types represents single bit of 16-bit word (see 10.5.2).
7. Column 10 is hardware Unique ID for input/output wiring.

PF Change History. Left col Chg#s relate to thes #s. [#S] are general notes.

1. 9/24/94: TURN_OFF_PCLWA Data Loc XX08 to XX0B.
2. 9/21/94: Inter chg names of CMD_A&B_FAM_TM_CLK & CMD_A&B_FAM_TM_RST.
3. 9/21/94: Delete 4 CPIC sigs as they are in active T10-25A list. UIDs: MM05D816T, MM05D817T, MM05D818T, MM05D820T.

TABLE 10-27. MODIS CP07 MODE COMMANDS

5/97

SURVIVAL	SAFE	STANDBY	OUTGAS (& Science)	SCIENCE
TURN ON MOD DR_DRV	TURN ON MOD DR_DRV	TURN OFF MOD BB	TURN MOD ON TGA	TURN MOD ON TGA
SET MOD DR_SDD_DRVA	SET MOD DR_SDD_DRVA	TURN OFF MOD SM	ENABLE MOD CP_IMOK	ENABLE MOD CP_IMOK
MOVE MOD DR_SDD TO CLOSED	MOVE MOD DR_SDD TO CLOSED	TURN OFF MOD SR	SET MOD CP_TMF_BUS TO A	SET MOD CP_TMF_BUS TO A
MOVE MOD DR_NAD TO CLOSED	MOVE MOD DR_NAD TO CLOSED	TURN OFF MOD RCCSHTR	TURN OFF MOD BB	TURN OFF MOD BB
MOVE MOD DR_SVD TO CLOSED	MOVE MOD DR_SVD TO CLOSED	TURN OFF MOD RCISHTR	TURN OFF MOD SM	TURN OFF MOD SM
DISABLE MOD CP_IMOK	DISABLE MOD CP_IMOK	TURN OFF MOD RCOSHTR	TURN OFF MOD SR	TURN OFF MOD SR
SET MOD CP_TMF_BUS TO A	SET MOD CP_TMF_BUS TO A	TURN ON MOD CEA	TURN OFF MOD RCOSHTR	TURN OFF MOD RCCSHTR
TURN OFF MOD BB	TURN OFF MOD BB	SET MOD RC_CFPA_TEMP TO T1	TURN ON MOD RCLWTLM	TURN OFF MOD RCISHTR
TURN OFF MOD SM	TURN OFF MOD SM	The Standby configuration is the same as the prior Mode or state, except for the listed commands.	TURN ON MOD RCSMTLM	TURN OFF MOD RCOSHTR
TURN OFF MOD SR	TURN OFF MOD SR		TURN ON MOD RCCSTLM	TURN ON MOD RCLWTLM
TURN OFF MOD RCCSHTR	TURN OFF MOD RCCSHTR		TURN ON MOD RCISTLM	TURN ON MOD RCSMTLM
TURN OFF MOD RCISHTR	TURN OFF MOD RCISHTR		TURN ON MOD RCOSTLM	TURN ON MOD RCCSTLM
TURN OFF MOD RCOSHTR	TURN OFF MOD RCOSHTR		TURN OFF MOD RCSMHTR	TURN ON MOD RCISTLM
TURN ON MOD RCLWTLM	TURN ON MOD RCLWTLM		TURN OFF MOD RCLWHTR	TURN ON MOD RCOSTLM
TURN ON MOD RCSMTLM	TURN ON MOD RCSMTLM		TURN ON MOD RCCSHTR	TURN OFF MOD RCSMHTR
TURN ON MOD RCCSTLM	TURN ON MOD RCCSTLM		TURN ON MOD RCISHTR	SET MOD RC_CFPA_TEMP TO T1
TURN ON MOD RCISTLM	TURN ON MOD RCISTLM	Spacecraft BDU Commands	SET MOD SA_HIGAIN	TURN ON RCLWHTR
TURN ON MOD RCOSTLM	TURN ON MOD RCOSTLM	• Survival to Safe	TURN ON MOD SAA	SET MOD SA_HIGAIN
TURN OFF MOD RCSMHTR	TURN OFF MOD RCSMHTR	TURN ON MOD CPA	TURN OFF MOD PCLW	TURN ON MOD SAA
TURN OFF MOD RCLWHTR	TURN OFF MOD RCLWHTR	ENABLE MOD PS1_SVHTR	TURN OFF MOD PVLW	TURN ON MOD PCLWA
TURN OFF MOD CE	TURN OFF MOD CE	ENABLE MOD PS2_SVHTR	TURN OFF MOD PVSMIR	TURN ON MOD PVVISA
TURN OFF MOD FI	TURN OFF MOD FI	ENABLE MOD PS12SHDN	TURN ON MOD PVVISA	TURN ON MOD PVNIRA
TURN OFF MOD FO	TURN OFF MOD FO	TURN ON MOD PS1	TURN ON MOD PVNIRA	TURN ON MOD PVLWA
TURN OFF MOD FR	TURN OFF MOD FR	after 30sec issue 1553 command	SET MOD PV_MEM TO RAM	TURN ON MOD PVSMIRA
TURN OFF MOD PCLW	TURN OFF MOD PCLW	SET MOD CP_OPER_MODE TO SAF	SELECT MOD FI_PORTA	SET MOD PV_MEM TO RAM
TURN OFF MOD PVVIS	TURN OFF MOD PVVIS		TURN ON MOD FIA	SELECT MOD FI_PORTA
TURN OFF MOD PVNIR	TURN OFF MOD PVNIR	• Safe to Survival	TURN ON MOD FO_BLK1	TURN ON MOD FIA
TURN OFF MOD PVSMIR	TURN OFF MOD PVSMIR	S/C BDU command	TURN ON MOD FO_BLK2	TURN ON MOD FO_BLK1
TURN OFF MOD PVLW	TURN OFF MOD PVLW	TURN OFF MOD PS1PS2A	TURN ON MOD FRA	TURN ON MOD FO_BLK2
TURN OFF MOD SA	TURN OFF MOD SA		SET MOD FR_PC_DCRCMP TO ON	TURN ON MOD FRA
(After doors are closed ~63sec)	(After doors are closed ~63sec)		SET MOD FR_PV_DCRCMP TO ON	SET MOD FR_PC_DCRCMP TO ON
TURN OFF MOD DR_PWR	TURN OFF MOD DR_PWR		SET MOD FR_RATE TO DAY	SET MOD FR_PV_DCRCMP TO ON
			ENABLE PV_ECAL	SET MOD FR_RATE TO DAY
			TURN ON MOD CEA	ENABLE PV_ECAL
				TURN ON MOD CEA

1. CP07 Mode selection is via the 1553 bus. Flight SW then issues the listed commands.
2. This table is in CSTOL command syntax; Table 10-25A is in command name syntax.
3. Survival entry/exit requires spacecraft BDU pt-pt commands. See above box.
4. Safe entry from Survival requires spacecraft BDU pt-pt commands. See above box.

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20.1 SCOPE

Tables in this Appendix are at the back for continuity of limited text.

Appendix B addresses MODIS telemetry, and contains a short telemetry overview, a definition of type telemetry signals by implementation, a definition of the functional mnemonic name structure, telemetry lists, telemetry alarm limits and telemetry scale factor equations. Appendix D describes command and telemetry relations. It also addresses subsystem redundancies and dependencies.

As noted in Section 1.2, the multiple use of this document for development and test, ICD data definition and operations planning, results in the inclusion of material that is not of interest to all users. In general, the left half of the telemetry list in Table 20-2A will be of interest to end users, while the right half will also be of interest to development designers, programmers, GSE, integration and test personnel.

The MODIS two-character subsystem abbreviations defined in Figure 11 and Table 10 are used throughout this Appendix along with full names.

Table 20-2A MODIS Telemetry is presented later, but remarks about some of its contents are presented earlier as a part of the definition development of particular parameters.

20.2 MODIS TELEMETRY & FLOW

MODIS telemetry is also called housekeeping telemetry in the sense that it is used to monitor the general health and safety of MODIS. Housekeeping telemetry is further categorized as normal housekeeping telemetry and critical housekeeping telemetry. Critical telemetry is a small subset of major configuration items, that when assembled with similar items from other instruments and the spacecraft (S/C), can be sent over a low rate down link to the ground from the S/C. For MODIS, critical telemetry is defined as the items that are directly point-to-point processed by the S/C. They appear with shading in the telemetry lists. Normal housekeeping (HK) telemetry is sent to the S/C over the MIL-STD-1553B Command and Telemetry Bus.

Figure 20-1 indicates the flow of telemetry to the EOS S/C. This includes the point-to-point S/C processed telemetry and the 1553 bus telemetry. The electrical interfaces for each type telemetry is defined in the GSFC 420-03-02 EOS General Instrument Interface Specification, (GIIS). The source of telemetry signals within MODIS is described in 20.4.

Telemetry points from a particular subsystem side are not redundant. Internally processed MODIS telemetry does have redundant paths for processing (it has a side A/B digital telemetry processor, a side A/B analog telemetry processor, and a side A/B 1553 bus).

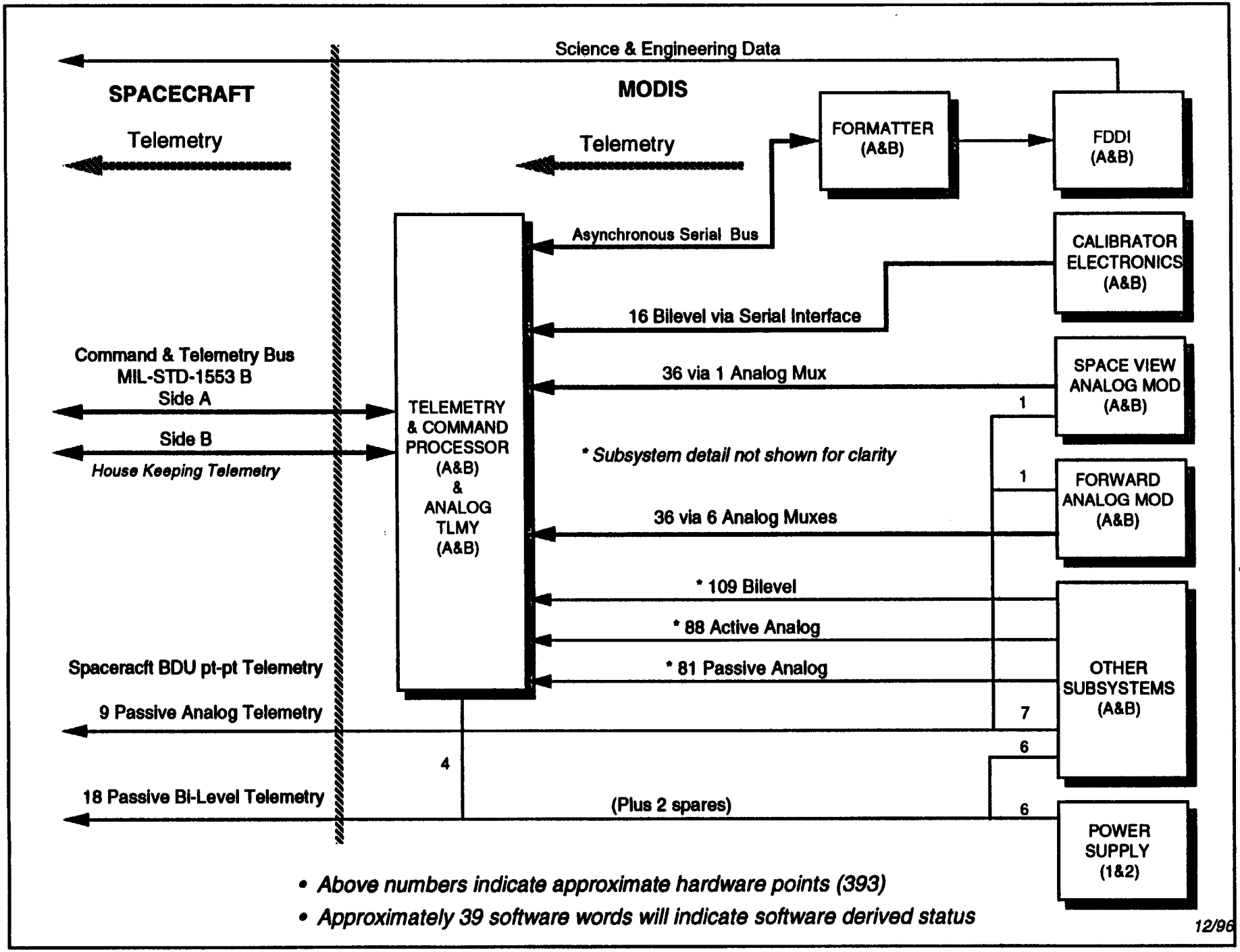

Figure 20-1. MODIS Telemetry Flow Diagram

20.2.1 S/C point-to-point bi-level telemetry. MODIS provides 18 point-to-point bi-level telemetry functions as shown in Figure 20-1 and detailed in Table 20-2A telemetry list. Most relate to the status of MODIS subsystems controlled directly by the S/C point-to-point commands. A few relate to closed-for-launch door status.

20.2.2 S/C point-to-point passive analog telemetry. MODIS provides the point-to-point passive analog telemetry (temperature sensors) shown in Figure 20-1 and detailed in Table 20-2A telemetry list.

20.2.3 1553 bus housekeeping telemetry. MODIS provides housekeeping bus telemetry functions shown in Figure 20-1 and detailed in Table 20-2A telemetry list. The 1553 bus timing and activity schedule was defined in Section 6. MODIS will provide telemetry for pickup during every 1.024 sec Major Cycle, but as noted in 5.2, some 1.024 sec sampled data may be old values since MODIS performs most of its functions based on its 1.477 sec scan cycle. The 1553 bus telemetry frame structure is defined in 20.8.

20.3 TELEMETRY FUNCTIONS BY MNEMONIC NAME

The GIIS requires that telemetry mnemonic names be limited to 16 characters, with the 2 leading characters indicative of the functional use of the telemetry (configuration, status, voltage, etc). Table 20-1 indicates the legend for the use of the 2 leading characters, which are to be followed by an underscore, then the balance of the name. For MODIS, the Type is interpreted to mean the functional use of the telemetry signal. For example, subsystem ON/OFF is classified as a configuration Type signal, even though hardware implementation is generally as a bilevel signal. Also, for the ON/OFF sample, Status is rejected as a Type in the context that Configuration Information items are positively controlled by a command selection, whereas Status items may vary according to other related conditions.

TABLE 20-1. TELEMETRY MNEMONIC NAME STRUCTURE

• 16 Characters: TT_NNNNNNNNNNNNN	
• Type(2 characters),_(1 character),Name(13 characters)	
• Type (TT)	
- 1st T is sample type:	I - Current
	V - Voltage
	T - Temperature
	B - Bilevel Status
	P - Power
	C - Configuration Information
	N - Numeric (i.e.counters)
	S - Status Information
- 2nd T is source:	A - Active Analog
	D - Pseudo or Derived Data
	R - Real or Raw Data
	S - Flight SW Generated Data
	P - Passive Analog
N's are limited to alphanumeric characters and the underscore.	

20.4 MODIS TYPE TELEMETRY

MODIS has several types of telemetry in the context of the hardware/software implementation of the source of its data. Column 8 of the telemetry list in Table 20-2A contains a Type classification code for each entry as defined below. Appendix

20.4.1 Active analog telemetry. Analog telemetry signals which require the sampled circuit to be ON (or active) are classified as active analog type telemetry. Examples are voltage and current telemetry, heater controller temperature sensors, etc. Active analog type are designated by an "A" in telemetry list Table 20-2A.

20.4.2 AEM analog telemetry. Analog telemetry signals which originate from the FAM (PC) or SAM (PV) flow from active circuits through telemetry muxes in each unit. They are designated respectively by an "APC" or an "APV" in telemetry list Table 20-2A.

20.4.3 Digital bilevel telemetry. Digital bilevel telemetry signals indicate the ON/OFF status or bilevel selection state of various subsystem items. They are designated by a "D" in telemetry list Table 20-2A.

20.4.4 Digital bilevel telemetry for calibrators. Digital bilevel telemetry signals indicate the ON/OFF status or bilevel selection state of various calibrators, and flow over the CP-CE serial link, rather than directly to the CP. They are designated by a "DCE" in telemetry list Table 20-2A.

20.4.5 Digital bilevel telemetry by S/C. Some digital bilevel telemetry signals are processed directly by the S/C rather than MODIS. They are designated by a "DS" in telemetry list Table 20-2A.

20.4.6 Passive analog telemetry. Passive analog telemetry does not require the sampled circuit to be ON (or active). For MODIS all passive analog telemetry consists of temperature sensors. These signals are generally processed by a double mux arrangement, with one mux providing an excitation current pulse, and the other mux sampling the resultant voltage across the temperature sensor. The temperature sensors are generally calibrated temperature sensitive resistors, such as thermistors or platinum resistance thermometers (PRT's). Passive analog signals are designated by an "P" in telemetry list Table 20-2A.

20.4.7 Passive analog telemetry by S/C. Some passive analog telemetry signals are processed directly by the S/C rather than MODIS. They are designated by an "PS" in telemetry list Table 20-2A.

20.4.8 Software telemetry. Some telemetry is generated from software (SW), and can vary from simple bilevel information, to digital values from a given bit word, to packed digital words that have field definitions. They are designated by a "SW" in telemetry list Table 20-2A.

20.5 MODIS ANALOG TELEMETRY FLOW

MODIS analog telemetry, active and passive, is processed by a chain of analog muxes, dedicated to particular signal groups as illustrated in Figure 20-2. The muxes are funneled down to a single path by a multi-stage process to a single analog-to-digital converter (ADC), which provides the conversion of all analog signals to a digital signal. All muxes have a 16 channel capacity. Passive muxes have related excitation muxes, which are not depicted in Figure 20-2. All the individual inputs to the muxes are directly addressable per the write/read address and data locations listed in the right side of telemetry list Table 20-2A. The FAM and SAM muxes are not directly addressable; access to their particular data is described in 20.5.4.

20.5.1 Analog mux groups. In Figure 20-2, it will be noted that there are the following groups:

a. Seven active muxes - all active analog telemetry signals are routed to one of these inputs directly from the monitored subsystem, except for FAM and SAM signals as noted below.

b. One passive mux dedicated to precision BB temperature processing.

c. One passive PRT mux for lower range temperature sensors (PRT's require a different excitation than thermistors).

d. Five passive muxes for general range temperature sensors.

20.5.2 ADC conversion. The resolution conversion of the analog signals are 8, 9, 10 and 12 bits. Special care is exercised in wiring implementation of signals to be converted to 12 bits. Also, passive analog signals that are converted to 12 bits generally use a 4-wire temperature sensor to minimize errors.

20.5.3 Analog references. There are various analog references associated with each of the analog muxes illustrated in Figure 20-2. The active muxes have voltages from precision resistance dividers, and the passive muxes have precision resistors. The BB mux has calibrated precision resistors. These calibration references are listed in the telemetry list Table 20-2A under the TM Subsystem as a VR functional signal. These references coupled with the knowledge that many subsystems are monitoring regulated voltages, should provide excellent data to assess the performance of the analog telemetry processor, and the ability to track long term variations.

20.5.4 FAM & SAM analog muxes. The FAM and SAM muxes flow as a single line per mux (6/FAM & 1/SAM) into one of the inputs of the active muxes in Figure 20-2. Table 20-2A provides the general input location of the FAM or SAM mux ports. Specific FAM (PC) or SAM (PV) analog signals are accessed by a common FAM/SAM mux Reset, then sequentially stepped through the muxes according to the locations listed in Table 20-3. FAM data automatically flows from whichever side is active. But the SAM shows data locations of the form 0/1, 2/3, 4/5, 6/7 and 1-->16 . This indicates that the left-hand numbers provide A_side data and the right-hand numbers provide B_side data. All of the SAM 1-16 ports per function group are not used (the 0/1, 2/3, etc, are not the PWB REF designators but correspond to PWB groups which support 4 FPAs.

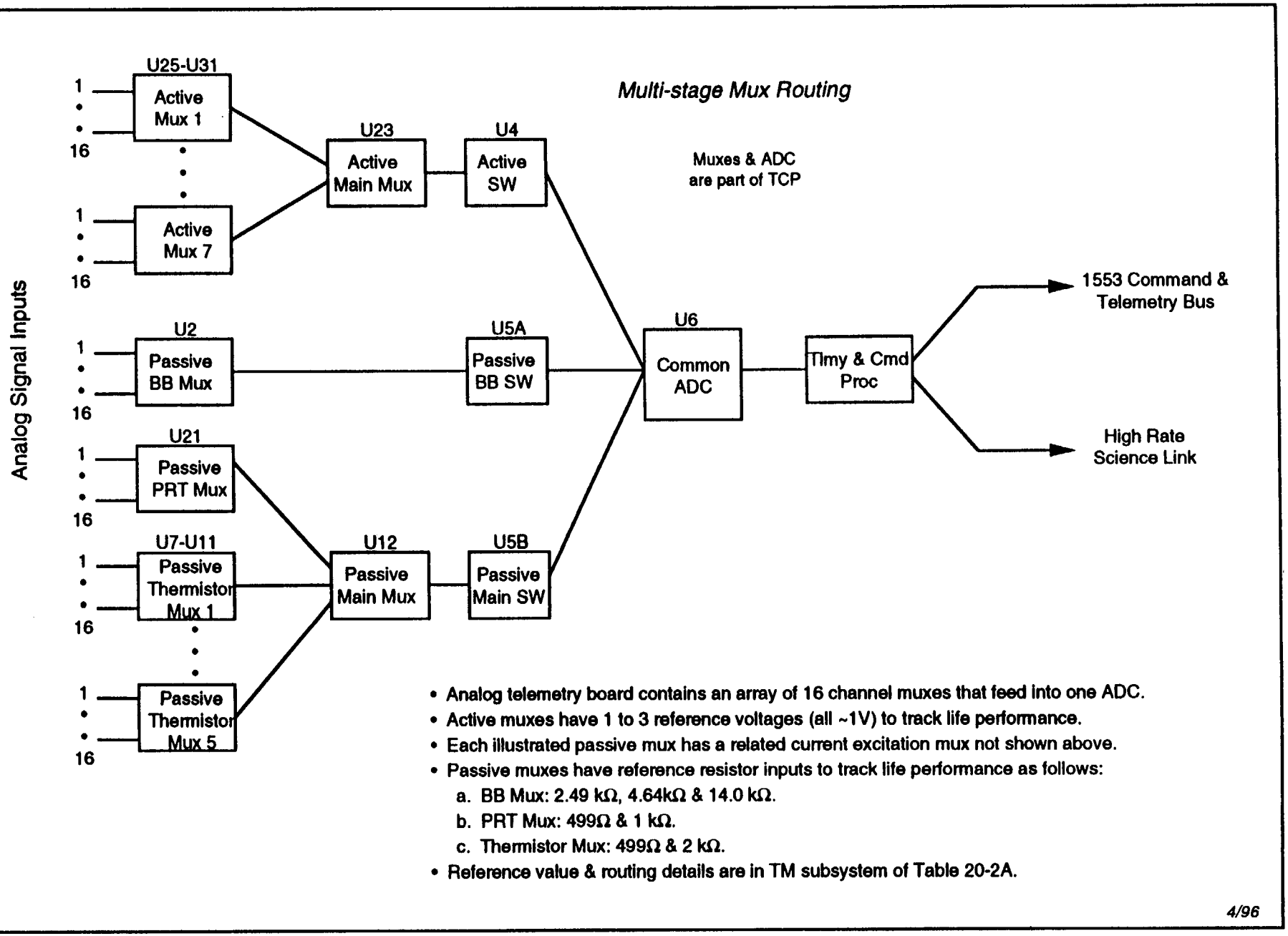

Figure 20-2. MODIS Analog Telemetry Flow Diagram

20.6 MODIS TELEMETRY

MODIS telemetry is presented by Table 20-2A MODIS Telemetry List, which is sorted by Subsystem, then by Mnemonic Name. As needed, Table 20-2B provides a further definition of some telemetry Items. Subsystems are identified by the leading 2 character legend in Table 20-1. Preceding 20.2, 20.3, 20.4 and 20.5 have already defined a major part of the Table 20-2A contents. Notes at the bottom of Table 20-2A also provide summary descriptions of table codes or other features. Material in these notes are not repeated at the end of Table 20-2B.

As constantly emphasized throughout this document, all of the data in the tables will not be of interest to all. End user interest is probably limited to data through Column 7. The remaining columns would be of interest to HW/SW development, integration and test personnel.

The Subsystem sort of Table 20-2A contains the total telemetry that is associated with each subsystem. It also includes development telemetry that has subsequently been turned into spares, as well as, initial hardware telemetry spare capability (listed at the bottom, not of interest to the end user). Spares information is included for documentation completeness.

As noted in the Remarks column, a few items in Table 20-2A also appear in the Engineering Data Packet, and have similar names. If they first appeared in the Engineering Data, and were added to the Telemetry List, their name ends in an "H". If they first appeared in the Telemetry List, then added to the Engineering Data, their name ends in "E".

20.7 FAM & SAM MUX DATA LOCATION

As noted, FAM and SAM analog telemetry data is routed to the analog telemetry processor (TM) by mux lines. The FAM has 6 analog muxes, one for each band, Band 31-36, and the SAM has a single mux with mused inputs. The muxes are not redundant, but they process active A side or B side data for the FAM and SAM. Each of these muxes has a unique input port location on the analog telemetry processor as listed in Table 20-2A. As described in 20.5.4, data from these muxes are not directly addressable, but are accessed by a reset signal, and then the sequential activation of a step control line to step through each input port. Table 20-3 provides the particular mux identification and data location for the FAM (PC) and SAM (PV) analog telemetry.

20.8 MODIS TELEMETRY FRAME DEFINITION

The telemetry contained in Table 20-2A, minus the S/C processed items, is formatted into a telemetry frame that is partitioned into 1 sec, 8 sec and 65 sec sample groups (really 1.024 sec, 8.192 sec & 65.536 sec) for transmittal over the 1553 bus. A telemetry Master Cycle consists of 64 Major Cycles (1.024 sec), and a Major Cycle contains 128 Minor Cycles (8 mS). Most discussions occur at the Major Cycle level. Table 20-4 provides the definition of the telemetry frame. The rationale for its structure is contained in its notes. Also, the notes contain a figure illustrating the boundaries of each sample group in terms of the Major Cycle bit ID and the number of 16-bit words contained in each sample group (512 bits = 32 16-bit words). MODIS 1553 bus telemetry pickup occurs in Minor Cycle 72.

20.9 TELEMETRY LIMITS & EQUATIONS

Normal operating limits and alarm limits for telemetry values are listed in Table 20-5 for active analog telemetry and in Table 20-6 for passive analog telemetry. These limits are also respectively referred to as yellow alarm limits and red alarm limits. Yellow alarm limits are to be taken as a notice to focus attention on parameters that may be shifting towards out-of-limit red alarms. Red alarms requires active response to implement action, to verify other key related telemetry values, or, turn off a subsystem, or, to immediately shift into a troubleshooting sequence (if one has had prior definition.) Dependent upon the nature of the subsystem, the reaction may be to turn it off, and immediately bring the redundant subsystem on line (if one exists) in order to continue science. Then formulate a troubleshooting sequence after the data has been analyzed.

The scale factor equations to transform analog telemetry raw data numbers (DN) into engineering units are contained in Table 20-5 for active analog items and Table 20-6 for passive analog items. Scale factors for digitally defined items and software items are contained in Table 20-2A, Column 7.

20.10 TMON TELEMETRY & RESPONSE

The EOS-AM S/C has telemetry monitoring (TMON) and response capability that is available to instruments. Initial TMON items are the 8 temperatures processed directly by the S/C (shaded items in Table 20-2A). Responses to Hot or Cold limit excursions will be defined by separate documentation.

20.11 MODIS TEMPERATURE SENSORS & LOCATION

MODIS contains a generous complement of temperature sensors as listed in Table 20-2A. They vary in temperature range, accuracy and manner of implementation. The types of temperature sensors vary from diodes, two-wire thermistors, three-wire thermistors and two-wire PRT's. They are implemented as active or passive sensors.

The temperature accuracy generally tracks the readout resolution, which varies from 8, 9, or 12 bits. However, all 12 bit temperature items do not have the same accuracy as some 12 bit items, such as, the focal plane, BB and outgas calibrated temperature points. Twelve bit resolution was selected for some noncalbirated temperature sensors to show internal subsystem relations during engineering development and thermal modeling verification. Thus, common scale factor equations are provided for many temperature items in Table 20-6 for the lower accuracy temperature sensors. Unique scale factor equations are provided for the cited higher accuracy temperature sensors in both Table 20-5 and T20-6.

Temperature sensor locations are defined by engineering drawings for each of the affected subsystems.

20.12 MODIS DIRECT TELEMETRY PINOUTS/TEST FRAMING

Table 20-7 provides reference information on SBRS RTIU pinouts, which is STE emulator for the spacecraft BDU.

TABLE 20-2A. MODIS TELEMETRY LIST

Sort by Subsystem - - End User Interest extends through Column 7 - - See Notes at table bottom - - Shaded area indicates S/C pt-pt processing. *5/97*

pfm chg#	1 Subsys	2 Mnemonic Name	3 # of Bits	4 Sample Period	5 Tlmy Range	6 Equations & Limits	7 Remarks	8 Tlmy Type	9 Analog Mux	10 HW Addr Write/Read	11 HW Data Loc	12 Design Unique ID
4	AO	TA_AO_NIR_FPA	12	65	-43 to +85°C	T20-5	NIR warm FPA temp	A	U28	C0003/C0004	5F75	MM11A27T
4	AO	TA_AO_VIS_FPA	12	65	-43 to +85°C	T20-5	VIS warm FPA temp	A	U28	C0003/C0004	5EF5	MM11A25T
	AO	TP_AO_LWIR_LENS	12	65	-43 to +85°C	T20-6	LWIR eye lens assy temp (4 wire)	P	U11	C0003/C0004	315B	AP00A03T
	AO	TP_AO_LWIR_OBJ	12	65	-43 to +85°C	T20-6	LWIR objective assy temp (4 wire)	P	U11	C0003/C0004	31DB	AP00A04T
	AO	TP_AO_PX_NZ_CORN	12	65	-43 to +85°C	T20-6	AOP +X, -Z corner (4 wire)	P	U11	C0003/C0004	335B	AP00A07T
	AO	TP_AO_PZ_BY_RC	8	65	-50 to +78°C	T20-6	AO lower end +Z temp near cooler mount (S/C)	PS	na	na	na	AP00A01T
	AO	TP_AO_SMIR_LENS	12	65	-43 to +85°C	T20-6	SMIR eye lens assy temp (4 wire)	P	U11	C0003/C0004	325B	AP00A05T
	AO	TP_AO_SMIR_OBJ	12	65	-43 to +85°C	T20-6	SMIR objective lens assy temp (4 wire)	P	U11	C0003/C0004	32DB	AP00A06T
	AO	TP_AO_VNDICH_HSG	12	65	-43 to +85°C	T20-6	VIS/NIR dichroic housing or mount temp (4 wire)	P	U11	C0003/C0004	30DB	AP00A02T
	BB	CR_BB_A_PWR_ON	1	8	na	na	BB Pwr AON_BOFF=1, AOFF=0 by R cmd	D	na	40005	E	MM09D26T
	BB	CR_BB_B_PWR_ON	1	8	na	na	BB Pwr BON_AOFF=1, BOFF=0 by R cmd	D	na	40005	F	MM09D27T
14	BB	CR_BB_SPARE	1	8	na	na	BB Spare (was BB HTR OFF via DCE)	DCE	na	C0001	0	na
	BB	CS_BB_TEMP_SET	12	8	0 to 999 DN	Col 7	BB Htr Temp Set Pt D#XXX integer DN. Valid from DN=338=311K to DN=129=317K. Normal DN=193=315K. Also in eng T30-5D	SW	na	na	na	na
	BB	IR_BB_HTRA_CURH	8	8	0 to 1.25A	T20-5	BB Htr A current; also in eng T30-5D	SW	U27	na	5572	MM09A01T
	BB	IR_BB_HTRB_CURH	8	8	0 to 1.25A	T20-5	BB Htr B current; also in eng T30-5D	SW	U27	na	5773	MM09A19T
18	BB	TP_BB_TEMP01H	12	8	270K to 320K	T20-6	Obc BB temp; also in eng T30-5D	SW	U2	na	X00B	CE01A01T
18	BB	TP_BB_TEMP02H	12	8	270K to 320K	T20-6	Obc BB temp; also in eng T30-5D	SW	U2	na	X08B	CE01A02T
18	BB	TP_BB_TEMP03H	12	8	270K to 320K	T20-6	Obc BB temp; also in eng T30-5D	SW	U2	na	X10B	CE01A03T
18	BB	TP_BB_TEMP04H	12	8	270K to 320K	T20-6	Obc BB temp; also in eng T30-5D	SW	U2	na	X18B	CE01A04T
18	BB	TP_BB_TEMP05H	12	8	270K to 320K	T20-6	Obc BB temp; also in eng T30-5D	SW	U2	na	X20B	CE01A05T
18	BB	TP_BB_TEMP06H	12	8	270K to 320K	T20-6	Obc BB temp; also in eng T30-5D	SW	U2	na	X28B	CE01A06T
18	BB	TP_BB_TEMP07H	12	8	270K to 320K	T20-6	Obc BB temp; also in eng T30-5D	SW	U2	na	X30B	CE01A07T
18	BB	TP_BB_TEMP08H	12	8	270K to 320K	T20-6	Obc BB temp; also in eng T30-5D	SW	U2	na	X38B	CE01A08T
18	BB	TP_BB_TEMP09H	12	8	270K to 320K	T20-6	Obc BB temp; also in eng T30-5D	SW	U2	na	X40B	CE01A09T
18	BB	TP_BB_TEMP10H	12	8	270K to 320K	T20-6	Obc BB temp; also in eng T30-5D	SW	U2	na	X48B	CE01A10T
18	BB	TP_BB_TEMP11H	12	8	270K to 320K	T20-6	Obc BB temp; also in eng T30-5D	SW	U2	na	X50B	CE01A11T
18	BB	TP_BB_TEMP12H	12	8	270K to 320K	T20-6	Obc BB temp; also in eng T30-5D	SW	U2	na	X58B	CE01A12T
	CE	CR_CE_A_ON	1	8	na	na	Cal Electronics AON_BOFF=1 by R cmd	D	na	C000E	C	MM09D20T
	CE	CR_CE_B_ON	1	8	na	na	Cal Electronics BON_AOFF=1 by R cmd	D	na	C000E	D	MM09D21T
	CE	TP_CE_CAL2	9	65	-43 to +85°C	T20-6	Cal control board 2 temp	P	U7	C0003/C0004	21BB	MM10A20T
70,75	CP	CR_CPA_EEP_WRE_M	1	8	na	na	Via 1553 tlmy, CP A EEP write enable=0, disable=1 by S/C R cmd (global disable by CP 1553); * * 'OFF' SIDE TLMY IS INVALID * *	D	na	C000E	E	MM05D009T
	CP	CR_CPA_EEP_WRE_S	1	8	na	na	Via S/C tlmy, CP A EEP write enable=0, disable=1 by S/C R cmd (global disable by CP 1553)	DS	na	na	na	MM05K000T
70,75	CP	CR_CPB_EEP_WRE_M	1	8	na	na	Via 1553 tlmy, CP B EEP write enable=0, disable=1 by S/C R cmd (global disable by CP 1553); * * 'OFF' SIDE TLMY IS INVALID * *	D	na	C000E	F	MM06D009T
	CP	CR_CPB_EEP_WRE_S	1	8	na	na	Via S/C tlmy, CP B EEP write enable=0, disable=1 by S/C R cmd (global disable by CP 1553)	DS	na	na	na	MM06K000T
29	CP	CR_CP_A_ON_M	1	8	na	na	Via 1553 tlmy, CP AON_BOFF=1 by S/C cmd	D	na	C000E	4	MM05D500T
	CP	CR_CP_A_ON_S	1	8	na	na	Via S/C tlmy, CP AON_BOFF=0, AOFF=1 by R cmd	DS	na	na	na	MM05K950T
29	CP	CR_CP_B_ON_M	1	8	na	na	Via 1553 tlmy, CP BON_AOFF=1 by S/C cmd	D	na	C000E	5	MM06D500T
	CP	CR_CP_B_ON_S	1	8	na	na	Via S/C tlmy, CP BON_AOFF=0, BOFF=1 by R cmd	DS	na	na	na	MM06K950T

TABLE 20-2A. MODIS TELEMETRY LIST

Sort by Subsystem - - End User Interest extends through Column 7 - - See Notes at table bottom - - Shaded area indicates S/C pt-pt processing. *5/97*

pfm chg#	1 Subsys	2 Mnemonic Name	3 # of Bits	4 Sample Period	5 Tlmy Range	6 Equations & Limits	7 Remarks	8 Tlmy Type	9 Analog Mux	10 HW Addr Write/Read	11 HW Data Loc	12 Design Unique ID
	CP	CR_CP_SET_TMF_A	1	8	na	na	CP TMF_A=0, B=1; also in eng T30-5D	D	na	C000B	0	na
	CP	CR_SPARE	1	na	na	na	(Spare S/C pt; formerly CP UPLD reset)	D9	na	na	na	?
	CP	CR_SPARE	1	na	na	na	(Spare S/C pt; formerly CP STD reset)	D9	na	na	na	wired spare
22,57	CP	CS_CP_MODIS_MOD	3	65	EM/PF/F1/F2	Col 7	MODIS Model EM=B#000, PF=B#001, F1=B#010, F2=B#011, other values not used	SW	na	na	na	na
66	CP	CP_SPARE	12	8	na	na	Was CS_CP_PK_PWR	SW	na	na	na	na
	CP	SS_CP1553_MAJCYC	6	1	0 to 63	na	Maj Cyc ID D#0-63 (MODIS tlmy placed in each Min Cyc#72)	SW	na	na	na	na
	CP	SS_CP_CMD_ECHO	16	1	na	na	Echos bus cmds in CP execution seq (1st word of bus structure, see T10-2 to T10-21)	SW	na	na	na	na
	CP	SS_CP_IMOK_ON	1	8	na	na	CP Monitor SC IMOK On=1/Off=0; (IMOK is in Min Cyc#44); also in eng T30-5D	SW	na	na	na	na
43,64	CP	SS_CP_LAST_EVENT	16	1	na	na	Upper 8-bits provide 1-255 event count, lower 8-bits provide event code. See 152932 Flt SW Maintenance Manual for event codes.	SW	na	na	na	na
64	CP	SS_CP_LOG_EVENT	1	1	na	na	High indicates entry into CP event log; see SS_CP_LAST_EVENT for type event	SW	na	na	na	na
53	CP	SS_CP_LOG_STATE	4	8	D#0-15		D#(4 bits) Reflects OPERAND & INSTRUCTION class of loads/dumps	SW	na	na	na	na
65	CP	SS_CP_MACRO_ID	5	1	D#0-31	na	If macro sequence is running, ID number = D#0-31; 0 if not running	SW	na	na	na	na
65	CP	SS_CP_MACRO_ON	1	1	na	na	Indicates if macro cmd sequence is running; YES=1, NO=0	SW	na	na	na	na
	CP	SS_CP_MODE	3	1	5 Modes	Col 7	CP MODE: Survival=D#1=B#001; Safe=D#2=B#010; Standby=D#3=B#011; Outgas=D#4=B#100; Science=D#5=B#101; all others invalid; also in eng T30-5D	SW	na	na	na	na
	CP	SS_CP_MODECHG_GO	1	1	na	na	CP Mode Chg Go (start): 1=Chg started, 0= Chg complete	SW	na	na	na	na
	CP	SS_CP_RESET_SRC	3	8	na	na	CP Reset source: 000=PS, 001=CPA/CPB select, 010=CP Standard, 011= CP Upload, 100 - 111 invalid.	SW	na	na	na	na
42	CP	SS_CP_SCAN_EST	16	8	tbd	na	Was CP_Status_02. SW estimate of scan period in milliseconds. If Sector transition interrupts are not being received from the FR, the value is set to FFFF.	SW	na	na	na	na
54	CP	SS_CP_SPARE	1	8	na	na	Was SS_CP_MEMPRO_ERR	SW	na	na	na	na
54	CP	SS_CP_SPARE	1	8	na	na	Was SS_CP_PARITY_ERR	SW	na	na	na	na
	CP	SS_CP_SPARE	8	1	na	na	CP Spare (was8-bit sec before new full TC1,2,3,4 time code)	SW	na	na	na	na
54	CP	SS_CP_SPARE	1	8	na	na	Was SS_CP_TEST_RES	SW	na	na	na	na
55, 77	CP	SS_CP_STATUS_04	16	8	tbd	na	CRC Checksum for the CP Flight Software VDD 153803	SW	na	na	na	na
77	CP	SS_CP_STATUS_05	16	8	tbd	na	CRC Checksum for the CP Flight Macro Table VDD 154132	SW	na	na	na	na
77	CP	SS_CP_STATUS_06	16	8	tbd	na	CRC Checksum for the FP Flight Software VDD 153803	SW	na	na	na	na
77	CP	SS_CP_STATUS_07	16	8	tbd	na	CRC Checksum for the Normal Mode WCS VDD 153936	SW	na	na	na	na
77	CP	SS_CP_STATUS_08	16	8	tbd	na	CRC Checksum for the Test Mode WCS VDD 153937	SW	na	na	na	na
77	CP	SS_CP_STATUS_09	16	8	tbd	na	CP/FR Reset Register Bits. See Table 20-2C for individual bit details	SW	na	na	na	na
44	CP	SS_CP_TC1_DAYS	16	1	Add TC1,2,3,4	Col 7	64 bit CCSDS time code as TC1, TC2, TC3,TC4. TC1 is days	SW	na	na	na	na
44	CP	SS_CP_TC2_MILLIS	16	1	Add TC1,2,3,4	Col 7	since 1/1/1958 epoch. TC2 is 16 MSBs of ms of day.	SW	na	na	na	na
44	CP	SS_CP_TC3_MILLIS	16	1	Add TC1,2,3,4	Col 7	TC3 is16 LSBs of day. TC4 is µs of ms. Add together for	SW	na	na	na	na
44	CP	SS_CP_TC4_MICROS	16	1	Add TC1,2,3,4	Col 7	display as YY:DDD:HH:MM:SS.S.	SW	na	na	na	na
2	CP	SS_CP_TMF_GONE	1	8	na	na	High means S/C sync gone & operation on internal MODIS TMF	SW	na	na	na	na
42	CP	SS_CP_UART_HUNT	16	8	tbd	na	Was CP_Status_11. Counts number of scans with internal UART logic in HUNT state	SW	na	na	na	na

TABLE 20-2A. MODIS TELEMETRY LIST

Sort by Subsystem - - End User Interest extends through Column 7 - - See Notes at table bottom - - Shaded area indicates S/C pt-pt processing.

5/97

pfm chg#	1 Subsys	2 Mnemonic Name	3 # of Bits	4 Sample Period	5 Tlmy Range	6 Equations & Limits	7 Remarks	8 Tlmy Type	9 Analog Mux	10 HW Addr Write/Read	11 HW Data Loc	12 Design Unique ID
42	CP	SS_CP_UART_NORM	16	8	tbd	na	Was CP_Status_13. Counts number of scans with internal UART logic in NORMAL state	SW	na	na	na	na
42	CP	SS_CP_UART_RESET	16	8	tbd	na	Was CP_Status_10. Counts number of times the internal UART to the FR has been reset	SW	na	na	na	na
42	CP	SS_CP_UART_SYNC	16	8	tbd	na	Was CP_Status_12. Counts number of scans with internal UART logic in SYNC state	SW	na	na	na	na
	CP	SS_CP_VALTLM_COL	1	1	na	na	CP HK tlmy collect valid=1, invalid=0	SW	na	na	na	na
	CP	SS_CP_VALTLM_FMT	1	1	na	na	CP HK tlmy format valid=1, invalid=0	SW	na	na	na	na
	CP	TP_CP_A_1553	9	65	-43 to +85°C	T20-6	Control Proc 1553 IC temp	P	U7	C0003/C0004	20BB	MM05A01T
	CP	TP_CP_B_1553	9	65	-43 to +85°C	T20-6	Control Proc 1553 IC temp	P	U7	C0003/C0004	213B	MM06A01T
	CP	VR_CP_N11V	8	65	-13.6 to 0V	T20-5	CP -11V Pwr	A	U25	C0003/C0004	8771	same PWB
	CP	VR_CP_N5V	8	65	-6.3 to 0V	T20-5	CP -5V Pwr	A	U25	C0003/C0004	87F1	same PWB
	CP	VR_CP_P11V	8	65	0 to 13.6V	T20-5	CP +11V Pwr	A	U25	C0003/C0004	8671	same PWB
	CP	VR_CP_P5V	8	65	0 to 6.3V	T20-5	CP +5V Pwr	A	U25	C0003/C0004	86F1	same PWB
60	CP	CR_WIREDSPARE1	1	8	na	na	S/C wired spare to J4 (not wired in M ODIS)	DS	na	na	na	na
60	CP	CR_WIREDSPARE2	1	8	na	na	S/C wired spare to J4 (not wired in M ODIS)	DS	na	na	na	na
	DR	CR_DRNAD_1LATCHD	1	8	na	na	1=latched (launch only, not relatched after release)	DS	na	na	na	DR02K01T
	DR	CR_DRNAD_2LATCHD	1	8	na	na	1=latched (launch only, not relatched after release)	DS	na	na	na	DR02K02T
	DR	CR_DRSDD_LATCHD	1	8	na	na	1=latched (launch only, not relatched after release)	DS	na	na	na	DR03K01T
	DR	CR_DRSVD_1LATCHD	1	8	na	na	1=latched (launch only, not relatched after release)	DS	na	na	na	DR01K01T
	DR	CR_DRSVD_2LATCHD	1	8	na	na	1=latched (launch only, not relatched after release)	DS	na	na	na	DR01K02T
	DR	CR_DR_DRV_ON	1	8	na	na	DR drive ON=1, OFF=0 by R cmd (Unlach A&B s/b off)	D	na	C0010	3	MM12K01T
	DR	CR_DR_FS_ENABL_M	1	8	na	na	Via 1553 tlmy, DR FS ENABLE=1 by S/C R cmd for global 1st FS step (disable by 1553 cmd)	D	na	C0010	B	MM12K09T
75	DR	CR_DR_FS_ENABL_S	1	8	na	na	Via S/C tlmy, DR FS ENABLE=0/DISABLE=1 by R cmd for global 1st FS step (disable by 1553 cmd)	DS	na	na	na	MM12R03T
	DR	CR_DR_FS_SW_CLSD	1	8	na	na	DR FS SW Closed=1, Open=0 common 2nd step by R cmd	D	na	C0010	4	MM12K02T
	DR	CR_DR_NAD_CLSD	1	8	na	na	NAD closed=1, not closed=0 by hi-lev cmd	D	na	C0012	A	DR02D01T
	DR	CR_DR_NAD_FS_ON	1	8	na	na	3rd final step NAD FS ON=1, Off=0 by R cmd	D	na	C0010	6	MM12K04T
	DR	CR_DR_NAD_OPEN	1	8	na	na	NAD Open=1, Not Open=0 by hi-lev cmd	D	na	C0012	B	DR02D02T
2	DR	CR_DR_PRI_FS_SEL	1	8	na	na	NAD & SVD FS Pri=1/Rdt=0 by R cmd, thermostatic SW in rtn	D	na	C0010	A	MM12K08T
	DR	CR_DR_SDD_CLSD	1	8	na	na	SD door closed=1, not closed=0; door and/or screen closed by same hi-lev cmd	D	na	C0012	C	DR03D01T
	DR	CR_DR_SDD_DRV_A	1	8	na	na	SDD DRV A=1, B=0 selected by R cmd	D	na	C0010	2	MM12D13T
	DR	CR_DR_SDD_OPEN	1	8	na	na	SDD Open=1, Not Open=0 by hi-lev cmd	D	na	C0012	D	DR03D02T
2	DR	CR_DR_SDFS_DRVON	1	8	na	na	SDD FS Drv On=1/Off=0 3rd step (has 4th final step w/o tlmy)	D	na	C0010	7	MM12K05T
	DR	CR_DR_SDS_OPEN	1	8	na	na	SD screen Open=1, Not Open=0 by hi-lev cmd	D	na	C0012	F	DR03D04T
24	DR	CR_DR_SPARE	1	8	na	na	Spare (was SD screen closed=1)	D	na	C0012	E	DR03D03T
	DR	CR_DR_SVD_CLSD	1	8	na	na	SVD Closed=1, Not Closed=0 by hi-lev cmd	D	na	C0012	8	DR01D01T
	DR	CR_DR_SVD_FS_ON	1	8	na	na	3rd final step SVD FS On=1, Off=0 by R cmd	D	na	C0010	5	MM12K03T
	DR	CR_DR_SVD_OPEN	1	8	na	na	SVD Open=1, Not Open=0 by hi-lev cmd	D	na	C0012	9	DR01D02T
	DR	CR_DR_UNLACH_AON	1	8	na	na	Unlatch A drive On=1, Off=0 by R cmd (unlch B & mtr drive s/b off)	D	na	C0010	0	MM12D11T
	DR	CR_DR_UNLACH_BON	1	8	na	na	Unlatch B drive On=1, Off=0 by R cmd (unlch A & mtr drive s/b off)	D	na	C0010	1	MM12D12T

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	DR	CS_DR_SVD_AT_OG	1	8	na	na	SVD at Outgas=1 (~5°=206 steps), Not at OG=0	SW	na			na
52,75	DR	SS_DR_NAD_STEP	13	1	D#0-3750	Col 7	NAD mtr absolute step count = D#(13 bits), max=3750 (0.0243°/step); Home=Clsd=0 step (to open=mtr CW)	SW	na	na	na	na
2,52,75	DR	SS_DR_SDD_STEP	12	1	D#0-2145	Col 7	SDD mtr absolute step count= D#(12 bits) , max=2145 both open, door only~1027 (0.0957°/step); Home=Clsd=0 step (to open=mtr CCW)	SW	na	na	na	na
52,75	DR	SS_DR_SVD_STEP	13	1	D#0-4060	Col 7	SVD mtr absolute step count=D#(13 bits), max=4060 (0.0243°/step); Home=Clsd=0 step (to open=mtr CCW)	SW	na	na	na	na
	DR	TP_DR_NAD	9	65	-43 to +85°C	T20-6	Nadir aperture door temp	P	U10	C0003/C0004	161B	DR02A01T
27	DR	TP_DR_NAD_FS	9	8	-43 to +85°C	T20-6	Nadir aperture door failsafe temp (was motor temp)	P	U10	C0003/C0004	169B	DR02A02T
	DR	TP_DR_SDD	9	65	-43 to +85°C	T20-6	Solar diffuser door temp	P	U10	C0003/C0004	179B	DR03A02T
27	DR	TP_DR_SPARE	9	8	-43 to +85°C	T20-6	Door TP_SPARE (was Solar diffuser door motor temp)	P	U10	C0003/C0004	171B	DR03A01T
	DR	TP_DR_SVD	9	65	-130 to +60°C	T20-6	Space view door temp	P	U21	C0003/C0004	38EB	DR01A01T
27	DR	TP_DR_SVD_FS	9	8	-43 to +85°C	T20-6	Space view door failsafe temp (was motor temp)	P	U10	C0003/C0004	159B	DR01A02T
	FI	CR_FI_A_ON	1	8	na	na	FDDI AON_BOFF=1, AOFF=0 by R cmd	D	na	C0011	4	MM17B03T
52,75	FI	CR_FI_PORT_A_ON	1	8	na	na	FDDI PORT_A AON_BOFF=1, AOFF_BON=0 by R cmd	D	na	C0011	5	MM17B04T
	FI	CR_FI_A_RESET	1	8	na	na	FDDI A reset=0, running=1 by D cmd	D	na	C0011	7	MM17D14T
	FI	CR_FI_B_ON	1	8	na	na	FDDI BON_A_OFF=1, BOFF=0 by R cmd	D	na	C0011	8	MM18B03T
52,75	FI	CR_FI_PORT_B_ON	1	8	na	na	FDDI PORT_B BON_AOFF=1, BOFF_AON=0 by R cmd	D	na	C0011	9	MM18B04T
	FI	CR_FI_B_RESET	1	8	na	na	FDDI B reset=0, running=1 by D cmd	D	na	C0011	B	MM18D14T
	FO	CR_FO_BLK1_ON	1	8	na	na	FIFO BLK1 ON=1, OFF=0 by R cmd	D	na	C000D	8	MM03B05T
	FO	CR_FO_BLK2_ON	1	8	na	na	FIFO BLK2 ON=1, OFF=0 by R cmd	D	na	C000D	9	MM03B06T
	FO	CR_FO_BLK3_ON	1	8	na	na	FIFO BLK3 ON=1, OFF=0 by R cmd	D	na	C000D	A	MM03B07T
	FO	CR_FO_BLK4_ON	1	8	na	na	FIFO BLK4 ON=1, OFF=0 by R cmd	D	na	C000D	B	MM03B08T
19	FO	CR_FO_SPARE	1	8	na	na	FO_SPARE, was CR_FO_BLK1_RESET	D	na	C000D	C	MM03D16T
19	FO	CR_FO_SPARE	1	8	na	na	FO_SPARE, was CR_FO_BLK2_RESET	D	na	C000D	D	MM03D17T
19	FO	CR_FO_SPARE	1	8	na	na	FO_SPARE, was CR_FO_BLK3_RESET	D	na	C000D	E	MM03D18T
19	FO	CR_FO_SPARE	1	8	na	na	FO_SPARE, was CR_FO_BLK4_RESET	D	na	C000D	F	MM03D19T
17	FO	SR_FO_BLK1_MODE	1	8	na	na	FIFO Blk1 mode status 0=read; 1=write	D	na	C000E	0	MM03D35T
17	FO	SR_FO_BLK2_MODE	1	8	na	na	FIFO Blk2 mode status 0=read; 1=write	D	na	C000E	1	MM03D36T
17	FO	SR_FO_BLK3_MODE	1	8	na	na	FIFO Blk3 mode status 0=read; 1=write	D	na	C000E	2	MM03D37T
17	FO	SR_FO_BLK4_MODE	1	8	na	na	FIFO Blk4 mode status 0=read; 1=write	D	na	C000E	3	MM03D38T
2	FR	CR_FRA_EEP_WRE	1	8	na	na	FRA EEP write enable=0/disable=1 by Rcmd, disable by CP 1553	D	na	C0011	F	MM01D44T
2	FR	CR_FRB_EEP_WRE	1	8	na	na	FRB EEP write enable=0/disable=1 by Rcmd, disable by CP 1553	D	na	C0012	0	MM02D44T
	FR	CR_FR_A_ON	1	8	na	na	FR AON_BOFF=1, AOFF=0 by R cmd	D	na	C0011	D	MM01B05T
	FR	CR_FR_A_RESET	1	8	na	na	FR A or B reset=0, 1=running by D cmd	D	na	C0011	E	MM01D24T
	FR	CR_FR_B_ON	1	8	na	na	FR BON_AOFF=1, BOFF=0 by R cmd	D	na	C0012	2	MM02B05T
	FR	CR_FR_B_RESET	1	8	na	na	FR B reset=0, 1=running by D cmd	D	na	C0012	3	MM02D24T
45	FR	CS_FR_BBRADTAB	1	1	na	na	Normal/Test = 1/0 resp for cmd FR32	SW	na	na	na	na
	FR	CS_FR_DAY_RATE	1	8	NA	na	FR Day Rate=1; also in eng T30-5D	SW	na	na	na	na
23	FR	CS_FR_DELAY_BB	7	8	D#0-50	Col 7	FR BB View Delay D#0-50, 1=6.66µs, 0.02IFOV; also in eng T30-5D	SW	na	na	na	na
23	FR	CS_FR_DELAY_EA	7	8	D#0-50	Col 7	FR Earth View Delay D#0-50, 1=6.66µs, 0.02IFOV; also in eng T30-5D	SW	na	na	na	na
23	FR	CS_FR_DELAY_SD	7	8	D#0-50	Col 7	FR SD View Delay D#0-50, 1=6.66µs, 0.02IFOV; also in eng T30-5D	SW	na	na	na	na

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23	FR	CS_FR_DELAY_SP	7	8	D#0-50	Col 7	FR Space View Delay D#0-50, 1=6.66μs, 0.02IFOV; also in eng T30-5D	SW	na	na	na	na
23	FR	CS_FR_DELAY_SR	7	8	D#0-50	Col 7	FR SRCA View Delay D#0-50, 1=6.66μs, 0.02IFOV; also in eng T30-5D	SW	na	na	na	na
35	FR	CS_FR_ENC_DELTA	14	8	D#-8191 to +8192	Col 7	FR encoder delta by 2sComplement to all views normal count; relates global collect rotation	SW	na	na	na	na
45	FR	CS_FR_GAINTAB	1	1	na	na	Normal/Test = 1/0 resp for cmd FR34	SW	na	na	na	na
45	FR	CS_FR_OFFSETTAB	1	1	na	na	Normal/Test = 1/0 resp for cmd FR33	SW	na	na	na	na
49,66,72	FR	SS_FR_SCIABNORM	1	8	na	na	Gnd set flag for known SCI abnormality; 0=ABNORM, 1=NORM	SW	na	na	na	na
49,66	FR	FR_SPARE	1	8	na	na	Was CS_FR_PCDCRPOST	SW	na	na	na	na
49,66	FR	FR_SPARE	1	8	na	na	Was CS_FR_PCDCRPRE	SW	na	na	na	na
	FR	CS_FR_PC_DCR_ON	1	8	na	na	FR PC DCR ON=1; also in eng T30-5D,cmd FR29	SW	na	na	na	na
	FR	CS_FR_PV_DCR_ON	1	8	na	na	FR PV DCR ON=1; also in eng T30-5D,cmd FR27	SW	na	na	na	na
51	FR	CS_FR_SCI_NORMAL	1	8	Yes/No	na	Yes/No=1/0 AND-ED tlmy results from 18 Normal/Test cmds. See T10-25B & T20-2B for details	SW	na	na	na	na
	FR	SR_FR_A_MODELONG	1	8	na	na	FR A Mode Long=1; Short=0	D	na	C0011	C	MM01D21T
	FR	SR_FR_B_MODELONG	1	8	na	na	FR B Mode Long=1; Short=0	D	na	C0012	1	MM02D21T
43,64	FR	SS_FR_LAST_EVENT	16	1	na	na	Upper 8-bits provide 1-255 event count, lower 8-bits provide event code. See 152932 Flt SW Maintenance Manual for event codes.	SW	na	na	na	na
64	FR	SS_FR_LOG_EVENT	1	1	na	na	High indicates entry into FR event log; see SS_FR_LAST_EVENT for type event	SW	na			na
53	FR	SS_FR_LOG_STATE	4	8	D#0-15		D#(4 bits) Reflects OPERAND & INSTRUCTION class of loads/dumps	SW	na	na	na	na
	FR	SS_FR_RESET_SRC	3	8	na	na	FR Reset source: 000=PS, 001=FRA/FRB select, 010=FR Standard, 011= FR Upload, 100 - 111 invalid.	SW	na	na	na	na
46	FR	SS_FR_PKT_TYPE	1	8	na	na	FR Pkt Normal/Test=0/1. Test pattern to ck hi-rate link.	SW	na	na	na	na
54	FR	SS_FR_SPARE	1	8	na	na	Was SS_FR_MEMPRO_ERR	SW	na	na	na	na
54	FR	SS_FR_SPARE	1	8	na	na	Was SS_FR_PARITY_ERR	SW	na	na	na	na
54	FR	SS_FR_SPARE	1	8	na	na	Was SS_FR_TEST_RES	SW	na	na	na	na
	FR	TP_FR_A_ENGINE	9	65	-43 to +85°C	T20-6	Formatter A engine temp	P	U8	C0003/C0004	1F2B	MM01A01T
	FR	TP_FR_B_ENGINE	9	65	-43 to +85°C	T20-6	Formatter B engine temp	P	U8	C0003/C0004	1FAB	MM02A01T
	ME	TP_ME_CHAS_TOP	9	65	-43 to +85°C	T20-6	Top of MEM chassis temp towards rear	P	U8	C0003/C0004	192B	ME00A03T
	ME	TP_ME_NX_HTSINK	8	65	-50 to +78°C	T20-6	MEM temp -X heat sink	PS	na	na	na	ME00A01T
	ME	TP_ME_PSRADIATOR	8	65	-50 to +78°C	T20-6	PS1,PS2 radiator area temp, inside side panel near radiator)	PS	na	na	na	ME00A02T
71	ME	TP_ME_SPARE	8	65	-43 to +85°C	na	Was TP_ME_TB07; no thermistor & fixed 4.99KΩ out of practical range	PS	na	na	na	ME00A04T
	MF	TP_MF_CALBKHD_SR	9	65	-43 to +85°C	T20-6	MF inside temp: -X Cal blkhd below SRCA mnt	P	U8	C0003/C0004	19AB	MF00A03T
	MF	TP_MF_CVR_OP_SR	9	65	-43 to +85°C	T20-6	MF inside temp: -X cover opposite SRCA	P	U8	C0003/C0004	1B2B	MF00A06T
	MF	TP_MF_NAD_APT_NX	9	65	-43 to +85°C	T20-6	MF inside temp: NAD -X, center aperture baffle	P	U8	C0003/C0004	1EAB	MF00A13T
	MF	TP_MF_NAD_APT_NY	9	65	-43 to +85°C	T20-6	MF inside temp: NAD -X, -Y aperture baffle	P	U8	C0003/C0004	1CAB	MF00A09T
	MF	TP_MF_NX_AOBKHD	9	65	-43 to +85°C	T20-6	MF inside temp: +Z, -X pt of AO blkhd	P	U8	C0003/C0004	1A2B	MF00A04T
	MF	TP_MF_OB_BLKHD	8	65	-50 to +78°C	T20-6	MF inside temp: +Z, MID X pt of AO blkhd	PS	na	na	na	MF00A02T
	MF	TP_MF_PX_AOBKHD	9	65	-43 to +85°C	T20-6	MF inside temp: +Z, +X pt of AO blkhd	P	U8	C0003/C0004	1AAB	MF00A05T
	MF	TP_MF_SV_PORT	9	65	-43 to +85°C	T20-6	Misnamed, really internal MF, closer to AO BKHD mount	P	U8	C0003/C0004	1D2B	MF00A10T
	MF	TP_MF_TOP_BY_KM1	8	65	-43 to +85°C	T20-6	MF inside temp: top, by 1-axis KM1	PS	na	na	na	MF00A07T
	MF	TP_MF_TOP_BY_KM2	9	65	-43 to +85°C	T20-6	MF inside temp: top, by 2-axis KM2	P	U8	C0003/C0004	1C2B	MF00A08T
	MF	TP_MF_TOP_BY_KM3	8	65	-50 to +78°C	T20-6	MF inside temp: top, by 3-axis KM3	PS	na	na	na	MF00A01T

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	MF	TP_MF_YZ_CALBKHD	9	65	-43 to +85°C	T20-6	MF outside temp -Y,+Z corner of cal blkhd	P	U8	C0003/C0004	1DAB	MF00A11T
	MF	TP_MF_Z_BKHD_BB	9	65	-43 to +85°C	T20-6	MF inside temp: Mid zenith blkhd near BB	P	U8	C0003/C0004	1E2B	MF00A12T
	PC	CR_PCLWA_ECAL_ON	1	8	na	na	PC LWIR A ECAL ON=1, OFF=0 by R cmd	D	na	C000C	1	AF07D02T
	PC	CR_PCLWB_ECAL_ON	1	8	na	na	PC LWIR B ECAL ON=1, OFF=0 by R cmd	D	na	C000C	3	AF08D02T
	PC	CR_PCLW_A_ON	1	8	na	na	PC LWIR A ON=1, Off=0 by R cmd (independent of LWIR B)	D	na	C000C	0	AF07D01T
	PC	CR_PCLW_B_ON	1	8	na	na	PC LWIR B ON=1, Off=0 by R cmd (independent of LWIR A)	D	na	C000C	2	AF08D01T
62,68	PC	CS_PC_3132_SFALL	8	8	0 to 425µs	Col7	PC B31&B32 sample clock fall location, nominal =25µs; also in eng T30-4D; (fall is relative to next pixel clock); value is 8-bit cnt x 1.67µs	SW	na	na	na	na
62,68	PC	CS_PC_3132_SRISE	8	8	0 to 425µs	Col7	PC B31&B32 sample clock rise location, nominal=317µs; also in eng T30-4D; value is 8-bit cnt x 1.67µs	SW	na	na	na	na
62,68	PC	CS_PC_3334_SFALL	8	8	0 to 425µs	Col7	PC B33&B34 sample clock fall location, nominal=25µs; also in eng T30-4D; (fall is relative to next pixel clock); value is 8-bit cnt x 1.67µs	SW	na	na	na	na
62,68	PC	CS_PC_3334_SRISE	8	8	0 to 425µs	Col7	PC B33&B34 sample clock rise location, nominal=317µs; also in eng T30-4D; value is 8-bit cnt x 1.67µs	SW	na	na	na	na
62,68	PC	CS_PC_3536_SFALL	8	8	0 to 425µs	Col7	PC B35&B36 sample clock fall location, nominal =25µs; also in eng T30-4D; (fall is relative to next pixel clock); value is 8-bit cnt x 1.67µs	SW	na	na	na	na
62,68	PC	CS_PC_3536_SRISE	8	8	0 to 425µs	Col7	PC B35&B36 sample clock rise location, nominal=317µs; also in eng T30-4D; value is 8-bit cnt x 1.67µs	SW	na	na	na	na
	PC	TA_PC_B31_MUX	9	65	0 to +50°C	T20-5	FAM AF01 active A/B side mux temp	APC	U25	C0003/C0004	0070	AF01A01T
	PC	TA_PC_B32_MUX	9	65	0 to +50°C	T20-5	FAM AF02 active A/B side mux temp	APC	U25	C0003/C0004	00F0	AF02A01T
	PC	TA_PC_B33_MUX	9	65	0 to +50°C	T20-5	FAM AF03 active A/B side mux temp	APC	U25	C0003/C0004	0170	AF03A01T
	PC	TA_PC_B34_MUX	9	65	0 to +50°C	T20-5	FAM AF04 active A/B side mux temp	APC	U25	C0003/C0004	01F0	AF04A01T
	PC	TA_PC_B35_MUX	9	65	0 to +50°C	T20-5	FAM AF05 active A/B side mux temp	APC	U25	C0003/C0004	0270	AF05A01T
	PC	TA_PC_B36_MUX	9	65	0 to +50°C	T20-5	FAM AF06 active A/B side mux temp	APC	U25	C0003/C0004	02F0	AF06A01T
	PC	TP_PCFAM_RADIATR	8	65	-50 to +78°C	T20-6	FAM temp inside side panel near radiator	PS	na	na	na	FM00A01T
	PC	TP_PC_CLAM_MNT	9	65	-43 to +85°C	T20-6	Clam chassis near mount pt temp	P	U10	C0003/C0004	109B	AF00A02T
	PC	VR_PC_B31_GND	8	65	-2.5 to +2.5V	T20-5	Via FAM mux AF01	APC	U25	C0003/C0004	0070	AF01A01T
	PC	VR_PC_B31_RN12V	8	65	-15.0 to 0V	T20-5	Via FAM mux AF01	APC	U25	C0003/C0004	0070	AF01A01T
	PC	VR_PC_B31_RN5V	8	65	-7.5 to 0V	T20-5	Via FAM mux AF01	APC	U25	C0003/C0004	0070	AF01A01T
	PC	VR_PC_B31_RP12V	8	65	0 to +15.0V	T20-5	Via FAM mux AF01	APC	U25	C0003/C0004	0070	AF01A01T
	PC	VR_PC_B31_RP5V	8	65	0 to +7.5V	T20-5	Via FAM mux AF01	APC	U25	C0003/C0004	0070	AF01A01T
	PC	VR_PC_B32_GND	8	65	-2.5 to +2.5V	T20-5	Via FAM mux AF02	APC	U25	C0003/C0004	00F0	AF02A01T
	PC	VR_PC_B32_RN12V	8	65	-15.0 to 0V	T20-5	Via FAM mux AF02	APC	U25	C0003/C0004	00F0	AF02A01T
	PC	VR_PC_B32_RN5V	8	65	-7.5 to 0V	T20-5	Via FAM mux AF02	APC	U25	C0003/C0004	00F0	AF02A01T
	PC	VR_PC_B32_RP12V	8	65	0 to +15.0V	T20-5	Via FAM mux AF02	APC	U25	C0003/C0004	00F0	AF02A01T
	PC	VR_PC_B32_RP5V	8	65	0 to +7.5V	T20-5	Via FAM mux AF02	APC	U25	C0003/C0004	00F0	AF02A01T
	PC	VR_PC_B33_GND	8	65	-2.5 to +2.5V	T20-5	Via FAM mux AF03	APC	U25	C0003/C0004	0170	AF03A01T
	PC	VR_PC_B33_RN12V	8	65	-15.0 to 0V	T20-5	Via FAM mux AF03	APC	U25	C0003/C0004	0170	AF03A01T
	PC	VR_PC_B33_RN5V	8	65	-7.5 to 0V	T20-5	Via FAM mux AF03	APC	U25	C0003/C0004	0170	AF03A01T
	PC	VR_PC_B33_RP12V	8	65	0 to +15.0V	T20-5	Via FAM mux AF03	APC	U25	C0003/C0004	0170	AF03A01T
	PC	VR_PC_B33_RP5V	8	65	0 to +7.5V	T20-5	Via FAM mux AF03	APC	U25	C0003/C0004	0170	AF03A01T
	PC	VR_PC_B34_GND	8	65	-2.5 to +2.5V	T20-5	Via FAM mux AF04	APC	U25	C0003/C0004	01F0	AF04A01T
	PC	VR_PC_B34_RN12V	8	65	-15.0 to 0V	T20-5	Via FAM mux AF04	APC	U25	C0003/C0004	01F0	AF04A01T

TABLE 20-2A. MODIS TELEMETRY LIST

Sort by Subsystem - - End User Interest extends through Column 7 - - See Notes at table bottom - - Shaded area indicates S/C pt-pt processing. *5/97*

pfm chg#	1 Subsys	2 Mnemonic Name	3 # of Bits	4 Sample Period	5 Tlmy Range	6 Equations & Limits	7 Remarks	8 Tlmy Type	9 Analog Mux	10 HW Addr Write/Read	11 HW Data Loc	12 Design Unique ID
	PC	VR_PC_B34_RN5V	8	65	-7.5 to 0V	T20-5	Via FAM mux AF04	APC	U25	C0003/C0004	01F0	AF04A01T
	PC	VR_PC_B34_RP12V	8	65	0 to +15.0V	T20-5	Via FAM mux AF04	APC	U25	C0003/C0004	01F0	AF04A01T
	PC	VR_PC_B34_RP5V	8	65	0 to +7.5V	T20-5	Via FAM mux AF04	APC	U25	C0003/C0004	01F0	AF04A01T
	PC	VR_PC_B35_GND	8	65	-2.5 to +2.5V	T20-5	Via FAM mux AF05	APC	U25	C0003/C0004	0270	AF05A01T
	PC	VR_PC_B35_RN12V	8	65	-15.0 to 0V	T20-5	Via FAM mux AF05	APC	U25	C0003/C0004	0270	AF05A01T
	PC	VR_PC_B35_RN5V	8	65	-7.5 to 0V	T20-5	Via FAM mux AF05	APC	U25	C0003/C0004	0270	AF05A01T
	PC	VR_PC_B35_RP12V	8	65	0 to +15.0V	T20-5	Via FAM mux AF05	APC	U25	C0003/C0004	0270	AF05A01T
	PC	VR_PC_B35_RP5V	8	65	0 to +7.5V	T20-5	Via FAM mux AF05	APC	U25	C0003/C0004	0270	AF05A01T
	PC	VR_PC_B36_GND	8	65	-2.5 to +2.5V	T20-5	Via FAM mux AF06	APC	U25	C0003/C0004	02F0	AF06A01T
	PC	VR_PC_B36_RN12V	8	65	-15.0 to 0V	T20-5	Via FAM mux AF06	APC	U25	C0003/C0004	02F0	AF06A01T
	PC	VR_PC_B36_RN5V	8	65	-7.5 to 0V	T20-5	Via FAM mux AF06	APC	U25	C0003/C0004	02F0	AF06A01T
	PC	VR_PC_B36_RP12V	8	65	0 to +15.0V	T20-5	Via FAM mux AF06	APC	U25	C0003/C0004	02F0	AF06A01T
	PC	VR_PC_B36_RP5V	8	65	0 to +7.5V	T20-5	Via FAM mux AF06	APC	U25	C0003/C0004	02F0	AF06A01T
75	PS	CR_PS1SHDN_ENA_M	1	8	na	na	Via 1553 tlmy, PS1 shutdown enable=1, disable=0 by S/C R cmd, (enables 3 auto SHDNs); * * 'OFF' SIDE TLMY IS INVALID * *	D	na	C000C	8	PS01A17T
	PS	CR_PS1SHDN_ENA_S	1	8	na	na	Via S/C tlmy, PS1 shutdown enable=1 by S/C R cmd, (enables 3 auto SHDNs)	DS	na	na	na	PS01K05T
	PS	CR_PS1SRVHTR_ENA	1	8	na	na	PS1 Srv Htr A enable=1 by S/C R cmd (no tlmy for thermostat sw on)	DS	na	na	na	PS01K06T
	PS	CR_PS1_ON	1	8	na	na	PS1 ON=1 by S/C R cmd (both can be ON or OFF)	DS	na	na	na	PS01K02T
76	PS	CR_PS2SHDN_ENA_M	1	8	na	na	Via 1553 tlmy, PS1 shutdown enable=1, disable=0 by S/C R cmd, (enables 3 auto SHDNs); * * 'OFF' SIDE TLMY IS INVALID * *	D	na	C000C	F	PS02A17T
	PS	CR_PS2SHDN_ENA_S	1	8	na	na	Via S/C tlmy, PS2 shutdown enable=1 by S/C R cmd, (enables 3 auto SHDNs)	DS	na	na	na	PS02KO5T
	PS	CR_PS2SRVHTR_ENA	1	8	na	na	PS2 Srv Htr B enable=1 by S/C R cmd (no tlmy for thermostat sw on)	DS	na	na	na	PS02K06T
	PS	CR_PS2_ON	1	8	na	na	PS2 ON=1 by R cmd (both can be ON or OFF)	DS	na	na	na	PS02K02T
	PS	IR_PS1_INPUT_CUR	10	1	0 to 3.750A	T20-5	PS1 120V Bus A input current (3.2A/1024=3.125mA/b)	A	U30	C0003/C0004	6EF6	PS01A16T
5	PS	IR_PS2_INPUT_CUR	10	1	0 to 3.750A	T20-5	PS2 120V Bus B input current (3.2A/1024=3.125mA/b)	A	U31	C0003/C0004	76F7	PS02A16T
	PS	TP_PS1_CVTR_SW	9	65	-43 to +85°C	T20-6	PS01 temp at converter sws & output xfmr	P	U7	C0003/C0004	22BB	PS01A19T
	PS	TP_PS1_DIODE_OUT	9	65	-43 to +85°C	T20-6	PS01 temp at output diodes near rad wall	P	U7	C0003/C0004	233B	PS01A20T
	PS	TP_PS1_DWNREG_SW	9	65	-43 to +85°C	T20-6	PS01 temp at near rad wall shtdwn sens	P	U7	C0003/C0004	223B	PS01A18T
	PS	TP_PS1_PRELOAD	9	65	-43 to +85°C	T20-6	PS01 temp at preload resistor	P	U7	C0003/C0004	23BB	PS01A21T
	PS	TP_PS2_CVTR_SW	9	65	-43 to +85°C	T20-6	PS02 temp at converter sws & output xfmr	P	U7	C0003/C0004	263B	PS02A19T
	PS	TP_PS2_DIODE_OUT	9	65	-43 to +85°C	T20-6	PS02 temp at output diodes near rad wall	P	U7	C0003/C0004	26BB	PS02A20T
	PS	TP_PS2_DWNREG_SW	9	65	-43 to +85°C	T20-6	PS02 temp at near rad wall shtdwn sens	P	U7	C0003/C0004	25BB	PS02A18T
	PS	TP_PS2_PRELOAD	9	65	-43 to +85°C	T20-6	PS02 temp at preload resistor	P	U7	C0003/C0004	273B	PS02A21T
	PS	VR_PS1_N15V_A1ME	8	65	-20.4 to 0V	T20-5	PS1P04N -15.6V to MEM A1 rtn	A	U30	C0003/C0004	6978	PS01A05T
	PS	VR_PS1_N15V_A2AF	8	65	-20.4 to 0V	T20-5	PS01P05N -15.6V FAM A2 rtn	A	U30	C0003/C0004	6A79	PS01A07T
	PS	VR_PS1_N15V_A3AS	8	65	-20.4 to 0V	T20-5	PS01P06N -15.6V SAM A3 rtn	A	U30	C0003/C0004	6B7A	PS01A09T
	PS	VR_PS1_N30V_A1ME	8	65	-37.5 to 0V	T20-5	PS01P07N -30V MEM A1 rtn	A	U30	C0003/C0004	6C78	PS01A11T
	PS	VR_PS1_N8V_A2	8	65	-11.8 to 0V	T20-5	PS01P03N -8.5V FAM, SAM A2 rtn	A	U30	C0003/C0004	6E79	PS01A15T
	PS	VR_PS1_P15V_A1ME	8	65	0 to +20.4V	T20-5	PS1P04P +15.6V to MEM A1 rtn	A	U30	C0003/C0004	69F8	PS01A06T
	PS	VR_PS1_P15V_A2AF	8	65	0 to +20.4V	T20-5	PS01P05P +15.6V FAM A2 rtn	A	U30	C0003/C0004	6AF9	PS01A08T
	PS	VR_PS1_P15V_A3AS	8	65	0 to +20.4V	T20-5	PS01P06P +15.6V SAM A3 rtn	A	U30	C0003/C0004	6BFA	PS01A10T

TABLE 20-2A. MODIS TELEMETRY LIST

Sort by Subsystem - - End User Interest extends through Column 7 - - See Notes at table bottom - - Shaded area indicates S/C pt-pt processing.

5/97

pfm chg#	1 Subsys	2 Mnemonic Name	3 # of Bits	4 Sample Period	5 Tlmy Range	6 Equations & Limits	7 Remarks	8 Tlmy Type	9 Analog Mux	10 HW Addr Write/Read	11 HW Data Loc	12 Design Unique ID
	PS	VR_PS1_P30V_A1	8	65	0 to +37.5V	T20-5	PS01P07P +30V MEM A1 rtn	A	U30	C0003/C0004	6CF8	PS01A12T
73	PS	VR_PS1_P5_6V_D1	8	65	0 to +6.3V	T20-5	PS01P01P +5.6V all digital D1 rtn (upped to 5.8V for PF)	A	U30	C0003/C0004	687B	PS01A03T
	PS	VR_PS1_P88V_A1ME	8	65	0 to +124V	T20-5	PS01P08P +88V MEM A1 rtn OG V	A	U30	C0003/C0004	6D78	PS01A13T
	PS	VR_PS1_P8V_A2	8	65	0 to +11.8V	T20-5	PS01P03P +8.5V FAM, SAM A2 rtn	A	U30	C0003/C0004	6DF9	PS01A14T
	PS	VR_PS1_P8V_N1ME	8	65	0 to +11.8V	T20-5	PS01P02P +8.5V MEM N1 lamp rtn	A	U30	C0003/C0004	68F8	PS01A04T
	PS	VR_PS2_N15V_A1ME	8	65	-20.4 to 0V	T20-5	PS2P04N -15.6V to MEM A1 rtn	A	U31	C0003/C0004	717C	PS02A05T
	PS	VR_PS2_N15V_A2AF	8	65	-20.4 to 0V	T20-5	PS02P05N -15.6V FAM A2 rtn	A	U31	C0003/C0004	727D	PS02A07T
	PS	VR_PS2_N15V_A3AS	8	65	-20.4 to 0V	T20-5	PS02P06N -15.6V SAM A3 rtn	A	U31	C0003/C0004	737E	PS02A09T
	PS	VR_PS2_N30V_A1ME	8	65	-37.5 to 0V	T20-5	PS02P07N -30V MEM A1 rtn	A	U31	C0003/C0004	747C	PS02A11T
	PS	VR_PS2_N8V_A2	8	65	-11.8 to 0V	T20-5	PS02P03N -8.5V FAM, SAM A2 rtn	A	U31	C0003/C0004	767D	PS02A15T
	PS	VR_PS2_P15V_A1ME	8	65	0 to +20.4V	T20-5	PS2P04P +15.6V to MEM A1 rtn	A	U31	C0003/C0004	71FC	PS02A06T
	PS	VR_PS2_P15V_A2AF	8	65	0 to +20.4V	T20-5	PS02P05P +15.6V FAM A2 rtn	A	U31	C0003/C0004	72FD	PS02A08T
	PS	VR_PS2_P15V_A3AS	8	65	0 to +20.4V	T20-5	PS02P06P +15.6V SAM A3 rtn	A	U31	C0003/C0004	73FE	PS02A10T
	PS	VR_PS2_P30V_A1	8	65	0 to +37.5V	T20-5	PS02P07P +30V MEM A1 rtn	A	U31	C0003/C0004	74FC	PS02A12T
73	PS	VR_PS2_P5_6V_D1	8	65	0 to +6.3V	T20-5	PS02P01P +5.6V all digital D1 rtn (upped to 5.8V for PF)	A	U31	C0003/C0004	707F	PS02A03T
	PS	VR_PS2_P88V_A1ME	8	65	0 to +124V	T20-5	PS02P08P +88V MEM A1 rtn OG V	A	U31	C0003/C0004	757C	PS02A13T
	PS	VR_PS2_P8V_A2	8	65	0 to +11.8V	T20-5	PS02P03P +8.5V FAM, SAM A2 rtn	A	U31	C0003/C0004	75FD	PS02A14T
	PS	VR_PS2_P8V_N1ME	8	65	0 to +11.8V	T20-5	PS02P02P +8.5V MEM N1 lamp rtn	A	U31	C0003/C0004	70FC	PS02A04T
	PV	CR_PVLWA_CSUB_ON	1	8	na	na	PV LWIR A CSUB ON=1 by D cmd	D	na	C000F	8	AS07G03T
	PV	CR_PVLWA_ECAL_ON	1	8	na	na	PV LWIR A ECAL On=1 by D cmd	D	na	C000C	A	AS07,09G02
	PV	CR_PVLWB_CSUB_ON	1	8	na	na	PV LWIR B CSUB ON=1 by D cmd	D	na	C000F	9	AS19G03T
	PV	CR_PVLWB_ECAL_ON	1	8	na	na	PV LWIR B ECAL On=1 by D cmd	D	na	C000D	3	AS19G02T
	PV	CR_PVLW_A_ON	1	8	na	na	PV LWIR AON_BOFF=1 by R cmd	D	na	C000C	9	AS07G01T
	PV	CR_PVLW_B_ON	1	8	na	na	PV LWIR BON_AOFF=1 by R cmd	D	na	C000D	2	AS19G01T
21,26,68	PV	CR_PVLW_S_DELAYH	8	8	0 to 210μs	T20-5	PV LWIR registration delay of A_4 or B_10 C&B-ACE pwb; also in eng T30-5D	SW	na	na	na	na
	PV	CR_PVNIRA_ECALON	1	8	na	na	PV NIR A ECAL ON=1 by D cmd, off=0	D	na	C000C	7	AS03G02T
	PV	CR_PVNIRB_ECALON	1	8	na	na	PV NIR B ECAL ON=1 by D cmd, off=0	D	na	C000D	1	AS15G02T
	PV	CR_PVNIR_A_ON	1	8	na	na	PV NIR AON_BOFF=1 by R cmd	D	na	C000C	6	AS03G01T
	PV	CR_PVNIR_B_ON	1	8	na	na	PV NIR BON_AOFF=1 by R cmd	D	na	C000D	0	AS15G01T
21,26,68	PV	CR_PVNIR_S_DELYH	8	8	0 to 210μs	T20-5	PV NIR registration sample delay of A_2 or B_8 C&B-ACE pwb; also in eng T30-5D	SW	na	na	na	na
	PV	CR_PVSMA_CSUB_ON	1	8	na	na	PV SMIR A Chrg Subtraction On=1, Off=0 by D cmd	D	na	C000F	A	AS09G03T
	PV	CR_PVSMA_ECAL_ON	1	8	na	na	PV SMIR A Electronic Cal On=1, Off=0 by D cmd	D	na	C000C	C	AS09G02T
	PV	CR_PVSMB_CSUB_ON	1	8	na	na	PV SMIR B Chrg Subtraction On=1, Off=0 by D cmd	D	na	C000F	B	AS21G03T
	PV	CR_PVSMB_ECAL_ON	1	8	na	na	PV SMIR B Electronic Cal On=1, Off=0 by D cmd	D	na	C000D	5	AS21G02T
	PV	CR_PVSM_A_ON	1	8	na	na	PV SMIR AON_BOFF=1, AOFF=0 by R cmd	D	na	C000C	B	AS09G01T
	PV	CR_PVSM_B_ON	1	8	na	na	PV SMIR BON_AOFF=1, BOFF=0 by R cmd	D	na	C000D	4	AS21G01T
21,26,68	PV	CR_PVSM_S_DELAYH	8	8	0 to 210μs	T20-5	PV SMIR registration sample delay of A_5 or B_11 C&B pwb; also in eng T30-5D	SW	na	na	na	na
	PV	CR_PVVISA_ECALON	1	8	na	na	PV VIS A Electronic Cal On=1, Off=0 by D cmd	D	na	C000C	5	AS01G02T
63	PV	CR_PVVISB_ECALON	1	8	na	na	PV VIS B Electronic Cal On=1, Off=0 by D cmd	D	na	C000C	E	AS13G02T

TABLE 20-2A. MODIS TELEMETRY LIST

Sort by Subsystem - - End User interest extends through Column 7 - - See Notes at table bottom - - Shaded area indicates S/C pt-pt processing. *5/97*

pfm chg#	1 Subsys	2 Mnemonic Name	3 # of Bits	4 Sample Period	5 Tlmy Range	6 Equations & Limits	7 Remarks	8 Tlmy Type	9 Analog Mux	10 HW Addr Write/Read	11 HW Data Loc	12 Design Unique ID
	PV	CR_PVVIS_A_ON	1	8	na	na	PV VIS AON_BOFF=1, AOFF=0 by R cmd	D	na	C000C	4	AS01G01T
63	PV	CR_PVVIS_B_ON	1	8	na	na	PV VIS BON_AOFF=1, BOFF=0 by R cmd	D	na	C000C	D	AS13G01T
21,26,68	PV	CR_PVVIS_S_DELYH	8	8	0 to 210µs	T20-5	PV VIS registration sample delay of A_1 or B_7 C&B-ACE pwb; also in eng T30-5D	SW	na	na	na	na
	PV	CR_PV_A_MEM_RAM	1	8	na	na	PV A MEM SET to RAM=1, ROM=0 by D cmd same logic	D	na	C0012	6	AS10G03T
	PV	CR_PV_B_MEM_RAM	1	8	na	na	PV B MEM SET to RAM=1, ROM=0 by D cmd same logic	D	na	C0012	7	AS22G03T
75	PV	CR_PV_ECAL_ENA_A	1	8	na	na	Elec Cal A for all PV Enabled=1, Disabled=0 by D cmd, both A&B have same state (also chrg subtraction for SMIR & LWIR)	D	na	C000D	6	AS10G04T
75	PV	CR_PV_ECAL_ENA_B	1	8	na	na	Elec Cal B for all PV Enabled=1, Disabled=0 by D cmd, both A&B have same state (also chrg subtraction for SMIR & LWIR)	D	na	C000D	7	AS22G04T
	PV	TA_PVLW_PWB4_10	9	65	10 to 65°C	T20-5	PV LWIR temp of A_4 or B_10 C&B-ACE pwb SAM mux	APV	U25	C0003/C0004	0371	AS10A02,03T
	PV	TA_PVNIR_PWB2_8	9	65	10 to 65°C	T20-5	PV NIR Temp of A_2 or B_8 C&B-ACE pwb SAM mux	APV	U25	C0003/C0004	0371	AS10A02,03T
	PV	TA_PVNIR_PWB3_9	9	65	10 to 65°C	T20-5	PV NIR Temp of A_3 or B_9 ACE-ACE pwb SAM mux	APV	U25	C0003/C0004	0371	AS10A02,03T
	PV	TA_PVSM_PWB5_11	9	65	10 to 65°C	T20-5	PV SMIR Temp of A_5 or B_11 C&B pwb SAM mux	APV	U25	C0003/C0004	0371	AS10A02,03T
	PV	TA_PVSM_PWB6_12	9	65	10 to 65°C	T20-5	PV SMIR Temp of A_6 or B_12 ACE-ACE pwb SAM mux	APV	U25	C0003/C0004	0371	AS10A02,03T
	PV	TA_PVVIS_PWB1_7	9	65	10 to 65°C	T20-5	PV VIS Temp of A_1 or B_7 C&B-ACE pwb SAM mux	APV	U25	C0003/C0004	0371	AS10A02,03T
	PV	TP_PVSAM_RADIATR	8	65	-50 to +78°C	T20-5	PV SAM temp inside side panel near radiator	PS	na	na	na	SM00A01T
21	PV	VR_PVLW_P30V	8	65	-35.8 to +35.8V	T20-5	PV LWIR +30V of A_4 or B_10 C&B-ACE pwb SAM mux	APV	U25	C0003/C0004	0371	AS10A02,03T
21	PV	VR_PVLW_RN11V	8	65	-12.5 to +12.5V	T20-5	PV LWIR regulated -11V of A_4 or B_10 C&B-ACE pwb SAM mux	APV	U25	C0003/C0004	0371	AS10A02,03T
21	PV	VR_PVLW_RN5V	8	65	-5.6 to +5.6V	T20-5	PV LWIR regulated -5V of A_4 or B_10 C&B-ACE pwb SAM mux	APV	U25	C0003/C0004	0371	AS10A02,03T
21	PV	VR_PVLW_RP11V	8	65	-12.5 to +12.5V	T20-5	PV LWIR regulated +11V of A_4 or B_10 C&B-ACE pwb SAM mux	APV	U25	C0003/C0004	0371	AS10A02,03T
21	PV	VR_PVLW_RP5V	8	65	-5.6 to +5.6V	T20-5	PV LWIR regulated +5V of A_4 or B_10 C&B-ACE pwb SAM mux	APV	U25	C0003/C0004	0371	AS10A02,03T
	PV	VR_PVLW_VCALH	8	8	-10 to +10V	T20-5	PV LWIR VCAL(ECAL)bias A_4/B_10 C&B-ACE pwb;also in eng T30-5D	SW	na	na	0371	AS10A02,03T
21	PV	VR_PVNIR_P30V	8	65	-35.8 to +35.8V	T20-5	PV NIR +30V of A_2 or B_8 C&B-ACE pwb SAM mux	APV	U25	C0003/C0004	0371	AS10A02,03T
21	PV	VR_PVNIR_P5VD3_9	8	65	-5.6 to +5.6V	T20-5	PV NIR digital +5V of A_3 or B_9 ACE-ACE pwb SAM mux	APV	U25	C0003/C0004	0371	AS10A02,03T
21	PV	VR_PVNIR_RN11V28	8	65	-12.5 to +12.5V	T20-5	PV NIR regulated -11V of A_2 or B_8 C&B-ACE pwb SAM mux	APV	U25	C0003/C0004	0371	AS10A02,03T
21	PV	VR_PVNIR_RN11V39	8	65	-12.5 to +12.5V	T20-5	PV NIR regulated -11V of A_3 or B_9 ACE-ACE pwb SAM mux	APV	U25	C0003/C0004	0371	AS10A02,03T
21	PV	VR_PVNIR_RN5V2_8	8	65	-5.6 to +5.6V	T20-5	PV NIR regulated -5V of A_2 or B_8 C&B-ACE pwb SAM mux	APV	U25	C0003/C0004	0371	AS10A02,03T
21	PV	VR_PVNIR_RN5V3_9	8	65	-5.6 to +5.6V	T20-5	PV NIR regulated -5V of A_3 or B_9 ACE-ACE pwb SAM mux	APV	U25	C0003/C0004	0371	AS10A02,03T
21	PV	VR_PVNIR_RP11V28	8	65	-12.5 to +12.5V	T20-5	PV NIR regulated +11V of A_2 or B_8 C&B-ACE pwb SAM mux	APV	U25	C0003/C0004	0371	AS10A02,03T
21	PV	VR_PVNIR_RP11V39	8	65	-12.5 to +12.5V	T20-5	PV NIR regulated +11V of A_3 or B_9 ACE-ACE pwb SAM mux	APV	U25	C0003/C0004	0371	AS10A02,03T
21	PV	VR_PVNIR_RP5V2_8	8	65	-5.6 to +5.6V	T20-5	PV NIR regulated +5V of A_2 or B_8 C&B-ACE pwb SAM mux	APV	U25	C0003/C0004	0371	AS10A02,03T
21	PV	VR_PVNIR_RP5V3_9	8	65	-5.6 to +5.6V	T20-5	PV NIR regulated +5V of A_3 or B_9 ACE-ACE pwb SAM mux	APV	U25	C0003/C0004	0371	AS10A02,03T
21	PV	VR_PVNIR_VCALH	8	8	-10 to +10V	T20-5	PV NIR VCAL(ECAL) bias A_2 /B_8 C&B-ACE pwb;also in eng T30-5D	SW	na	na	na	na
21	PV	VR_PVSM_P30V	8	65	-35.8 to +35.8V	T20-5	PV SMIR +30V of A_5 or B_11 C&B pwb SAM mux	APV	U25	C0003/C0004	0371	AS10A02,03T
21	PV	VR_PVSM_P5VD6_12	8	65	-5.6 to +5.6V	T20-5	PV SMIR digital +5V of A_6 or B_12 ACE-ACE pwb SAM mux	APV	U25	C0003/C0004	0371	AS10A02,03T
21	PV	VR_PVSM_RN11V511	8	65	-12.5 to +12.5V	T20-5	PV SMIR regulated -11V of A_5 or B_11 C&B pwb SAM mux	APV	U25	C0003/C0004	0371	AS10A02,03T
21	PV	VR_PVSM_RN11V612	8	65	-12.5 to +12.5V	T20-5	PV SMIR regulated -11V of A_6 or B_12 ACE-ACE pwb SAM mux	APV	U25	C0003/C0004	0371	AS10A02,03T
21	PV	VR_PVSM_RN5V5_11	8	65	-5.6 to +5.6V	T20-5	PV SMIR regulated -5V of A_5 or B_11 C&B pwb SAM mux	APV	U25	C0003/C0004	0371	AS10A02,03T
21	PV	VR_PVSM_RN5V6_12	8	65	-5.6 to +5.6V	T20-5	PV SMIR regulated -5V of A_6 or B_12 ACE-ACE pwb SAM mux	APV	U25	C0003/C0004	0371	AS10A02,03T
21	PV	VR_PVSM_RP11V511	8	65	-12.5 to +12.5V	T20-5	PV SMIR regulated +11V of A_5 or B_11 C&B pwb SAM mux	APV	U25	C0003/C0004	0371	AS10A02,03T

TABLE 20-2A. MODIS TELEMETRY LIST

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pfm chg#	1 Subsys	2 Mnemonic Name	3 # of Bits	4 Sample Period	5 Tlmy Range	6 Equations & Limits	7 Remarks	8 Tlmy Type	9 Analog Mux	10 HW Addr Write/Read	11 HW Data Loc	12 Design Unique ID
21	PV	VR_PVSM_RP11V612	8	65	-12.5 to +12.5V	T20-5	PV SMIR regulated +11V of A_6 or B_12 ACE-ACE pwb SAM mux	APV	U25	C0003/C0004	0371	AS10A02,03T
21	PV	VR_PVSM_RP5V5_11	8	65	-5.6 to +5.6V	T20-5	PV SMIR regulated +5V of A_5 or B_11 C&B pwb SAM mux	APV	U25	C0003/C0004	0371	AS10A02,03T
21	PV	VR_PVSM_RP5V6_12	8	65	-5.6 to +5.6V	T20-5	PV SMIR regulated +5V of A_6 or B_12 ACE-ACE pwb SAM mux	APV	U25	C0003/C0004	0371	AS10A02,03T
	PV	VR_PVSM_VCALH	8	8	-10 to +10V	T20-5	PV SMIR VCAL(ECAL) bias A_5/B_11 C&B pwb;also in eng T30-5D	SW	na	na	na	na
21	PV	VR_PVVIS_P30V	8	65	-35.8 to +35.8V	T20-5	PV VIS +30V of A_1 or B_7 C&B-ACE pwb SAM mux	APV	U25	C0003/C0004	0371	AS10A02,03T
21	PV	VR_PVVIS_RN11V	8	65	-12.5 to +12.5V	T20-5	PV VIS regulated -11V of A_1 or B_7 C&B-ACE pwb SAM mux	APV	U25	C0003/C0004	0371	AS10A02,03T
21	PV	VR_PVVIS_RN5V	8	65	-5.6 to +5.6V	T20-5	PV VIS regulated -5V of A_1 or B_7 C&B-ACE pwb SAM mux	APV	U25	C0003/C0004	0371	AS10A02,03T
21	PV	VR_PVVIS_RP11V	8	65	-12.5 to +12.5V	T20-5	PV VIS regulated +11V of A_1 or B_7 C&B-ACE pwb SAM mux	APV	U25	C0003/C0004	0371	AS10A02,03T
21	PV	VR_PVVIS_RP5V	8	65	-5.6 to +5.6V	T20-5	PV VIS regulated +5V of A_1 or B_7 C&B-ACE pwb SAM mux	APV	U25	C0003/C0004	0371	AS10A02,03T
	PV	VR_PVVIS_VCALH	8	8	-10 to +10V	T20-5	PV VIS VCAL(ECAL) bias A_1/B_7 C&B-ACE pwb;also in eng T30-5D	SW	na	na	na	na
37	RC	TP_RC_SPARE	12	65	-130 to +60°C	T20-6	Was Outerstage fin temp	P	PP	C0003/C0004	396B	RC00A02T
	RC	CR_RC_CFPA_T1SET	1	8	na	na	RC CFPA Htr (both SMIR&LWIR) T1 set=1 by R cmd, no direct T2 tlmy	D	na	C000F	0004	MM11D09T
	RC	CR_RC_CFPA_T3SET	1	8	na	na	RC CFPA Htr (both SMIR&LWIR) T3 set=1 by R cmd, no direct T2 tlmy	D	na	C000F	0005	MM11D10T
oasis67	RC	CR_RC_CFPA_SETPT	2	8	83,85,88K	Col 7	RC CFPA Tlmy OASIS composite of T1&T3: =83K if T1=1&T3=0; =85K if T1=0 & T3=0; =88K if T1=0 & T3=1	SW	na	na	na	na
	RC	CR_RC_CSHTR_ON	1	8	na	na	RC cold stage OG htr ON=1, Off=0 by R cmd	D	na	C000F	0	MM11D01T
	RC	CR_RC_CSTLM_ON	1	8	na	na	RC cold stage tlmy ON=1, Off=0 by R cmd	D	na	C000F	1	MM11D03T
	RC	CR_RC_ISHTR_ON	1	8	na	na	RC intermediate stage OG htr ON=1, Off=0 by R cmd	D	na	C000F	6	MM11D11T
	RC	CR_RC_ISTLM_ON	1	8	na	na	RC intermediate stage tlmy ON=1, Off=0 by R cmd	D	na	C000F	7	MM11D13T
	RC	CR_RC_LWHTR_ON	1	8	na	na	LWIR FPA Htr ON=1, Off=0 by R cmd	D	na	C000F	E	MM11D19T
	RC	CR_RC_LWTLM_ON	1	8	na	na	LWIR FPA Tlmy ON=1, Off=0 by R cmd	D	na	C000F	F	MM11D21T
	RC	CR_RC_OSHTR_ON	1	8	na	na	RC outer stage OG htr ON=1, Off=0 by R cmd	D	na	C000F	2	MM11D05T
	RC	CR_RC_OSTLM_ON	1	8	na	na	RC outer stage tlmy ON=1, Off=0 by R cmd	D	na	C000F	3	MM11D07T
	RC	CR_RC_SMHTR_ON	1	8	na	na	SMIR FPA Htr ON=1, Off=0 by R cmd	D	na	C000F	C	MM11D16T
	RC	CR_RC_SMTLM_ON	1	8	na	na	SMIR FPA Tlmy ON=1, Off=0 by R cmd	D	na	C000F	D	MM11D17T
21	RC	TA_RC_CS	12	65	50K TO 110K	T20-5	RC cold stage temp, uses CS outgas PRT	A	U29	C0003/C0004	64F5	MM11A50T
	RC	TA_RC_CS_OG	12	65	53K to 361K	T20-5	RC Coldstage outgas temp by PRT	A	U28	C0003/C0004	5BF5	MM11A03T
21	RC	TA_RC_IS	12	65	90K to 170K	T20-5	RC intermediate stage temp,Uses IS outgas PRT	A	U29	C0003/C0004	6575	MM11A51T
	RC	TA_RC_IS_OG	12	65	53K to 361K	T20-5	Interstage outgas PRT temp	A	U28	C0003/C0004	5CF5	MM11A09T
	RC	TA_RC_LWIR_CFPA	12	1	82K to 88K	T20-5	RC LWIR FPA temp; range shifts with set point	A	U28	C0003/C0004	5E75	MM11A23T
	RC	TA_RC_OS_OG	12	65	53K to 361K	T20-5	Outerstage outgas PRT temp	A	U29	C0003/C0004	63F5	MM11A47T
	RC	TA_RC_SMIR_CFPA	12	1	60K to 100K	T20-5	RC SMIR FPA temp; fixed range temp	A	U28	C0003/C0004	5DF5	MM11A21T
	RC	TP_RC_MNT_RING	12	65	-43 to +85°C	T20-6	Mount ring temp	P	U11	C0003/C0004	33DB	RC00A07T
4	RC	TP_RC_SPARE	12	65	na	na	Was TP_RC_OS_WH (PRT)	P	PP	C0003/C0004	39EB	na
13,32	RC	VR_RC_LW_FPA_HTR	10	65	0 to +15V	T20-5	RC via Temp Cntlr LWIR FPA htr +V (I=V/1kΩ)	A	U29	C0003/C0004	6075	MM11A39T
13,32	RC	VR_RC_SM_FPA_HTR	10	65	0 to +15V	T20-5	RC via Temp Cntlr SMIR FPA htr +V (I=V/1kΩ)	A	U29	C0003/C0004	65F5	MM11A37T
2	SA	CR_SA_A_HI_GAIN	1	8	na	na	Scan Assy A Hi Gain=0, Lo=1 by R cmd (high gain is normal)	D	na	C000E	8	MM07D08T
	SA	CR_SA_A_SCAN_ON	1	8	na	na	Scan Assy A On=1, Off=0 by R cmd	D	na	C000E	6	MM07D03T
2	SA	CR_SA_B_HI_GAIN	1	8	na	na	Scan Assy B Hi Gain=0, Lo=1 by R cmd (high gain is normal)	D	na	C000E	B	MM08D08T
	SA	CR_SA_B_SCAN_ON	1	8	na	na	Scan Assy B On=1, Off=0 by R cmd	D	na	C000E	9	MM08D03T

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pfm chg#	1 Subsys	2 Mnemonic Name	3 # of Bits	4 Sample Period	5 Tlmy Range	6 Equations & Limits	7 Remarks	8 Tlmy Type	9 Analog Mux	10 HW Addr Write/Read	11 HW Data Loc	12 Design Unique ID
21,76	SA	IR_SA_A_ECDR_LED	12	65	0 to 75mA	T20-5	Scan Assy A mtr encoder LED current	A	U27	C0003/C0004	50F0	MM07A11T
21,76	SA	IR_SA_B_ECDR_LED	12	65	0 to 75mA	T20-5	Scan Assy B mtr encoder LED current	A	U27	C0003/C0004	5371	MM08A11T
	SA	SD_SA_APX_PERIOD	12	1	0 to 4095ms	Col 7	Scan Assy approx scan period; integer nominal=1477ms=X#5C5; spec 1477.165±1.5ms	SW	na	na	na	na
	SA	SR_SA_A_PH_LOCK	1	8	na	na	Scan Assy A Ph Locked=1, Not Locked=0 (S/B~1 sec after On)	D	na	C000E	7	MM07D07T
	SA	SR_SA_B_PH_LOCK	1	8	na	na	Scan Assy B Ph Locked=1, Not Locked=0 (S/B~1 sec after On)	D	na	C000E	A	MM08D07T
	SA	TP_SA_A_MTR	9	65	-43 to +85°C	T20-6	Scan mtr temp A	P	U11	C0003/C0004	345B	SA00A02T
59	SA	TP_SA_SPARE	12	65	-43 to +85°C	T20-6	Was: TP_SA_RCT1_HSG Scan Assy mirror radiative temp monitor support base temp1	P	U11	C0003/C0004	35DB	SA00A04T
21	SA	TP_SA_RCT1_MIR	12	65	-43 to +85°C	T20-6	Scan Assy mirror radiatively coupled temp 1 monitor	P	U11	C0003/C0004	365B	SA00A05T
59	SA	TP_SA_SPARE	12	65	-43 to +85°C	T20-6	Was: TP_SA_RCT2_HSG Scan Assy mirror radiative temp monitor support base temp2	P	U11	C0003/C0004	36DB	SA00A06T
21	SA	TP_SA_RCT2_MIR	12	65	-43 to +85°C	T20-6	Scan Assy mirror radiatively coupled temp 2 monitor	P	U11	C0003/C0004	375B	SA00A07T
76	SA	VR_SA_A_ECDR_MON	12	65	0 to +2.5V	T20-5	Scan Assy A mtr encoder photo detector signal	A	U27	C0003/C0004	5270	MM07A20T
31	SA	VR_SA_A_MTR_TORQ	10	65	0 to 47.4 IN OZ	T20-5	Scan Assy servo A Mtr torque = B#	A	U27	C0003/C0004	5070	MM07A01T
	SA	VR_SA_A_RN11V	8	65	-12.5 to 0V	T20-5	Scan Assy A servo regulated -11V	A	U27	C0003/C0004	51F0	MM07A15T
	SA	VR_SA_A_RP11V	8	65	0 to +12.5V	T20-5	Scan Assy A servo regulated +11V	A	U27	C0003/C0004	5170	MM07A13T
76	SA	VR_SA_B_ECDR_MON	12	65	0 to +2.5V	T20-5	Scan Assy B mtr encoder photo detector signal	A	U27	C0003/C0004	54F1	MM08A20T
31	SA	VR_SA_B_MTR_TORQ	10	65	0 to 47.4 IN OZ	T20-5	Scan Assy servo B Mtr torque = B#	A	U27	C0003/C0004	52F1	MM08A01T
	SA	VR_SA_B_RN11V	8	65	-12.5 to 0V	T20-5	Scan Assy B servo regulated -11V	A	U27	C0003/C0004	5471	MM08A15T
	SA	VR_SA_B_RP11V	8	65	0 to +12.5V	T20-5	Scan Assy B servo regulated +11V	A	U27	C0003/C0004	53F1	MM08A13T
36	SD	TP_SD_SPARE	9	65	-43 to +85°C	na	Deleted on PF, was Solar diffuser temp	P	U10	C0003/C0004	111B	CE02A01T
33	SM	CR_SM_MIR_HOME_A	1	1	na	na	SDSM Mirror Home A=0/Not=1 (see Note 11); Home=DCR view	DCE	na	C0001	6	na
33	SM	CR_SM_MIR_HOME_B	1	1	na	na	SDSM Mirror Home B=0/Not=1 (see Note 11); Home=DCR view	DCE	na	C0001	7	na
	SM	CR_SM_SDSM_A_ON	1	8	na	na	SDSM AON_BOFF=1, AOFF=0 by R cmd	D	na	40005	C	MM09D24T
	SM	CR_SM_SDSM_B_ON	1	8	na	na	SDSM BON_AOFF=1, BOFF=0 by R cmd	D	na	40005	D	MM09D25T
52	SM	CS_SM_MIR_STEP	7	1	D# 0-95 steps	na	SDSM Mirror mtr absolute step count=D#(7 bits), max=58; (3.75°/step); 0 step=SD, 29 steps=DCR (tlmy Home), 58 steps=Sun; relative steps can rotate 360° & increase step count; similar pt in eng T30-5D	SW	na	na	na	na
21,25	SM	TP_SM_DET_AMP3	9	65	-43 to +85°C	T20-6	SDSM temp at det amp 3 board	P	U10	C0003/C0004	151B	CE04A01T
	SR	CR_SR_A_ON	1	8	na	na	SRCA AON_BOFF=1, AOFF=0 by R cmd	D	na	40005	A	MM09D22T
	SR	CR_SR_B_ON	1	8	na	na	SRCA BON_AOFF=1, BOFF=0 by R cmd	D	na	40005	B	MM09D23T
	SR	CR_SR_GRAT_CH_A	1	1	na	na	SRCA Grating/Mirror Coarse Home A=0/Not=1 (see Note 12 &10.8.9.c)	DCE	na	C0001	8	na
48	SR	CR_SR_GRAT_CH_B	1	1	na	na	SRCA Grating/Mirror Coarse Home B=0/Not=1 (see Note 12 &10.8.9.c)	DCE	na	C0001	C	na
4	SR	CR_SR_GRAT_FH_A	1	1	na	na	SRCA Grating/Mirror Fine Home A=0/Not=1(see Note 12 & 10.8.9.c)	DCE	na	C0001	9	na
	SR	CR_SR_GRAT_FH_B	1	1	na	na	SRCA Grating/Mirror Fine Home B=0/Not=1 (see Note 12 & 10.8.9.c)	DCE	na	C0001	D	na
48	SR	CR_SR_IR_SRC_OFF	1	1	na	na	SRCA IR Source ON/OFF = 0/1 , (see Note 12)	DCE	na	C0001	1	na
41,46,75	SR	CR_SR_LAMPS_LOW	1	8	na	na	SRCA Lamp Level High/Low = 1/0; High is normal; Low might be used near end of life	SW	na	na	na	na
38	SR	CR_SR_L_SHDN_ENA	1	8	na	na	SRCA SIS LAMP overvoltage Enabled/Disabled=0/1 (see Note 12)	DCE	na	C0001	4	na
	SR	CR_SR_SISFB_RAD	1	8	na	na	SRCA SIS feedback control to Rad/Current=0/1 (see Note 12)	DCE	na	C0001	3	na
46	SR	CR_SR_SISHTR_OFF	1	1	na	na	SRCA SIS det Htr ON/OFF=0/1 (see Note 12)	DCE	na	C0001	2	na
	SR	CR_SR_SLIT_HOMEA	1	1	na	na	SRCA Slit Home A=0/Not Home=1 (see Note 12)	DCE	na	C0001	A	na

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pfm chg#	1 Subsys	2 Mnemonic Name	3 # of Bits	4 Sample Period	5 Tlmy Range	6 Equations & Limits	7 Remarks	8 Tlmy Type	9 Analog Mux	10 HW Addr Write/Read	11 HW Data Loc	12 Design Unique ID
	SR	CR_SR_SLIT_HOMEB	1	1	na	na	SRCA Slit Home B=0/Not Home=1 (see Note 12)	DCE	na	C0001	E	na
	SR	CR_SR_WHL_HOMEA	1	1	na	na	SRCA Source Wheel Home A=0/Not Home=1 (see Note 12)	DCE	na	C0001	B	na
	SR	CR_SR_WHL_HOMEB	1	1	na	na	SRCA Source Wheel Home B=0/Not Home=1 (see Note 12)	DCE	na	C0001	F	na
52	SR	CS_SR_GRAT_STEP	16	1	D# 0-61199 steps	Col 7	Grating/Mirror mtr absolute step count=D#(16bits), max=61199; (~0.006°/step); Home=Mirror=0 step; can rotate 360°; also in T30-5D	SW	na	na	na	na
39,75	SR	CS_SR_LAMPS	3	1	OFF/1W/10W/ 20W/30W	Col 7	OFF/WATT_ONE/WATT10/WATT20/WATT30 = 000/001/010 /011/100	SW	na	na	na	na
52,69	SR	CS_SR_SLIT_STEP	6	1	D# 0 - 48 steps	Col 7	Slit mtr absolute step=D#(6 bits), max=48; (3.75°/step); 0 step=Along Track Reticle, 24 steps=Along Scan Reticle (tlmy Home), 48 steps=Slit Reticle; hard stops just beyond 0 & 48 steps; also in eng T30-5D	SW	na	na	na	na
52	SR	CS_SR_SRCWH_STEP	7	1	D# 0 - 119 steps	Col 7	Filter Wheel mtr absolute step=D#(7 bits), max=100; (3°/step); 0 step=ND Filter, 20 steps=Open (tlmy Home), 40 steps=Order Filt#1, 60 steps=Order Flt#2, 80 steps=Order Filr#3, 100 steps=Beamcombiner; rel steps can rotate 360°; similar pt in eng T30-5D	SW	na	na	na	na
40	SR	CS_SR_USE_L10WX1	4	8	1 of 4	Col 7	SRCA 10WX1 lamp use with B#1/0 for ea bit for lamps 1,2,3,4	SW	na	na	na	na
40	SR	CS_SR_USE_L10WX2	4	8	2 of 4	Col 7	SRCA 10WX2 lamp use with B#1/0 for ea bit for lamps 1,2,3,4	SW	na	na	na	na
40	SR	CS_SR_USE_L10WX3	4	8	3 of 4	Col 7	SRCA 10WX3 lamp use with B#1/0 for ea bit for lamps 1,2,3,4	SW	na	na	na	na
40	SR	CS_SR_USE_L1WX1	2	8	1 of 2	Col 7	SRCA 1WX1 lamp with B#1/0 ea AB from lamps 5,6	SW	na	na	na	na
21	SR	IR_SR_10WLA_CURH	12	8	tbd	T20-5	SRCA 10W Lamp Current_A=B#, also in eng T30-5D	SW	na	na	58F3	MM10A02T
21	SR	IR_SR_10WLB_CURH	12	8	tbd	T20-5	SRCA 10W Lamp Current_B=B#, also in eng T30-5D	SW	na	na	5A73	MM10A05T
21	SR	IR_SR_1WLA_CURH	12	8	tbd	T20-5	SRCA 1W Lamp Current_A=B#, also in eng T30-5D	SW	na	na	5873	MM10A01T
21	SR	IR_SR_1WLB_CURH	12	8	tbd	T20-5	SRCA 1W Lamp Current_B=B#, also in eng T30-5D	SW	na	na	59F3	MM10A04T
21	SR	TA_SR_IR_SRC_A	9	8	-55 to +200°C	T20-5	IR source A temp	A	U27	C0003/C0004	55F3	MM09A06T
21	SR	TA_SR_IR_SRC_B	9	8	-55 to +200°C	T20-5	IR source B temp	A	U26	C0003/C0004	4EF3	MM09A20T
1,21	SR	TA_SR_SRC_A_SIPD	9	8	-43 to +85°C	T20-5	Temp of Silicon photodiode A for SIS rad FB control	A	U27	C0003/C0004	5673	MM09A07T
1,21	SR	TA_SR_SRC_B_SIPD	9	8	-43 to +85°C	T20-5	Temp of Silicon photodiode B for SIS rad FB control	A	U27	C0003/C0004	56F3	MM09A08T
21	SR	TP_SR_GRAT_ELEX	9	8	-43 to +85°C	T20-6	Grating motor drive board temp	P	U10	C0003/C0004	139B	CE03A05T
21	SR	TP_SR_GRAT_MOTOR	9	8	-43 to +85°C	T20-6	SRCA grating motor temp	P	U10	C0003/C0004	141B	CE03A06T
21	SR	TP_SR_LAMP_RING	9	8	-43 to +85°C	T20-6	SIS lamp ring temp	P	U10	C0003/C0004	119B	CE03A01T
21	SR	TP_SR_MIR2_DET	9	8	-43 to +85°C	T20-6	Near secondary mirror diode temp	P	U10	C0003/C0004	131B	CE03A04T
21	SR	TP_SR_MONO_CHAS1	9	65	-43 to +85°C	T20-6	Monochromator chassis1 temp	P	U10	C0003/C0004	149B	CE03A11T
21	SR	TP_SR_MONO_CHAS2	9	65	-43 to +85°C	T20-6	Monochromator chassis2 temp	P	U10	C0003/C0004	129B	CE03A03T
21	SR	TP_SR_SNOUT	9	65	-43 to +85°C	T20-6	Output collimator of SRCA temp	P	U10	C0003/C0004	121B	CE03A02T
21	SR	VR_SR_LAMPS_H	12	8	tbd	T20-5	Common voltage across all lamps, also in eng T30-5D	SW	na	na	5B74	MM10A22T
21	SR	VR_SR_SRC_A_RADH	12	8	tbd	T20-5	Output of temp stabilized Silicon photodiode A for SIS rad FB control, also in eng T30-5D	SW	na	na	5973	MM10A03T
21	SR	VR_SR_SRC_B_RADH	12	8	tbd	T20-5	Output of temp stabilized Silicon photodiode B for SIS rad FB control, also in eng T30-5D	SW	na	na	5AF3	MM10A06T
21,75	SS	TP_SS_SPARE	9	65	-43 to +85°C	T20-6	Was TP_SS_SUNSHADE	P	U9	C0003/C0004	2A4B	SS00A01T
	TC	VR_TC_CSCKT_PV	8	65	0 to +12.5V	T20-5	Temp Cntlr cold stage tlmy ckt +V	A	U28	C0003/C0004	5C75	MM11A05T
	TC	VR_TC_ISCKT_PV	8	65	0 to +12.5V	T20-5	Temp Cntlr intermediate stage tlmy ckt +V	A	U28	C0003/C0004	5D75	MM11A11T
	TC	VR_TC_LWCKT_NV	8	65	-12.5 to 0V	T20-5	Temp Cntlr LWIR FPA tlmy ckt -V	A	U29	C0003/C0004	6275	MM11A44T
	TC	VR_TC_LWCKT_PV	8	65	0 to +12.5V	T20-5	Temp Cntlr LWIR FPA tlmy ckt +V	A	U29	C0003/C0004	61F5	MM11A43T
	TC	VR_TC_OSCKT_PV	8	65	0 to +12.5V	T20-5	Temp Cntlr outer stage tlmy ckt +V	A	U29	C0003/C0004	6475	MM11A49T

TABLE 20-2A. MODIS TELEMETRY LIST

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5/97

pfm chg#	1 Subsys	2 Mnemonic Name	3 # of Bits	4 Sample Period	5 Tlmy Range	6 Equations & Limits	7 Remarks	8 Tlmy Type	9 Analog Mux	10 HW Addr Write/Read	11 HW Data Loc	12 Design Unique ID
	TC	VR_TC_SMCKT_NV	8	65	-12.5 to 0V	T20-5	Temp Cntlr SMIR FPA tlmy ckt -V	A	U29	C0003/C0004	6175	MM11A42T
	TC	VR_TC_SMCKT_PV	8	65	0 to +12.5V	T20-5	Temp Cntlr LWIR FPA tlmy ckt +V	A	U29	C0003/C0004	60F5	MM11A41T
74	TC	VR_TC_VISCKT_NV	8	65	-12.5 to 0V	T20-5	Temp Cntlr VIS tlmy ckt -V and NIR tlmy ckt	A	U29	C0003/C0004	6375	MM11A46T
74	TC	VR_TC_VISCKT_PV	8	65	0 to +12.5V	T20-5	Temp Cntlr VIS tlmy ckt +V and NIR tlmy ckt	A	U29	C0003/C0004	62F5	MM11A45T
	TE	TP_TE_FOLD_MIR	9	65	-43 to +85°C	T20-6	Telescope fold mirror temp	P	U9	C0003/C0004	2ACB	TE00A01T
	TE	TP_TE_PRI_MIR	9	65	-43 to +85°C	T20-6	Telescope primary mirror temp	P	U9	C0003/C0004	2B4B	TE00A02T
	TE	TP_TE_SEC_MIR	9	65	-43 to +85°C	T20-6	Telescope secondary mirror temp	P	U9	C0003/C0004	2BCB	TE00A03T
	TG	CR_TG_A_ON	1	8	na	na	Timing Gen AON_BOFF=1, AOFF=0 by R cmd	D	na	C0010	C	MM13B06T
	TG	CR_TG_A_RESET	1	8	na	na	Timing Gen A Reset=0, Running=1 by D cmd (transitory)	D	na	C0010	D	MM13D29T
	TG	CR_TG_B_ON	1	8	na	na	Timing Gen BON_AOFF=1, BOFF=0 by R cmd	D	na	C0011	0	MM14B06T
	TG	CR_TG_B_RESET	1	8	na	na	Timing Gen B Reset=0, Running=1 by D cmd (transitory)	D	na	C0011	1	MM14D29T
	TM	TP_TM_ANLG_CKT	9	65	-43 to +85°C	T20-6	Active A/B analog tlmy ckt temp	P	U7	C0003/C0004	27BB	same PWB
3	TM	VR_TM_REF_ACT1_1	12	65	-2.5 to +2.5V	T20-5	TM mux Act1 Ref1 = B# volts (~1 V), all Ref1's same source (BB)	A	U25	C0003/C0004	85F0	same PWB
3	TM	VR_TM_REF_ACT1_2	12	65	-2.5 to +2.5V	T20-5	TM mux Act1 Ref2 = B# volts (~1 V), all Ref2's same source (Therm)	A	U25	C0003/C0004	8570	same PWB
3	TM	VR_TM_REF_ACT1_3	12	65	-2.5 to +2.5V	T20-5	TM mux Act1 Ref3 = B# volts (~1 V), all Ref3's same source (PRT)	A	U25	C0003/C0004	84F0	same PWB
3	TM	VR_TM_REF_ACT2_1	12	65	-2.5 to +2.5V	T20-5	TM mux Act2 Ref1 = B# volts (~1 V), all Ref1's same source (BB)	A	U26	C0003/C0004	8FF0	same PWB
3	TM	VR_TM_REF_ACT2_2	12	65	-2.5 to +2.5V	T20-5	TM mux Act2 Ref2 = B# volts (~1 V), all Ref2's same source (Therm)	A	U26	C0003/C0004	8F70	same PWB
3,47	TM	VR_TM_REF_ACT3_1	12	65	-2.5 to +2.5V	T20-5	TM mux Act3 Ref1 = B# volts (~1 V), all Ref1's same source (BB)	A	U27	C0003/C0004	97F0	same PWB
3,47	TM	VR_TM_REF_ACT4_1	12	65	-2.5 to +2.5V	T20-5	TM mux Act4 Ref1 = B# volts (~1 V), all Ref1's same source (BB)	A	U28	C0003/C0004	9FF0	same PWB
3	TM	VR_TM_REF_ACT5_1	12	65	-2.5 to +2.5V	T20-5	TM mux Act5 Ref1 = B# volts (~1 V), all Ref1's same source (BB)	A	U29	C0003/C0004	A7F0	same PWB
3	TM	VR_TM_REF_ACT5_2	12	65	-2.5 to +2.5V	T20-5	TM mux Act5 Ref2 = B# volts (~1 V), all Ref2's same source (Therm)	A	U29	C0003/C0004	A770	same PWB
3	TM	VR_TM_REF_ACT5_3	12	65	-2.5 to +2.5V	T20-5	TM mux Act5 Ref3 = B# volts (~1 V), all Ref3's same source (PRT)	A	U29	C0003/C0004	A6F0	same PWB
3	TM	VR_TM_REF_ACT6_1	12	65	-2.5 to +2.5V	T20-5	TM mux Act6 Ref1 = B# volts (~1 V), all Ref1's same source (BB)	A	U30	C0003/C0004	AFF0	same PWB
3	TM	VR_TM_REF_ACT6_3	12	65	-2.5 to +2.5V	T20-5	TM mux Act6 Ref3 = B# volts (~1 V), all Ref3's same source (PRT)	A	U30	C0003/C0004	AF70	same PWB
3,47	TM	VR_TM_REF_ACT7_1	12	65	-2.5 to +2.5V	T20-5	TM mux Act7 Ref1 = B# volts (~1 V), all Ref1's same source (BB)	A	U31	C0003/C0004	B7F0	same PWB
6	TM	VR_TM_REF_ACTGND	12	65	-2.5 to +2.5V	T20-5	Analog tlmy Gnd Ref, D#X.XXXX V	A	A	C0003/C0004	B870	same PWB
3,28,61	TM	VR_TM_REF_BB_1	12	65	DN	T20-6	TM BB Ref1, DN from R1.a= 2490.0Ω, nominal DN=94	P	U2	C0003/C0004	068B	same PWB
3,28,61	TM	VR_TM_REF_BB_2	12	65	DN	T20-6	TM BB Ref2, DN from R2.a= 4639.8Ω, nominal DN=680	P	U2	C0003/C0004	070B	same PWB
3,28,61	TM	VR_TM_REF_BB_3	12	65	DN	T20-6	TM BB Ref3, DN from R3.a= 14000.8Ω, nominal DN=3226	P	U2	C0003/C0004	078B	same PWB
7,28,61	TM	VR_TM_REF_PRT1	12	65	DN	T20-6	TM PRT1 mux 96, DN from R69.a= 1000.08Ω, nominal DN=2502	P	U21	C0003/C0004	386B	same PWB
8,28,61	TM	VR_TM_REF_PRT2	12	65	DN	T20-6	TM PRT2 mux 96, DN from R107.a= 499.06, nominal DN=1072	P	U21	C0003/C0004	3CEB	same PWB
3,28,61	TM	VR_TM_REF_PSV1	12	65	DN	T20-6	TM Psv1 mux 16, DN from R74.a= 2000.06Ω, nominal DN=1311	P	U10	C0003/C0004	101B	same PWB
3,28,61	TM	VR_TM_REF_PSV2	12	65	DN	T20-6	TM Psv2 mux 32, DN from R73.a= 2000.02Ω, nominal DN=1311	P	U8	C0003/C0004	182B	same PWB
3,28,61	TM	VR_TM_REF_PSV3	12	65	DN	T20-6	TM Psv3 mux 48, DN from R72.a= 2000.09Ω, nominal DN=1311	P	U7	C0003/C0004	203B	same PWB
3,28,61	TM	VR_TM_REF_PSV4	12	65	DN	T20-6	TM Psv4 mux 64, DN from R71.a= 2000.04Ω, nominal DN=1311	P	U9	C0003/C0004	284B	same PWB
3,28,61	TM	VR_TM_REF_PSV5	12	65	DN	T20-6	TM Psv5 mux 80, DN from R70.a= 2000.08Ω, nominal DN=1311	P	U11	C0003/C0004	305B	same PWB
10,28,61	TM	VR_TM_REF_PSV6	12	65	DN	T20-6	TM Psv6 mux 48, DN from R106.a= 499.07Ω, nominal DN=65	P	U17	C0003/C0004	24BB	same PWB
11,28,61	TM	VR_TM_REF_PSV7	12	65	DN	T20-6	TM Psv7 mux 64, DN from R105.a= 499.09Ω, nominal DN=65	P	U16	C0003/C0004	2CCB	same PWB
9,28,61	TM	VR_TM_REF_PSV8	12	65	DN	T20-6	TM Psv8 mux 80, DN from R104.a= 499.10Ω, nominal DN=65	P	U15	C0003/C0004	34DB	same PWB
	459	*<--List total w/o spares*	**3182**		*<--Bit total (90 bits by S/C)*							

TABLE 20-2A. MODIS TELEMETRY LIST

Sort by Subsystem - - End User Interest extends through Column 7 - - See Notes at table bottom - - Shaded area indicates S/C pt-pt processing. *5/97*

pfm chg#	1 Subsys	2 Mnemonic Name	3 # of Bits	4 Sample Period	5 Tlmy Range	6 Equations & Limits	7 Remarks	8 Tlmy Type	9 Analog Mux	10 HW Addr Write/Read	11 HW Data Loc	12 Design Unique ID
	TELEMETRY SPARES ARE NOT AN END USER INTEREST ITEM.											
	SPAN	VR_SPARE	na	na	na	na	Spare analog gen purpose 009	A	A	C0003/C0004	047F	na
	SPAN	VR_SPARE	na	na	na	na	Spare analog gen purpose (was T30-5D Ge Det SM10, now deleted)	A	A	C0003/C0004	0DFD	na
	SPAN	VR_SPARE	na	na	na	na	Spare analog gen purpose (was T30-5D Ge Det SM11, now deleted)	A	A	C0003/C0004	0E7D	na
	SPAN	VR_SPARE	na	na	na	na	Spare analog gen purpose111	A	A	C0003/C0004	377F	na
	SPAN	VR_SPARE	na	na	na	na	Spare analog gen purpose 077	A	A	C0003/C0004	A67F	na
	SPBB	TP_SPARE	na	na	na	na	Spare BB passive temp spare	P	PB	C0003/C0004	X60B	na
	SPD	CR_SPARE	na	na	na	na	Spare digital bilevel tlmy 19	D	na	C0011	2	na
	SPD	CR_SPARE	na	na	na	na	Spare digital bilevel tlmy 20	D	na	C0011	3	na
	SPD	CR_SPARE	na	na	na	na	Spare digital bilevel tlmy 23	D	na	C0012	4	na
	SPD	CR_SPARE	na	na	na	na	Spare digital bilevel tlmy 24	D	na	C0012	5	na
	SPD	CR_SPARE	na	na	na	na	Spare digital bilevel tlmy 25	D	na	C0011	6	na
	SPD	CR_SPARE	na	na	na	na	Spare digital bilevel tlmy 13	D	na	C0010	8	na
	SPD	CR_SPARE	na	na	na	na	Spare digital bilevel tlmy 14	D	na	C0010	9	na
	SPD	CR_SPARE	na	na	na	na	Spare digital bilevel tlmy 26	D	na	C0011	A	na
	SPD	CR_SPARE	na	na	na	na	Spare digital bilevel tlmy 15	D	na	C0010	E	na
	SPD	CR_SPARE	na	na	na	na	Spare digital bilevel tlmy 16	D	na	C0010	F	na
	SPPV	VR_PV_MUX_B	na	na	na	na	Spare PV mux to analog tlmy	A	A	C0003/C0004	03F1	AS10A03T
12	SPTP	TP_SPARE	na	na	na	na	Spare passive temp 33	P	PT	C0003/C0004	18AB	na
15	SPTP	TP_SPARE	na	na	na	na	Spare passive temp; (was MF top by KM1; now done by S/C)	P	PT	C0003/C0004	1BAB	na
	SPTP	TP_SPARE	na	na	na	na	Spare passive temp 41	P	PT	C0003/C0004	243B	na
	SPTP	TP_SPARE	na	na	na	na	Spare passive temp 43	P	PT	C0003/C0004	253B	na
	SPTP	TP_SPARE	na	na	na	na	Spare passive temp 50	P	PT	C0003/C0004	28CB	na
	SPTP	TP_SPARE	na	na	na	na	Spare passive temp 51	P	PT	C0003/C0004	294B	na
	SPTP	TP_SPARE	na	na	na	na	Spare passive temp 52	P	PT	C0003/C0004	29CB	na
	SPTP	TP_SPARE	na	na	na	na	Spare passive temp 57	P	PT	C0003/C0004	2C4B	na
	SPTP	TP_SPARE	na	na	na	na	Spare passive temp 59	P	PT	C0003/C0004	2D4B	na
	SPTP	TP_SPARE	na	na	na	na	Spare passive temp 60	P	PT	C0003/C0004	2DCB	na
	SPTP	TP_SPARE	na	na	na	na	Spare passive temp 61	P	PT	C0003/C0004	2E4B	na
	SPTP	TP_SPARE	na	na	na	na	Spare passive temp 62	P	PT	C0003/C0004	2ECB	na
	SPTP	TP_SPARE	na	na	na	na	Spare passive temp 63	P	PT	C0003/C0004	2F4B	na
	SPTP	TP_SPARE	na	na	na	na	Spare passive temp 64	P	PT	C0003/C0004	2FCB	na
	SPTP	TP_SPARE	na	na	na	na	Spare passive temp 75	P	PT	C0003/C0004	355B	na
	SPTP	TP_SPARE	na	na	na	na	Spare passive temp 80	P	PT	C0003/C0004	37DB	na
	SPTP	TP_SPARE	na	na	na	na	Spare passive temp 85	P	PT	C0003/C0004	3A6B	na
	SPTP	TP_SPARE	na	na	na	na	Spare passive temp 86	P	PT	C0003/C0004	3AEB	na
	SPTP	TP_SPARE	na	na	na	na	Spare passive temp 87	P	PT	C0003/C0004	3B6B	na
	SPTP	TP_SPARE	na	na	na	na	Spare passive temp 88	P	PT	C0003/C0004	3BEB	na
	SPTP	TP_SPARE	na	na	na	na	Spare passive temp 89	P	PT	C0003/C0004	3C6B	na

TABLE 20-2A. MODIS TELEMETRY LIST

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pfm chg#	1 Subsys	2 Mnemonic Name	3 # of Bits	4 Sample Period	5 Tlmy Range	6 Equations & Limits	7 Remarks	8 Tlmy Type	9 Analog Mux	10 HW Addr Write/Read	11 HW Data Loc	12 Design Unique ID

Notes:

1. Column 1 is Subsystem 2-alpha code defined by 151840 Table 10 or Figure 11.

2. Column 2 Mnemonic Name is 2nd 16 character field of OASIS name. First 16 character field (not shown) contains External Element, which is MOD.
Leading 2 characters indicate:
1st character: C = configuration, I = current, S = status, T = temperature, V = voltage
2nd character: A = active analog, D = pseudo or derived, R = real or raw data, S = flight software generated, P = passive analog.

3. Column 3 relates number of bits (status or digital value).

4. Column 4 indicates coarse 1553 Bus sampling period in sec, actuals are:
1 = 1.024 sec, 1 major cycle (128x8ms minor cycles); 8 = 8.192 sec, 8 major cycles; 65 = 65.536 sec, 1 master cycle, 64 major cycles.

5. Column 5 provides nominal analog tlmy range. Column 6 is reference pointer to analog scale factors and alarm limits.

6. Column 7 provides remarks. Tables T30-5C & T30-5D are noted for some items which are SW echo of items in T30-5C eng data, or are sourced from T30-5D cmd parameters. Echoes, whose prime location value is derived from HW as opposed to SW, have an H for HK appended to its name in this list.

7. Column 8 is a tlmy processing type code to indicate:
A = active analog direct, APC = analog via 1 of 6 PC muxes (FAM), APV = active analog via 1 of 1 PV mux (SAM), D = digital bilevel direct, DCE = digital bilevel via CP-CE bus, DS = digital bilevel via S/C, P = passive analog direct, PS = passive analog via S/C, SW = software.

8. Column 9 relates to analog tlmy, and is mux processing group on analog tlmy PWB:
A = active analog, PB = passive blackbody thermistors (273 to 320K), PT = passive thermistor group generally with high temperature range (-45 to +85°C) PP = passive PRT sensors generally low temperature range (-130 to +60°C).

9. Columns 10 & 11 provides the hardware to software interface information, which varies according to the Col 8 Type Tlmy (see 20.4 for details). Briefly, analog types A, APC, APV & P hex Write/Read addresses are in Col 10 and related hex data locations are in Col 11. In addition, APC & APV are a general mux data location with the detail step locations provided by Table 20-3 . Type D bilevel data is read directly from the address in Col 10 and the value is indicated for the single bit position of a 16-bit word in Col 11 (data bit 0 corresponds to the least significant bit). See Note 12 for type DCE. SW locations are only in SW code.

10. Column 12 is a Unique ID for hardware related items.

11. For a defintion of how Type DCE tlmy is accessed, see Appendix E for PL3095-N02646A MODIS Software Commands for On Board Calibrator Control. This defines the internal commands & telemetry that flow across CP-CE serial link to control the BB, SDSM and SRCA.

12. Initial HW spares are listed at bottom of Table 20-2A. Active items changed to spares appear in top of table if carried as spare in Table 20-4 Tlmy Frame. If frame use as been reassigned, subsequent spares are moved to bottom of Table 20-4.

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PF Change History. Left column Chg #s relate to these #s. [#s] are general notes.

1. 8/7/95 3 Col2 chgs. Deleted extra space in TA_SR_SRC_A_SIPD & TA_SR_SRC_B_SIPD & CR_BB_SPARE(DCE) to meet 16 charcter name count(see 14 for later CR_BB spare).
2. 8/10/95 8 Col 7 Remark chgs to shorten # of characters. No functional chgs.
3. 8/13/95 Revised all VR_TM_REF_XXXX's Col7 Remarks to note, all Ref1's are common source, all Ref2's etc, all Ref3's etc. Also added UXX device ref designator to Col 9 Mux ID. Changed VR_TM_REF_ACT6_1 to VR_TM_REF_ACT6_3 because of internal ref 3.
4. 8/13/95 Changed relation of VIS & NIR FPAs from WF subsys to AO subsys. New names are TA_AO_VIS_FPA & TA_AO_NIR_FPA. Chged TP_RC_OS_WH to SPARE. Corrected minor typo in CR_SR_GRAT_FH_A Col7 of B=0 to A=0.
5. 10/4/95 IR_PS2_INPUT_CUR revised HW loc to 76F7 from 75F7.
6. 10/4/95 VR_TM_REF_GND chged codes on Col 8,9 to A, A from P, P.
7. 10/4/95 VR_TM_REF_PRT1, add 1 to name in Col2&7.
8. 10/4/95 Create new tlmy VR_TM_REF_PRT2 at 3CEB.
9. 10/4/95 Create new tlmy VR_TM_REF_PSV8 at 34DB. Replaces TP_SA_B_MTR at loc 34DB.
10. 10/4/95 Create new tlmy VR_TM_REF_PSV6 at 24BB. Also, delete SPTP Psv Temp 42 at 24BB.
11. 10/4/95 Create new tlmy VR_TM_REF_PSV7 at 2CCB. Also, delete SPTP Psv Temp 58 at 2CCB.
12. 10/4/95 Correct SPTP Spare passive temp 33 loc to 18AB from 1BAB.
13. 10/8/95 Chg subsys relation of VR_TC_LW_FPA_HTR to VR_RC_LW_FPA_HTR and VR_TC_SM_FPA_HTR to VR_RC_SM_FPA_HTR.
14. 10/13/95 Chg CR_BB_ HTR_ OFF into CR_BB_SPARE(DCE) at C0001, bit 0. Was redundant to BB_HTR_CURR.
15. 10/16/95 Added TP_SPARE at bottom of table at C0003/C0004, 1BAB. This was made a spare in 9/94 when TP_MF_KM1 went to S/C processing, but later got dropped from spares.

[16] 11/1/95 Revise Chg #s to directly apply to one or multiple items. (XX) notes like this one are general and don't appear near table body.

17. 11/4/95 Revise logic values on SR_FO_BLK1,2,3,4_MODEto 0=Read, 1=Write vs 1=Read, 2=Write.
18. 11/5/95 Chg tlmy range on TP_BB_TEMP01H,12H to 270K to 320K from 273K to 320K.
19. 11/5/95 Chged CR_FO_BLK1,2,3,4_RESET's to FO_SPARE's.

[20] 11/5/95 Minor revision to Notes to compact them, and make remark how spares are handled Note 12.

21. 11/5/95 Clean up Col 7 references for Eqs & limits, mostly PV Subsys, but a few other subsys items.
22. 11/5/95 Add new 3-bit tlmy CS_CP_MODIS_XX, XX=EM, PF, F1, F2.
23. 11/24/95 Revise Col 5 Range & Col 8 Remarks on 5 CS_FR_DELAY_XX from D#0-100, 1=3.33µs to D#0-50, 1=6.66µs, 0.02IFOV.
24. 11/24/95 Chg door CR_DR_SDS_CLSD to CR_DR_SPARE. On ly 3 SDD limit switches are needed. If SDD is closed, then SDS is closed.
25. 11/24/95 chg name TP_SM_SDSM_GEDET to TP_SM_DET_AMP3.
26. 11/24/95 Revise range of 4 PV sample delays, e.g., CR_PVLW_S_DELAYH to 0-50 units vs 0-63 units, where 1=3.33µs.
27. 11/27/95 Chg names on TP_DR_MTRs 1) to TP_DR_NAD_FS from TP_DR_NAD_MTR, 2) to TP_DR_SVD_FS from TP_DR_SVD_MTR, 3) to TP_DR_SPARE from TP_DR_SDD_MTR.
28. 11/30/95 Insert measured A_side resistance values for VR_TM_REF_BB/PSV ref resistors in Remarks Col 13 pl: BB1,2,3; PRT1,2; PSV1-8.
29. 11/30/95 Chg UIDs on CR_CP_A_ON _M TO MM05D500Y from MM05D976T AND CR_CP_B_ON _M TO MM06D500T from MM06D976T.
30. 12/3/95 Return bit size on TP_RC_MNT_RING back to 12 vs 9 bits. FLT SW never altered to 9.

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31. 12/3/95 Increase # of bits on VR_SA_A_MTR_TORQ & VR_SA_B_MTR_TORQ to 10 bits from 8 bit. (Affects tlmy framing.)
32. 12/3/95 Increase # of bits on VR_RC_LW_FPA_HTR & VR_RC_SM_FPA_HTR to 10 bits from 8 bit. (Affects tlmy framing.)

33. 1/5/96 CR_SM_MIR_HOME_A & CR_SM_MIR_HOME_B: in Remarks 1) chg Note 12 to Note 11, and 2) add Home=DCR View.
34. 1/5/96 CS_SM_MIR_STEP: in Remarks add ~3.75°/step.
35. 2/29/96 add new CS_FR_ENC_DELTA -8191 to +8191 by 14-bit 2s Complement. Shows amount of global collect rotation of all 5 views.
36. 2/29/96 Chg TP_SD_TEMP to TP_SD_Spare. Temp sensor deleted from PF.
37. 2/29/96 Chg TP_RC_OS_FIN to TP_RC_SPARE.
38. 2/29/96 Minor name chg from CR_SR_SISOV_ENA to CR_SR_L_SHDN_ENA.
39. 2/29/96 CR_SR_SIS_OFF revised/expanded: CR_SR_LAMPS_ON =OFF/1W/10W/20W/30W = 000/001/010 /011/100. FLT SW sets up DCE word to go over CP/CE link.
40. 3/3/96 Add new lamp group selection: CS_SR_3L10W_SET, CS_SR_2L10W_SET, CS_SR_1L10W_SET, CS_SR_1L1W_SET.
41. 3/3/96 Add new CR_SR_LAMPS_LOW with Low/High = 0/1. Use HW adress/location thatrevised CR_SIS_OFF Off/On=0/1 at C0001,5.
42. 3/17/96 chg 5 spares to active: SS_CP_SCAN_EST from CP_Status_02, SS_CP_UART_RESET from CP_Status_10, SS_CP_UART_HUNT from CP_Status_11, SS_CP_UART_SYNC from CP_Status_12, SS_CP_UART_NORM from CP_Status_13.
43. 3/17/96 Add 2 new 1-sec words: CP SS_CP_LAST_EVENT and FR SS_FR_LAST_EVENT.
44. 3/17/96 Revise sample time on 4 time code words CP SS_CP_TC1,TC2,TC3,TC4 from 65 sec to 1 sec.
45. 3/17/96 Add 2 new FR words & revise 1 FR_Spare. New CS_FR_BBRADTAB & CS_FR_GAINTAB. Revised from spare CS_FR_OFFSETTAB.
46. 3/17/96 Minor name chg & result: to SS_FR_SCI_PKT Normal/Test from SS_FR_PKT_TEST.
47. 3/20/96 Minor name addon of last _X to 3 TM words to tie to particular Vref= 1, 2, 3. See Remarks.
48. 3/20/97 Correct BB, SDSM & SRCA logic & HW locations to match 3/1/94 Memo 16-bit serial link protocol. Logic on CE_SR_IR_SRC_OFF. HW locations on CR_SR_GRAT_CH_B, CR_SR_GRAT_FH_B, CR_SR_SLIT_HOMEB, CR_SR_LAMPS_LOW.
49. 3/21/96 add 3 new words to match new cmds: SET_FR_PCDCRDBG, SET_FR_PCDCRPOST & SET_FR_PCDCRPRE.

[50] 4/2/96 reinstate - 3/22/96 2 to spares: TP_SA_SPARE was TP_SA_RCT1_HSG & TP_SA_SPARE was TP_SA_RCT2_HSG.

51. 3/22/96 add new CS_FR_SCI_NORMAL yes/no from 20 cmd selections (27 tlmy because of PV A/B). Also created T20-2A & T20-2B so T20-2B canb be vehicle to summarize details that go into SCI_NORMAL.
52. 3/24/96 Clairfy door & OBC mtr step tlmy is in absolute step count. 4/13 add step count for absolute positions.
53. 3/25/96 Partition SS_CP_STATUS_03 into 2 new 4-bit words with left over bits in T20-4 frame going to frame fill. Add SS_CP_LOG_STATE & SS_FR_LOG_STATE
54. 3/28/96 Chg 6 CP/FR items to SS_CP_SPARE or SS_FR_SPARE deemed unecessary for online ops: SS_CP_MEMPRO_ERR, SS_FR_MEMPRO_ERR, SS_CP_PARITY_ERR, SS_FR_PARITY_ERR, SS_CP_TEST_RES & SS_FR_TEST_RES. AffectsT20-4.
55. 4/6/96 Reinstate SS_CP_STATUS_04 inadvertently deleted while doing Chgs#53&#54. FYI T20-4 has related cleanup.

[56] 4/6/96 Shortened table title to MODIS TELEMETRY LIST from MODIS TELEMETRY LIST - BY SUBSYSTEM.

57. 4/8/96 Minor name chg to CS_CP_MODIS_MOD from CS_CP_MODIS_XX. Same chg in T20-4.

[58] 4/12/96 added Col 9 entries for mux chip U## for active and passive analog tlmy.

59. 4/24/96 Revise Chg Note#50 to again chg 2 pts back to spares: TP_SA_SPARE was TP_SA_RCT1_HSG & TP_SA_SPARE was TP_SA_RCT2_HSG.

----------Changes since 151840 initial 5/96 release----------

60. 5/8/96 For completeness, add back in 2 S/C tlmy wired-spares that inadvertently got dropped.

TABLE 20-2A. MODIS TELEMETRY LIST

Sort by Subsystem - - End User Interest extends through Column 7 - - See Notes at table bottom - - Shaded area indicates S/C pt-pt processing. *5/97*

pfm chg#	1 Subsys	2 Mnemonic Name	3 # of Bits	4 Sample Period	5 Tlmy Range	6 Equations & Limits	7 Remarks	8 Tlmy Type	9 Analog Mux	10 HW Addr Write/Read	11 HW Data Loc	12 Design Unique ID

61. 8/7/96 Chg Col 5 Tlmy range & Col 7 Remarks on last 13 reference signals of TM to read in raw DN. Nominal DN listed in Col 7.
62. 8/7/96 Chg name, function & nominal value of 6 PC signals from individual band parameters to band-pair sample clock rise/fall locations.
63. 8/12/96 Correct Col 11 interchanged HW Address locations on CR_PVVISB_ECALON & CR_PVVIS_B_ON.
64. 8/13/96 Add 152932 reference definition pointer to Col 7 Remarks for SS_CP_LAST_EVENT & SS_FR_LAST_EVENT to define codes for events. Also add note to SS_CP_LOG_EVENT & SS_FR_LOG_EVENT to point to SS_CP_LAST_EVENT & SS_FR_LAST_EVENT for info.
65. 8/15/96 Add two new words SS_CP_MACRO_ID and SS_CP_MACRO_ON.
66. 8/15/96 Revise 1 CP and 3 FR to spares.
67. 8/26/96 Generate OASIS composite CR_RC_CFPA_SETPT to 83, 85, 88K from CR_RC_CFPA_T1SET & CR_RC_CFPA_T3SET.
68. 9/15/96 Revise units on 6 CS_PC3132_SRISE,etc and 4 CR_PVLW_S_DELAYH, etc to be µsec vs units.
69. 9/26/96 On CS_SR_SLIT_STEP, readout is in steps, and updated to be 0 step=Along Track Reticle, 24 steps=Along Scan Reticle (tlmy Home), & 48 steps=Slit Reticle.
70. 9/29/96 Revise logic CR_CPA_EEP_WRE_M & CR_CPB_EEP_WRE_M to be 1=ENABLED, 0=DISABLED.
71. 10/10/96 Convert TP_ME_TB07 to TP_ME_SPARE; 1 of 9 S/C (RTIU test) temp tlmy pts to spare, others remain active.
72. 10/17/96 Reactivate 8-sec FR_SPARE as SS_FR_SCIABNORM with ABNORM/NORM. Gnd flag to ID know SCI abnormalities other than MODIS.
73. 10/21/96 Correct names for VR_PS1_P5.6V_D1 & VR_PS2_P5.6V_D1 to be VR_PS1_P5_6V_D1 & VR_PS2_P5_6V_D1 to be consistent with OASIS convention.
74. 12/9/96 Expand remarks on VR_TC_VISCKT_NV & _PV to also pertain to NIR CKT.
75. 4/97 Multiple EO1122D Incorporations for Rev B. See EO1122D (released 970305) for details of bit increase for several words and name chg & spare chg.
76. 4/97 Direct Rev B chg to increase bits from 8 to 12 and relocate to Maj Cyc 32: 1) IR_SA_A_ECDR_LED, 2) IR_SA_B_ECDR_LED, 3) VR_SA_A_ECDR_MON and VR_SA_B_ECDR_MON.
77. 4/97 Direct Rev B chg to add Remarks use definition for SS_CP_STATUS_04 through _09.

TABLE 20-2B. MODIS TELEMETRY DEFINITION EXTENSION

4/97

pfm chg#	0 Item#	1 Subsys	2 Telemetry Mnemonic Name	3 # of Bits	4 Related Cmd	5 Remarks
	1	FR	CS_FR_SCI_NORMAL	1	All below	Flt SW Polls the following for ANDED Yes/No response.
		FR	CS_FR_BBRADTAB	1	FR35	
		FR	CS_FR_DELAY_BB	7	FR19	
		FR	CS_FR_DELAY_EA	7	FR21	
		FR	CS_FR_DELAY_SD	7	FR17	
		FR	CS_FR_DELAY_SP	7	FR20	
		FR	CS_FR_DELAY_SR	7	FR18	
		FR	CS_FR_ENC_DELTA	14	FR31	
		FR	CS_FR_GAINTAB	1	FR34	
		FR	CS_FR_OFFSETTAB	1	FR33	
		FR	SS_FR_SCI_PKT	1	FR26	
		PC	CR_PCLWA_ECAL_ON	1	PC05	A/B sides count as 1 item for content count to CS_FR_SCI_NORMAL
		PC	CR_PCLWB_ECAL_ON	1	PC05	A/B sides count as 1 item for content count to CS_FR_SCI_NORMAL
		PV	CR_PVLWA_CSUB_ON	1	PV26	A/B sides count as 1 item for content count to CS_FR_SCI_NORMAL
		PV	CR_PVLWA_ECAL_ON	1	PV24	A/B sides count as 1 item for content count to CS_FR_SCI_NORMAL
		PV	CR_PVLWB_CSUB_ON	1	PV26	A/B sides count as 1 item for content count to CS_FR_SCI_NORMAL
		PV	CR_PVLWB_ECAL_ON	1	PV24	A/B sides count as 1 item for content count to CS_FR_SCI_NORMAL
		PV	CR_PVNIRA_ECALON	1	PV10	A/B sides count as 1 item for content count to CS_FR_SCI_NORMAL
		PV	CR_PVNIRB_ECALON	1	PV10	A/B sides count as 1 item for content count to CS_FR_SCI_NORMAL
		PV	CR_PVSMA_CSUB_ON	1	PV18	A/B sides count as 1 item for content count to CS_FR_SCI_NORMAL
		PV	CR_PVSMA_ECAL_ON	1	PV16	A/B sides count as 1 item for content count to CS_FR_SCI_NORMAL
		PV	CR_PVSMB_CSUB_ON	1	PV18	A/B sides count as 1 item for content count to CS_FR_SCI_NORMAL
		PV	CR_PVSMB_ECAL_ON	1	PV16	A/B sides count as 1 item for content count to CS_FR_SCI_NORMAL
		PV	CR_PVVISA_ECALON	1	PV04	A/B sides count as 1 item for content count to CS_FR_SCI_NORMAL
		PV	CR_PVVISB_ECALON	1	PV04	A/B sides count as 1 item for content count to CS_FR_SCI_NORMAL
		PV	CR_PV_A_MEM_RAM	1	PV31	A/B sides count as 1 item for content count to CS_FR_SCI_NORMAL
		PV	CR_PV_B_MEM_RAM	1	PV31	A/B sides count as 1 item for content count to CS_FR_SCI_NORMAL
		18	*<--List contents, note lower A/B items only count as one item.*			

NOTE

1. The status of the first item in the table is the Flt SW ANDED results of the 21 items beneath it.

T20-25B PF Change History

[1] 4/7/96 For PF changed table title & functionas listed from MODIS HOUSEKEEPING TELEMETRY - BY FUNCTION.

——————Changes since 151840 initial 5/96 release——————

[2] 8/15/96 Delete tlmy related to delted cmds: CS_FR_PCDCRDBG, CS_FR_PCDCRPOST, & CS_FR_PCDCRPRE.

[3] 10/11/96 FYI - For lower A/B choices,Flt SW looks at commands instead of internal tlmy, but end result is effectively the same for overall status.

TABLE 20-2C. MODIS TELEMETRY LIST REMARKS EXTENSION

5/97

pfm chg#	1 Subsys	2 Mnemonic Name	3 # of Bits	4 Sample Period	5 Tlmy Range	6 Equations & Limits	7 Remarks	8 Tlmy Type	9 Analog Mux	10 HW Addr Write/Read	11 HW Data Loc	12 Design Unique ID
	CP	SS_CP_STATUS_09	16	8	na	na	CP/FR Reset Register Bits 0 through 15 coded as follows	SW	na	na	na	na
							Bit 0: CP: Spare - MSB					
							Bit 1: CP: Spare					
							Bit 2: CP: Spare					
							Bit 3: CP: 0=Reset caused by Upload Reset Relay Command					
							Bit 4: CP: 0=Reset caused by Standard Reset Relay Command					
							Bit 5: CP: 0=Reset generated by Power Supply transient					
							Bit 6 CP: Spare					
							Bit 7 CP: 0=Reset generated by Watchdog Timer expiration					
							Bit 8 FR: 0=Power On Reset					
							Bit 9 FR: 0=Emulator Reset					
							Bit 10 FR: 0=Watchdog Reset					
							Bit 11 FR: 0=Upload Reset					
							Bit 12 FR: 0=Standard Reset					
							Bit 13 FR: Spare					
							Bit 14 FR: Spare					
							Bit 15 FR: Spare - LSB					

Notes

1. This table extends Remarks Column for Table 20-2A

PF Change History.

1. 5/97 New table for Rev B. SS_CP_STATUS-09 only entry at this time.

TABLE 20-3. FAM (PC) & SAM (PV) MUX DATA LOCATION

5/97

chg	1 Subsystem	2 Mnemonic Name	3 # of Bits	4 Sample Rate	5 N/A	6 N/A	7 Remarks	8 Type Data	9 TM HW Addr/Read	10 TM HW Data	11 PWB Mux	12 Mux Step
	This table is of primary interest to HW/SW development, integration & test -- See Notes at table bottom for description of columns.											
	PC	VR_PC_B31_GND	8	65			Via FAM mux AF01	HK	C0003/C0004	0070	1	0
	PC	TA_PC_B31_MUX	9	65			FAM AF01 active A/B side mux temp	HK	C0003/C0004	0070	1	1
	PC	VR_PC_B31_RN12V	8	65			Via FAM mux AF01	HK	C0003/C0004	0070	1	2
	PC	VR_PC_B31_RN5V	8	65			Via FAM mux AF01	HK	C0003/C0004	0070	1	3
	PC	VR_PC_B31_RP5V	8	65			Via FAM mux AF01	HK	C0003/C0004	0070	1	4
	PC	VR_PC_B31_RP12V	8	65			Via FAM mux AF01	HK	C0003/C0004	0070	1	5
2	PC	VR_PC_B31C10_DCR	8	1.5			Via FAM AF01mux	SCI	C0003/C0004	0070	1	6
2	PC	VR_PC_B31C09_DCR	8	1.5			Via FAM AF01mux	SCI	C0003/C0004	0070	1	7
2	PC	VR_PC_B31C08_DCR	8	1.5			Via FAM AF01mux	SCI	C0003/C0004	0070	1	8
2	PC	VR_PC_B31C07_DCR	8	1.5			Via FAM AF01mux	SCI	C0003/C0004	0070	1	9
2	PC	VR_PC_B31C06_DCR	8	1.5			Via FAM AF01mux	SCI	C0003/C0004	0070	1	10
2	PC	VR_PC_B31C05_DCR	8	1.5			Via FAM AF01mux	SCI	C0003/C0004	0070	1	11
2	PC	VR_PC_B31C04_DCR	8	1.5			Via FAM AF01mux	SCI	C0003/C0004	0070	1	12
2	PC	VR_PC_B31C03_DCR	8	1.5			Via FAM AF01mux	SCI	C0003/C0004	0070	1	13
2	PC	VR_PC_B31C02_DCR	8	1.5			Via FAM AF01mux	SCI	C0003/C0004	0070	1	14
2	PC	VR_PC_B31C01_DCR	8	1.5			Via FAM AF01mux	SCI	C0003/C0004	0070	1	15
	PC	VR_PC_B32_GND	8	65			Via FAM mux AF02	HK	C0003/C0004	00F0	2	0
	PC	TA_PC_B32_MUX	9	65			FAM AF02 active A/B side mux temp	HK	C0003/C0004	00F0	2	1
	PC	VR_PC_B32_RN12V	8	65			Via FAM mux AF02	HK	C0003/C0004	00F0	2	2
	PC	VR_PC_B32_RN5V	8	65			Via FAM mux AF02	HK	C0003/C0004	00F0	2	3
	PC	VR_PC_B32_RP5V	8	65			Via FAM mux AF02	HK	C0003/C0004	00F0	2	4
	PC	VR_PC_B32_RP12V	8	65			Via FAM mux AF02	HK	C0003/C0004	00F0	2	5
2	PC	VR_PC_B32C10_DCR	8	1.5			Via FAM AF02 mux	SCI	C0003/C0004	00F0	2	6
2	PC	VR_PC_B32C09_DCR	8	1.5			Via FAM AF02 mux	SCI	C0003/C0004	00F0	2	7
2	PC	VR_PC_B32C08_DCR	8	1.5			Via FAM AF02 mux	SCI	C0003/C0004	00F0	2	8
2	PC	VR_PC_B32C07_DCR	8	1.5			Via FAM AF02 mux	SCI	C0003/C0004	00F0	2	9
2	PC	VR_PC_B32C06_DCR	8	1.5			Via FAM AF02 mux	SCI	C0003/C0004	00F0	2	10
2	PC	VR_PC_B32C05_DCR	8	1.5			Via FAM AF02 mux	SCI	C0003/C0004	00F0	2	11
2	PC	VR_PC_B32C04_DCR	8	1.5			Via FAM AF02 mux	SCI	C0003/C0004	00F0	2	12
2	PC	VR_PC_B32C03_DCR	8	1.5			Via FAM AF02 mux	SCI	C0003/C0004	00F0	2	13
2	PC	VR_PC_B32C02_DCR	8	1.5			Via FAM AF02 mux	SCI	C0003/C0004	00F0	2	14
2	PC	VR_PC_B32C01_DCR	8	1.5			Via FAM AF02 mux	SCI	C0003/C0004	00F0	2	15
	PC	VR_PC_B33_GND	8	65			Via FAM mux AF03	HK	C0003/C0004	0170	3	0
	PC	TA_PC_B33_MUX	9	65			FAM AF03 active A/B side mux temp	HK	C0003/C0004	0170	3	1
	PC	VR_PC_B33_RN12V	8	65			Via FAM mux AF03	HK	C0003/C0004	0170	3	2
	PC	VR_PC_B33_RN5V	8	65			Via FAM mux AF03	HK	C0003/C0004	0170	3	3
	PC	VR_PC_B33_RP5V	8	65			Via FAM mux AF03	HK	C0003/C0004	0170	3	4
	PC	VR_PC_B33_RP12V	8	65			Via FAM mux AF03	HK	C0003/C0004	0170	3	5
2	PC	VR_PC_B33C10_DCR	8	1.5			Via FAM AF03 mux	SCI	C0003/C0004	0170	3	6

TABLE 20-3. FAM (PC) & SAM (PV) MUX DATA LOCATION

5/97

chg	1 Subsystem	2 Mnemonic Name	3 # of Bits	4 Sample Rate	5 N/A	6 N/A	7 Remarks	8 Type Data	9 TM HW Addr/Read	10 TM HW Data	11 PWB Mux	12 Mux Step
	This table is of primary interest to HW/SW development, integration & test - - See Notes at table bottom for description of columns.											
2	PC	VR_PC_B33C09_DCR	8	1.5			Via FAM AF03 mux	SCI	C0003/C0004	0170	3	7
2	PC	VR_PC_B33C08_DCR	8	1.5			Via FAM AF03 mux	SCI	C0003/C0004	0170	3	8
2	PC	VR_PC_B33C07_DCR	8	1.5			Via FAM AF03 mux	SCI	C0003/C0004	0170	3	9
2	PC	VR_PC_B33C06_DCR	8	1.5			Via FAM AF03 mux	SCI	C0003/C0004	0170	3	10
2	PC	VR_PC_B33C05_DCR	8	1.5			Via FAM AF03 mux	SCI	C0003/C0004	0170	3	11
2	PC	VR_PC_B33C04_DCR	8	1.5			Via FAM AF03 mux	SCI	C0003/C0004	0170	3	12
2	PC	VR_PC_B33C03_DCR	8	1.5			Via FAM AF03 mux	SCI	C0003/C0004	0170	3	13
2	PC	VR_PC_B33C02_DCR	8	1.5			Via FAM AF03 mux	SCI	C0003/C0004	0170	3	14
2	PC	VR_PC_B33C01_DCR	8	1.5			Via FAM AF03 mux	SCI	C0003/C0004	0170	3	15
	PC	VR_PC_B34_GND	8	65			Via FAM mux AF04	HK	C0003/C0004	01F0	4	0
	PC	TA_PC_B34_MUX	9	65			FAM AF04 active A/B side mux temp	HK	C0003/C0004	01F0	4	1
	PC	VR_PC_B34_RN12V	8	65			Via FAM mux AF04	HK	C0003/C0004	01F0	4	2
	PC	VR_PC_B34_RN5V	8	65			Via FAM mux AF04	HK	C0003/C0004	01F0	4	3
	PC	VR_PC_B34_RP5V	8	65			Via FAM mux AF04	HK	C0003/C0004	01F0	4	4
	PC	VR_PC_B34_RP12V	8	65			Via FAM mux AF04	HK	C0003/C0004	01F0	4	5
2	PC	VR_PC_B34C10_DCR	8	1.5			Via FAM AF04 mux	SCI	C0003/C0004	01F0	4	6
2	PC	VR_PC_B34C09_DCR	8	1.5			Via FAM AF04 mux	SCI	C0003/C0004	01F0	4	7
2	PC	VR_PC_B34C08_DCR	8	1.5			Via FAM AF04 mux	SCI	C0003/C0004	01F0	4	8
2	PC	VR_PC_B34C07_DCR	8	1.5			Via FAM AF04 mux	SCI	C0003/C0004	01F0	4	9
2	PC	VR_PC_B34C06_DCR	8	1.5			Via FAM AF04 mux	SCI	C0003/C0004	01F0	4	10
2	PC	VR_PC_B34C05_DCR	8	1.5			Via FAM AF04 mux	SCI	C0003/C0004	01F0	4	11
2	PC	VR_PC_B34C04_DCR	8	1.5			Via FAM AF04 mux	SCI	C0003/C0004	01F0	4	12
2	PC	VR_PC_B34C03_DCR	8	1.5			Via FAM AF04 mux	SCI	C0003/C0004	01F0	4	13
2	PC	VR_PC_B34C02_DCR	8	1.5			Via FAM AF04 mux	SCI	C0003/C0004	01F0	4	14
2	PC	VR_PC_B34C01_DCR	8	1.5			Via FAM AF04 mux	SCI	C0003/C0004	01F0	4	15
	PC	VR_PC_B35_GND	8	65			Via FAM mux AF05	HK	C0003/C0004	0270	5	0
	PC	TA_PC_B35_MUX	9	65			FAM AF05 active A/B side mux temp	HK	C0003/C0004	0270	5	1
	PC	VR_PC_B35_RN12V	8	65			Via FAM mux AF05	HK	C0003/C0004	0270	5	2
	PC	VR_PC_B35_RN5V	8	65			Via FAM mux AF05	HK	C0003/C0004	0270	5	3
	PC	VR_PC_B35_RP5V	8	65			Via FAM mux AF05	HK	C0003/C0004	0270	5	4
	PC	VR_PC_B35_RP12V	8	65			Via FAM mux AF05	HK	C0003/C0004	0270	5	5
2	PC	VR_PC_B35C10_DCR	8	1.5			Via FAM AF05 mux	SCI	C0003/C0004	0270	5	6
2	PC	VR_PC_B35C09_DCR	8	1.5			Via FAM AF05 mux	SCI	C0003/C0004	0270	5	7
2	PC	VR_PC_B35C08_DCR	8	1.5			Via FAM AF05 mux	SCI	C0003/C0004	0270	5	8
2	PC	VR_PC_B35C07_DCR	8	1.5			Via FAM AF05 mux	SCI	C0003/C0004	0270	5	9
2	PC	VR_PC_B35C06_DCR	8	1.5			Via FAM AF05 mux	SCI	C0003/C0004	0270	5	10
2	PC	VR_PC_B35C05_DCR	8	1.5			Via FAM AF05 mux	SCI	C0003/C0004	0270	5	11
2	PC	VR_PC_B35C04_DCR	8	1.5			Via FAM AF05 mux	SCI	C0003/C0004	0270	5	12
2	PC	VR_PC_B35C03_DCR	8	1.5			Via FAM AF05 mux	SCI	C0003/C0004	0270	5	13

TABLE 20-3. FAM (PC) & SAM (PV) MUX DATA LOCATION

5/97

chg	1 Subsystem	2 Mnemonic Name	3 # of Bits	4 Sample Rate	5 N/A	6 N/A	7 Remarks	8 Type Data	9 TM HW Addr/Read	10 TM HW Data	11 PWB Mux	12 Mux Step
	This table is of primary interest to HW/SW development, integration & test - - See Notes at table bottom for description of columns.											
2	PC	VR_PC_B35C02_DCR	8	1.5			Via FAM AF05 mux	SCI	C0003/C0004	0270	5	14
2	PC	VR_PC_B35C01_DCR	8	1.5			Via FAM AF05 mux	SCI	C0003/C0004	0270	5	15
	PC	VR_PC_B36_GND	8	65			Via FAM mux AF06	HK	C0003/C0004	02F0	6	0
	PC	TA_PC_B36_MUX	9	65			FAM AF06 active A/B side mux temp	HK	C0003/C0004	02F0	6	1
	PC	VR_PC_B36_RN12V	8	65			Via FAM mux AF06	HK	C0003/C0004	02F0	6	2
	PC	VR_PC_B36_RN5V	8	65			Via FAM mux AF06	HK	C0003/C0004	02F0	6	3
	PC	VR_PC_B36_RP5V	8	65			Via FAM mux AF06	HK	C0003/C0004	02F0	6	4
	PC	VR_PC_B36_RP12V	8	65			Via FAM mux AF06	HK	C0003/C0004	02F0	6	5
2	PC	VR_PC_B36C10_DCR	8	1.5			Via FAM AF06 mux	SCI	C0003/C0004	02F0	6	6
2	PC	VR_PC_B36C09_DCR	8	1.5			Via FAM AF06 mux	SCI	C0003/C0004	02F0	6	7
2	PC	VR_PC_B36C08_DCR	8	1.5			Via FAM AF06 mux	SCI	C0003/C0004	02F0	6	8
2	PC	VR_PC_B36C07_DCR	8	1.5			Via FAM AF06 mux	SCI	C0003/C0004	02F0	6	9
2	PC	VR_PC_B36C06_DCR	8	1.5			Via FAM AF06 mux	SCI	C0003/C0004	02F0	6	10
2	PC	VR_PC_B36C05_DCR	8	1.5			Via FAM AF06 mux	SCI	C0003/C0004	02F0	6	11
2	PC	VR_PC_B36C04_DCR	8	1.5			Via FAM AF06 mux	SCI	C0003/C0004	02F0	6	12
2	PC	VR_PC_B36C03_DCR	8	1.5			Via FAM AF06 mux	SCI	C0003/C0004	02F0	6	13
2	PC	VR_PC_B36C02_DCR	8	1.5			Via FAM AF06 mux	SCI	C0003/C0004	02F0	6	14
2	PC	VR_PC_B36C01_DCR	8	1.5			Via FAM AF06 mux	SCI	C0003/C0004	02F0	6	15
11	PV	VR_PVVIS_VDET	8	1.5			PV VIS SCA VDET bias of A_1 or B_7 C&B-ACE pwb	SCI	C0003/C0004	0371	0/6	0
11	PV	VR_PVVIS_VDDA	8	1.5			PV VIS SCA VDDA bias of A_1 or B_7 C&B-ACE pwb	SCI	C0003/C0004	0371	0/6	1
11	PV	VR_PVVIS_ITWKA	8	1.5			PV VIS SCA ITWKA bias of A_1 or B_7 C&B-ACE pwb	SCI	C0003/C0004	0371	0/6	2
11	PV	VR_PVVIS_VD1	8	1.5			PV VIS SCA VD1 bias of A_1 or B_7 C&B-ACE pwb	SCI	C0003/C0004	0371	0/6	3
11	PV	VR_PVVIS_VGUARD	8	1.5			PV VIS SCA VGUARD bias of A_1 or B_7 C&B-ACE pwb	SCI	C0003/C0004	0371	0/6	4
11	PV	CR_PVVIS_S_DELAY	8	1.5			PV VIS sample delay of A_1 or B_7 C&B-ACE pwb in D#0-63 units of 3.33µs steps for registration (msb bits 7&8=0 for D#63 limit)	SCI	C0003/C0004	0371	0/6	5
11	PV	VR_PVVIS_VCAL	8	1.5			PV VIS SCA VCAL(ECAL) bias of A_1 or B_7 C&B-ACE pwb	SCI	C0003/C0004	0371	0/6	6
11	PV	VR_PVVIS_VDDD	8	1.5			PV VIS SCA VDDD bias of A_1 or B_7 C&B-ACE pwb	SCI	C0003/C0004	0371	0/6	7
11	PV	VR_PVVIS_VPWELL	8	1.5			PV VIS SCA VPWELL bias of A_1 or B_7 C&B-ACE pwb	SCI	C0003/C0004	0371	0/6	8
11	PV	VR_PVVIS_VDDOUT	8	1.5			PV VIS SCA VDDOUT bias of A_1 or B_7 C&B-ACE pwb	SCI	C0003/C0004	0371	0/6	9
11	PV	VR_PVVIS_P30V	8	65			PV VIS +30V of A_1 or B_7 C&B-ACE pwb	HK	C0003/C0004	0371	0/6	10
11	PV	VR_PVVIS_RN5V	8	65			PV VIS regulated -5V of A_1 or B_7 C&B-ACE pwb	HK	C0003/C0004	0371	0/6	11
11	PV	VR_PVVIS_RN11V	8	65			PV VIS regulated -11V of A_1 or B_7 C&B-ACE pwb	HK	C0003/C0004	0371	0/6	12
11	PV	VR_PVVIS_RP5V	8	65			PV VIS regulated +5V of A_1 or B_7 C&B-ACE pwb	HK	C0003/C0004	0371	0/6	13
11	PV	VR_PVVIS_RP11V	8	65			PV VIS regulated +11V of A_1 or B_7 C&B-ACE pwb	HK	C0003/C0004	0371	0/6	14
11	PV	TA_PVVIS_PWB1_7	9	65			PV VIS Temp of A_1 or B_7 C&B-ACE pwb	HK	C0003/C0004	0371	0/6	15
11	PV	VR_PVNIR_VDET	8	1.5			PV NIR SCA VDET bias of A_2 or B_8 C&B-ACE pwb	SCI	C0003/C0004	0371	1/7	0
11	PV	VR_PVNIR_VDDA	8	1.5			PV NIR SCA VDDA bias of A_2 or B_8 C&B-ACE pwb	SCI	C0003/C0004	0371	1/7	1
11	PV	VR_PVNIR_ITWKA	8	1.5			PV NIR SCA ITWKA bias of A_2 or B_8 C&B-ACE pwb	SCI	C0003/C0004	0371	1/7	2
11	PV	VR_PVNIR_VD1	8	1.5			PV NIR SCA VD1 bias of A_2 or B_8 C&B-ACE pwb	SCI	C0003/C0004	0371	1/7	3

TABLE 20-3. FAM (PC) & SAM (PV) MUX DATA LOCATION

5/97

chg	1 Subsystem	2 Mnemonic Name	3 # of Bits	4 Sample Rate	5 N/A	6 N/A	7 Remarks	8 Type Data	9 TM HW Addr/Read	10 TM HW Data	11 PWB Mux	12 Mux Step
	This table is of primary interest to HW/SW development, integration & test -- See Notes at table bottom for description of columns.											
11	PV	VR_PVNIR_VGUARD	8	1.5			PV NIR SCA VGUARD bias of A_2 or B_8 C&B-ACE pwb	SCI	C0003/C0004	0371	1/7	4
2,11	PV	CR_PVNIR_S_DELAY	8	1.5			PV NIR sample delay of A_2 or B_8 C&B-ACE pwb in D#0-63 units of 3.33µs steps for registration (msb bits 7&8=0 for D#63 limit)	SCI	C0003/C0004	0371	1/7	5
11	PV	VR_PVNIR_VCAL	8	1.5			PV NIR SCA VCAL(ECAL) bias of A_2 or B_8 C&B-ACE pwb	SCI	C0003/C0004	0371	1/7	6
11	PV	VR_PVNIR_VDDD	8	1.5			PV NIR SCA VDDD bias of A_2 or B_8 C&B-ACE pwb	SCI	C0003/C0004	0371	1/7	7
11	PV	VR_PVNIR_VPWELL	8	1.5			PV NIR SCA VPWELL bias of A_2 or B_8 C&B-ACE pwb	SCI	C0003/C0004	0371	1/7	8
11	PV	VR_PVNIR_VDDOUT	8	1.5			PV NIR SCA VDDOUT bias of A_2 or B_8 C&B-ACE pwb	SCI	C0003/C0004	0371	1/7	9
11	PV	VR_PVNIR_P30V	8	65			PV NIR +30V of A_1 or B_7 C&B-ACE pwb	HK	C0003/C0004	0371	1/7	10
11	PV	VR_PVNIR_RN5V2_8	8	65			PV NIR regulated -5V of A_2 or B_8 C&B-ACE pwb	HK	C0003/C0004	0371	1/7	11
11	PV	VR_PVNIR_RN11V28	8	65			PV NIR regulated -11V of A_2 or B_8 C&B-ACE pwb	HK	C0003/C0004	0371	1/7	12
11	PV	VR_PVNIR_RP5V2_8	8	65			PV NIR regulated +5V of A_2 or B_8 C&B-ACE pwb	HK	C0003/C0004	0371	1/7	13
11	PV	VR_PVNIR_RP11V28	8	65			PV NIR regulated +11V of A_2 or B_8 C&B-ACE pwb	HK	C0003/C0004	0371	1/7	14
11	PV	TA_PVNIR_PWB2_8	9	65			PV NIR Temp of A_2 or B_8 C&B-ACE pwb	HK	C0003/C0004	0371	1/7	15
11	PV	VR_PVNIR_RP11V39	8	65			PV NIR regulated +11V of A_3 or B_9 ACE-ACE pwb	HK	C0003/C0004	0371	2/8	3
11	PV	VR_PVNIR_RN11V39	8	65			PV NIR regulated -11V of A_3 or B_9 ACE-ACE pwb	HK	C0003/C0004	0371	2/8	4
11	PV	VR_PVNIR_RP5V3_9	8	65			PV NIR regulated +5V of A_3 or B_9 ACE-ACE pwb	HK	C0003/C0004	0371	2/8	7
11	PV	VR_PVNIR_RN5V3_9	8	65			PV NIR regulated -5V of A_3 or B_9 ACE-ACE pwb	HK	C0003/C0004	0371	2/8	8
11	PV	VR_PVNIR_P5VD3_9	8	65			PV NIR digital +5V of A_3 or B_9 ACE-ACE pwb	HK	C0003/C0004	0371	2/8	11
11	PV	TA_PVNIR_PWB3_9	9	65			PV NIR Temp of A_3 or B_9 ACE-ACE pwb	HK	C0003/C0004	0371	2/8	12
11	PV	VR_PVLW_VDET	8	1.5			PV LWIR SCA VDET bias of A_4 or B_10 C&B-ACE pwb	SCI	C0003/C0004	0371	3/9	0
11	PV	VR_PVLW_VDDA	8	1.5			PV LWIR SCA VDDA bias of A_4 or B_10 C&B-ACE pwb	SCI	C0003/C0004	0371	3/9	1
11	PV	VR_PVLW_ITWKA	8	1.5			PV LWIR SCA ITWKA bias of A_4 or B_10 C&B-ACE pwb	SCI	C0003/C0004	0371	3/9	2
11	PV	CR_PVLW_S_DELAY	8	1.5			PV LWIR sample delay of A_4 or B_10 C&B-ACE pwb in D#0-63 units of 3.33µs steps for registration (msb bits 7&8=0 for D#63 limit)	SCI	C0003/C0004	0371	3/9	5
11	PV	VR_PVLW_VCAL	8	1.5			PV LWIR SCA VCAL(ECAL) bias of A_4 or B_10 C&B-ACE pwb	SCI	C0003/C0004	0371	3/9	6
11	PV	VR_PVLW_VDDD	8	1.5			PV LWIR SCA VDDD bias of A_4 or B_10 C&B-ACE pwb	SCI	C0003/C0004	0371	3/9	7
11	PV	VR_PVLW_VPWELL	8	1.5			PV LWIR SCA VPWELL bias of A_4 or B_10 C&B-ACE pwb	SCI	C0003/C0004	0371	3/9	8
11	PV	VR_PVLW_VDDOUT	8	1.5			PV LWIR SCA VDDOUT bias of A_4 or B_10 C&B-ACE pwb	SCI	C0003/C0004	0371	3/9	9
11	PV	VR_PVLW_P30V	8	65			PV LWIR +30V of A_4 or B_10 C&B-ACE pwb	HK	C0003/C0004	0371	3/9	10
11	PV	VR_PVLW_RN5V	8	65			PV LWIR regulated -5V of A_4 or B_10 C&B-ACE pwb	HK	C0003/C0004	0371	3/9	11
11	PV	VR_PVLW_RN11V	8	65			PV LWIR regulated -11V of A_4 or B_10 C&B-ACE pwb	HK	C0003/C0004	0371	3/9	12
11	PV	VR_PVLW_RP5V	8	65			PV LWIR regulated +5V of A_4 or B_10 C&B-ACE pwb	HK	C0003/C0004	0371	3/9	13
11	PV	VR_PVLW_RP11V	8	65			PV LWIR regulated +11V of A_4 or B_10 C&B-ACE pwb	HK	C0003/C0004	0371	3/9	14
11	PV	TA_PVLW_PWB4_10	9	65			PV LWIR temp of A_4 or B_10 C&B-ACE pwb	HK	C0003/C0004	0371	3/9	15
11	PV	VR_PVSM_VDET	8	1.5			PV SMIR SCA VDET bias of A_5 or B_11 C&B pwb	SCI	C0003/C0004	0371	4/10	0
11	PV	VR_PVSM_VDDA	8	1.5			PV SMIR SCA VDDA bias of A_5 or B_11 C&B pwb	SCI	C0003/C0004	0371	4/10	1
11	PV	VR_PVSM_ITWKA	8	1.5			PV SMIR SCA ITWKA bias of A_5 or B_11 C&B pwb	SCI	C0003/C0004	0371	4/10	2
11	PV	CR_PVSM_S_DELAY	8	1.5			PV SMIR sample delay of A_5 or B_11 C&B pwb in D#0-63 units of 3.33µs steps for registration (msb bits 7&8=0 for D#63 limit)	SCI	C0003/C0004	0371	4/10	5
11	PV	VR_PVSM_VCAL	8	1.5			PV SMIR SCA VCAL(ECAL) bias of A_5 or B_11 C&B pwb	SCI	C0003/C0004	0371	4/10	6

TABLE 20-3. FAM (PC) & SAM (PV) MUX DATA LOCATION

5/97

chg	1 Subsystem	2 Mnemonic Name	3 # of Bits	4 Sample Rate	5 N/A	6 N/A	7 Remarks	8 Type Data	9 TM HW Addr/Read	10 TM HW Data	11 PWB Mux	12 Mux Step
	This table is of primary interest to HW/SW development, integration & test - - See Notes at table bottom for description of columns.											
11	PV	VR_PVSM_VDDD	8	1.5			PV SMIR SCA VDDD bias of A_5 or B_11 C&B pwb	SCI	C0003/C0004	0371	4/10	7
11	PV	VR_PVSM_VPWELL	8	1.5			PV SMIR SCA VPWELL bias of A_5 or B_11 C&B pwb	SCI	C0003/C0004	0371	4/10	8
11	PV	VR_PVSM_VDDOUT	8	1.5			PV SMIR SCA VDDOUT bias of A_5 or B_11 C&B pwb	SCI	C0003/C0004	0371	4/10	9
11	PV	VR_PVSM_P30V	8	65			PV SMIR regulated +30V of A_5 or B_11 C&B pwb	HK	C0003/C0004	0371	4/10	10
11	PV	VR_PVSM_RN5V5_11	8	65			PV SMIR regulated -5V of A_5 or B_11 C&B pwb	HK	C0003/C0004	0371	4/10	11
11	PV	VR_PVSM_RN11V511	8	65			PV SMIR regulated -11V of A_5 or B_11 C&B pwb	HK	C0003/C0004	0371	4/10	12
11	PV	VR_PVSM_RP5V5_11	8	65			PV SMIR regulated +5V of A_5 or B_11 C&B pwb	HK	C0003/C0004	0371	4/10	13
11	PV	VR_PVSM_RP11V511	8	65			PV SMIR regulated +11V of A_5 or B_11 C&B pwb	HK	C0003/C0004	0371	4/10	14
11	PV	TA_PVSM_PWB5_11	9	65			PV SMIR Temp of A_5 or B_11 C&B pwb	HK	C0003/C0004	0371	4/10	15
11	PV	VR_PVSM_RP11V612	8	65			PV SMIR regulated +11V of A_6 or B_12 ACE-ACE pwb	HK	C0003/C0004	0371	5/11	3
11	PV	VR_PVSM_RN11V612	8	65			PV SMIR regulated -11V of A_6 or B_12 ACE-ACE pwb	HK	C0003/C0004	0371	5/11	4
11	PV	VR_PVSM_RP5V6_12	8	65			PV SMIR regulated +5V of A_6 or B_12 ACE-ACE pwb	HK	C0003/C0004	0371	5/11	7
11	PV	VR_PVSM_RN5V6_12	8	65			PV SMIR regulated -5V of A_6 or B_12 ACE-ACE pwb	HK	C0003/C0004	0371	5/11	8
11	PV	VR_PVSM_P5VD6_12	8	65			PV SMIR digital +5V of A_6 or B_12 ACE-ACE pwb	HK	C0003/C0004	0371	5/11	11
11	PV	TA_PVSM_PWB6_12	9	65			PV SMIR Temp of A_6 or B_12 ACE-ACE pwb	HK	C0003/C0004	0371	5/11	12
	168	***<--List Total***										

Notes:

1. Columns 1 - 4, 7, 9 & 10 have the same meaning as in Table 20-2A. Columns 5 & 6 are not used.

2. Column 8 indicates the type of data since this table is a mix of housekeeping & science engineering data that originates in the FAM & SAM muxes.

3. Columns 9 & 10 are hex address & data locations on the analog telemetry PWB (as indicated in Tables 20-2A, 20-2B & 30-5C).

4. Columns 11 & 12 identify mux data locations by decimal numbers. Both the FAM & SAM muxes have 16 input ports. The FAM has 6 individual analog muxes. The SAM has one mux with equivalent extensions for each pwb. The mux ports are not directly addressable. After a common mux reset, data is sequentially accessed by a step control line. All FAM ports are used. Some SAM ports are not used (only NIR & SMIR have 2 PWBs each, hence missing step points for VIS & LWIR). Note, the FAM & SAM have the same relative data stepping ID's of 0-15, but different style PWB Mux ID's (FAM 1-6, SAM 0-11).

TABLE 20-4. MODIS TELEMETRY FRAME DEFINITION

See Notes below for how 1553 bus telemetry frame was developed. True sample periods are 1.024 sec, 8.192 sec & 65.536 sec.

5/97

pfm chg#	FB	1 Subsystem	2 Mnemonic Name	3 # of Bits	4 Sample Period	5 Major Cycle (0 - 63)	6 Major Cyc Start Bit	7 Group Start Bit	8 Cum Group Bits Used	9 Group 16bit Words	10 Tlmy Type	11 HW Addr Write/Read	12 HW Data Loc
	0	CP	SS_CP1553_MAJCYC	6	1	all	0	0	6		SW	na	na
		CP	SS_CP_CMD_ECHO	16	1	all	6	6	22		SW	na	na
		CP	SS_CP_LOG_EVENT	1	1	all	22	22	23		SW	na	na
		CP	SS_CP_MODE	3	1	all	23	23	26		SW	na	na
2		CP	SS_CP_MODECHG_GO	1	1	all	26	26	27		SW	na	na
		CP	SS_CP_SPARE	8	1	all	27	27	35		SW	na	na
		CP	SS_CP_VALTLM_COL	1	1	all	35	35	36		SW	na	na
		CP	SS_CP_VALTLM_FMT	1	1	all	36	36	37		SW	na	na
38		DR	SS_DR_NAD_STEP	13	1	all	37	37	50		SW	na	na
38		DR	SS_DR_SPARE	9	1	all	50	50	59		SW	na	na
38		DR	SS_DR_SVD_STEP	13	1	all	59	59	72		SW	na	na
21		FR	CS_FR_BBRADTAB	1	1	all	72	72	73		SW	na	na
		FR	SS_FR_LOG_EVENT	1	1	all	73	73	74		SW	na	na
		PS	IR_PS1_INPUT_CUR	10	1	all	74	74	84		A	C0003/C0004	6EF6
		PS	IR_PS2_INPUT_CUR	10	1	all	84	84	94		A	C0003/C0004	75F7
		RC	TA_RC_LWIR_CFPA	12	1	all	94	94	106		A	C0003/C0004	5E75
		RC	TA_RC_SMIR_CFPA	12	1	all	106	106	118		A	C0003/C0004	5DF5
		SA	SD_SA_APX_PERIOD	12	1	all	118	118	130		SW	na	na
		SM	CR_SM_MIR_HOME_A	1	1	all	130	130	131		DCE	C0001	6
		SM	CR_SM_MIR_HOME_B	1	1	all	131	131	132		DCE	C0001	7
		SM	CS_SM_MIR_STEP	7	1	all	132	132	139		SW	na	na
		SR	CR_SR_GRAT_CH_A	1	1	all	139	139	140		DCE	C0001	8
		SR	CR_SR_GRAT_CH_B	1	1	all	140	140	141		DCE	C0001	C
		SR	CR_SR_GRAT_FH_A	1	1	all	141	141	142		DCE	C0001	9
		SR	CR_SR_GRAT_FH_B	1	1	all	142	142	143		DCE	C0001	D
		SR	CR_SR_IR_SRC_OFF	1	1	all	143	143	144		DCE	C0001	1
		SR	CR_SR_SISHTR_OFF	1	1	all	144	144	145		DCE	C0001	2
19,21		FR	CS_FR_GAINTAB	1	1	all	145	145	146		SW	na	na
		SR	CR_SR_SLIT_HOMEA	1	1	all	146	146	147		DCE	C0001	A
		SR	CR_SR_SLIT_HOMEB	1	1	all	147	147	148		DCE	C0001	E
		SR	CR_SR_WHL_HOMEA	1	1	all	148	148	149		DCE	C0001	B
		SR	CR_SR_WHL_HOMEB	1	1	all	149	149	150		DCE	C0001	F
		SR	CS_SR_GRAT_STEP	16	1	all	150	150	166		SW	na	na
		SR	CS_SR_SLIT_STEP	6	1	all	166	166	172		SW	na	na
		SR	CS_SR_SRCWH_STEP	7	1	all	172	172	179		SW	na	na
20		SR	CS_SR_LAMPS	3	1	all	179	179	182		SW	na	na
20		CP	SS_CP_LAST_EVENT	16	1	all	182	182	198		SW	na	na
20		FR	SS_FR_LAST_EVENT	16	1	all	198	198	214		SW	na	na
21		CP	SS_CP_TC1_DAYS	16	1	all	214	214	230		SW	na	na
21		CP	SS_CP_TC2_MILLIS	16	1	all	230	230	246		SW	na	na

FRAME BOUNDARIES

TABLE 20-4. MODIS TELEMETRY FRAME DEFINITION

See Notes below for how 1553 bus telemetry frame was developed. True sample periods are 1.024 sec, 8.192 sec & 65.536 sec. *5/97*

pfm chg#	FB	1 Subsystem	2 Mnemonic Name	3 # of Bits	4 Sample Period	5 Major Cycle (0 - 63)	6 Major Cyc Start Bit	7 Group Start Bit	8 Cum Group Bits Used	9 Group 16bit Words	10 Tlmy Type	11 HW Addr Write/Read	12 HW Data Loc
21		CP	SS_CP_TC3_MILLIS	16	1	all	246	246	262		SW	na	na
21		CP	SS_CP_TC4_MICROS	16	1	all	262	262	278		SW	na	na
20		FR	CS_FR_OFFSETTAB	1	1	all	278	278	279		SW	na	na
32		CP	SS_CP_MACRO_ID	5	1	all	279	279	284		SW	na	na
32		CP	SS_CP_MACRO_ON	1	1	all	284	284	285		SW	na	na
38		DR	SS_DR_SDD_STEP	12	1	all	285	285	297		SW	na	na
21,38	**319**	**XX**	**1 SEC FRAME FILL**	**23**	**1**	**all**	**297**	**297**	**320**	**20**			
	320	BB	CR_BB_A_PWR_ON	1	8	0 8 16 24 32 40 48 56	320	0	1		D	40005	E
		BB	CR_BB_B_PWR_ON	1	8	0 8 16 24 32 40 48 56	321	1	2		D	40005	F
		BB	CR_BB_SPARE	1	8	0 8 16 24 32 40 48 56	322	2	3		DCE	C0001	0
		BB	CS_BB_TEMP_SET	12	8	0 8 16 24 32 40 48 56	323	3	15		SW	na	na
		BB	IR_BB_HTRA_CURH	8	8	0 8 16 24 32 40 48 56	335	15	23		SW	na	na
		BB	IR_BB_HTRB_CURH	8	8	0 8 16 24 32 40 48 56	343	23	31		SW	na	na
		BB	TP_BB_TEMP01H	12	8	0 8 16 24 32 40 48 56	351	31	43		SW	na	na
		BB	TP_BB_TEMP02H	12	8	0 8 16 24 32 40 48 56	363	43	55		SW	na	na
		BB	TP_BB_TEMP03H	12	8	0 8 16 24 32 40 48 56	375	55	67		SW	na	na
		BB	TP_BB_TEMP04H	12	8	0 8 16 24 32 40 48 56	387	67	79		SW	na	na
		BB	TP_BB_TEMP05H	12	8	0 8 16 24 32 40 48 56	399	79	91		SW	na	na
		BB	TP_BB_TEMP06H	12	8	0 8 16 24 32 40 48 56	411	91	103		SW	na	na
		BB	TP_BB_TEMP07H	12	8	0 8 16 24 32 40 48 56	423	103	115		SW	na	na
		BB	TP_BB_TEMP08H	12	8	0 8 16 24 32 40 48 56	435	115	127		SW	na	na
	447	**XX**	**8 SEC FRAME FILL**	**1**	**8**	**0 8 16 24 32 40 48 56**	**447**	**127**	**128**	**8**			
	320	BB	TP_BB_TEMP09H	12	8	1 9 17 25 33 41 49 57	320	0	12		SW	na	na
		BB	TP_BB_TEMP10H	12	8	1 9 17 25 33 41 49 57	332	12	24		SW	na	na
		BB	TP_BB_TEMP11H	12	8	1 9 17 25 33 41 49 57	344	24	36		SW	na	na
		BB	TP_BB_TEMP12H	12	8	1 9 17 25 33 41 49 57	356	36	48		SW	na	na
		CE	CR_CE_A_ON	1	8	1 9 17 25 33 41 49 57	368	48	49		D	C000E	C
		CE	CR_CE_B_ON	1	8	1 9 17 25 33 41 49 57	369	49	50		D	C000E	D
		CP	CR_CPA_EEP_WRE_M	1	8	1 9 17 25 33 41 49 57	370	50	51		D	C000E	E
		CP	CR_CPB_EEP_WRE_M	1	8	1 9 17 25 33 41 49 57	371	51	52		D	C000E	F
		CP	CR_CP_A_ON_M	1	8	1 9 17 25 33 41 49 57	372	52	53		D	C000E	4
		CP	CR_CP_B_ON_M	1	8	1 9 17 25 33 41 49 57	373	53	54		D	C000E	5
		CP	CR_CP_SET_TMF_A	1	8	1 9 17 25 33 41 49 57	374	54	55		D	C000B	0
33		CP	CS_CP_SPARE	12	8	1 9 17 25 33 41 49 57	375	55	67		SW	na	na
		CP	SS_CP_IMOK_ON	1	8	1 9 17 25 33 41 49 57	387	67	68		SW	na	na
22		CP	SS_CP_SPARE	1	8	1 9 17 25 33 41 49 57	388	68	69		SW	na	na
22		CP	SS_CP_SPARE	1	8	1 9 17 25 33 41 49 57	389	69	70		SW	na	na
		CP	SS_CP_RESET_SRC	3	8	1 9 17 25 33 41 49 57	390	70	73		SW	na	na
21		CP	SS_CP_SCAN_EST	16	8	1 9 17 25 33 41 49 57	393	73	89		SW	na	na
24		CP	SS_CP_LOG_STATE	4	8	1 9 17 25 33 41 49 57	409	89	93		SW	na	na

TABLE 20-4. MODIS TELEMETRY FRAME DEFINITION

See Notes below for how 1553 bus telemetry frame was developed. True sample periods are 1.024 sec, 8.192 sec & 65.536 sec.

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pfm chg#	FB	1 Subsystem	2 Mnemonic Name	3 # of Bits	4 Sample Period	5 Major Cycle (0 - 63)								6 Major Cyc Start Bit	7 Group Start Bit	8 Cum Group Bits Used	9 Group 16bit Words	10 Tlmy Type	11 HW Addr Write/Read	12 HW Data Loc
24		FR	SS_FR_LOG_STATE	4	8	1	9	17	25	33	41	49	57	413	93	97		SW	na	na
24,33,36		FR	SS_FR_SCIABNORM	1	8	1	9	17	25	33	41	49	57	417	97	98		SW	na	na
24,33		FR	CS_FR_SPARE	1	8	1	9	17	25	33	41	49	57	418	98	99		SW	na	na
24,33		FR	CS_FR_SPARE	1	8	1	9	17	25	33	41	49	57	419	99	100		SW	na	na
24		CP	SS_CP_STATUS_04	16	8	1	9	17	25	33	41	49	57	420	100	116		SW	na	na
21	**447**	**XX**	**8 SEC FRAME FILL**	**12**	**8**	**1**	**9**	**17**	**25**	**33**	**41**	**49**	**57**	436	116	128		SW	na	na
	320	CP	SS_CP_STATUS_05	16	8	2	10	18	26	34	42	50	58	320	0	16		SW	na	na
		CP	SS_CP_STATUS_06	16	8	2	10	18	26	34	42	50	58	336	16	32		SW	na	na
		CP	SS_CP_STATUS_07	16	8	2	10	18	26	34	42	50	58	352	32	48		SW	na	na
		CP	SS_CP_STATUS_08	16	8	2	10	18	26	34	42	50	58	368	48	64		SW	na	na
		CP	SS_CP_STATUS_09	16	8	2	10	18	26	34	42	50	58	384	64	80		SW	na	na
21		CP	SS_CP_UART_RESET	16	8	2	10	18	26	34	42	50	58	400	80	96		SW	na	na
21		CP	SS_CP_UART_HUNT	16	8	2	10	18	26	34	42	50	58	416	96	112		SW	na	na
21	**447**	**CP**	**SS_CP_UART_SYNC**	**16**	**8**	**2**	**10**	**18**	**26**	**34**	**42**	**50**	**58**	**432**	**112**	**128**	**8**	SW	na	na
21	**320**	CP	SS_CP_UART_NORM	16	8	3	11	19	27	35	43	51	59	320	0	16		SW	na	na
22		CP	SS_CP_SPARE	1	8	3	11	19	27	35	43	51	59	336	16	17		SW	na	na
		CP	SS_CP_TMF_GONE	1	8	3	11	19	27	35	43	51	59	337	17	18		SW	na	na
		DR	CR_DR_DRV_ON	1	8	3	11	19	27	35	43	51	59	338	18	19		D	C0010	3
		DR	CR_DR_FS_ENABL_M	1	8	3	11	19	27	35	43	51	59	339	19	20		D	C0010	B
		DR	CR_DR_FS_SW_CLSD	1	8	3	11	19	27	35	43	51	59	340	20	21		D	C0010	4
		DR	CR_DR_NAD_CLSD	1	8	3	11	19	27	35	43	51	59	341	21	22		D	C0012	A
		DR	CR_DR_NAD_FS_ON	1	8	3	11	19	27	35	43	51	59	342	22	23		D	C0010	6
		DR	CR_DR_NAD_OPEN	1	8	3	11	19	27	35	43	51	59	343	23	24		D	C0012	B
		DR	CR_DR_PRI_FS_SEL	1	8	3	11	19	27	35	43	51	59	344	24	25		D	C0010	A
		DR	CR_DR_SDD_CLSD	1	8	3	11	19	27	35	43	51	59	345	25	26		D	C0012	C
		DR	CR_DR_SDD_DRV_A	1	8	3	11	19	27	35	43	51	59	346	26	27		D	C0010	2
		DR	CR_DR_SDD_OPEN	1	8	3	11	19	27	35	43	51	59	347	27	28		D	C0012	D
		DR	CR_DR_SDFS_DRVON	1	8	3	11	19	27	35	43	51	59	348	28	29		D	C0010	7
19		DR	CR_DR_SPARE	1	8	3	11	19	27	35	43	51	59	349	29	30		D	C0012	E
		DR	CR_DR_SDS_OPEN	1	8	3	11	19	27	35	43	51	59	350	30	31		D	C0012	F
		DR	CR_DR_SVD_CLSD	1	8	3	11	19	27	35	43	51	59	351	31	32		D	C0012	8
		DR	CR_DR_SVD_FS_ON	1	8	3	11	19	27	35	43	51	59	352	32	33		D	C0010	5
		DR	CR_DR_SVD_OPEN	1	8	3	11	19	27	35	43	51	59	353	33	34		D	C0012	9
		DR	CR_DR_UNLACH_AON	1	8	3	11	19	27	35	43	51	59	354	34	35		D	C0010	0
		DR	CR_DR_UNLACH_BON	1	8	3	11	19	27	35	43	51	59	355	35	36		D	C0010	1
		DR	CS_DR_SVD_AT_OG	1	8	3	11	19	27	35	43	51	59	356	36	37		SW		
13		DR	TP_DR_NAD_FS	9	8	3	11	19	27	35	43	51	59	357	37	46		P	C0003/C0004	169B
13		DR	TP_DR_SPARE	9	8	3	11	19	27	35	43	51	59	366	46	55		P	C0003/C0004	171B
13		DR	TP_DR_SVD_FS	9	8	3	11	19	27	35	43	51	59	375	55	64		P	C0003/C0004	159B
		FI	CR_FI_A_ON	1	8	3	11	19	27	35	43	51	59	384	64	65		D	C0011	4

TABLE 20-4. MODIS TELEMETRY FRAME DEFINITION

See Notes below for how 1553 bus telemetry frame was developed. True sample periods are 1.024 sec, 8.192 sec & 65.536 sec.

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pfm chg#	FB	1 Subsystem	2 Mnemonic Name	3 # of Bits	4 Sample Period	5 Major Cycle (0 - 63)	6 Major Cyc Start Bit	7 Group Start Bit	8 Cum Group Bits Used	9 Group 16bit Words	10 Tlmy Type	11 HW Addr Write/Read	12 HW Data Loc
38		FI	CR_FI_PORT_A_ON	1	8	3 11 19 27 35 43 51 59	385	65	66		D	C0011	5
		FI	CR_FI_A_RESET	1	8	3 11 19 27 35 43 51 59	386	66	67		D	C0011	7
		FI	CR_FI_B_ON	1	8	3 11 19 27 35 43 51 59	387	67	68		D	C0011	8
38		FI	CR_FI_PORT_B_ON	1	8	3 11 19 27 35 43 51 59	388	68	69		D	C0011	9
		FI	CR_FI_B_RESET	1	8	3 11 19 27 35 43 51 59	389	69	70		D	C0011	B
		FO	CR_FO_BLK1_ON	1	8	3 11 19 27 35 43 51 59	390	70	71		D	C000D	8
9		FO	CR_FO_SPARE	1	8	3 11 19 27 35 43 51 59	391	71	72		D	C000D	C
		FO	CR_FO_BLK2_ON	1	8	3 11 19 27 35 43 51 59	392	72	73		D	C000D	9
9		FO	CR_FO_SPARE	1	8	3 11 19 27 35 43 51 59	393	73	74		D	C000D	D
		FO	CR_FO_BLK3_ON	1	8	3 11 19 27 35 43 51 59	394	74	75		D	C000D	A
9		FO	CR_FO_SPARE	1	8	3 11 19 27 35 43 51 59	395	75	76		D	C000D	E
		FO	CR_FO_BLK4_ON	1	8	3 11 19 27 35 43 51 59	396	76	77		D	C000D	B
9,21		FR	CS_FR_SCI_NORMAL	1	8	3 11 19 27 35 43 51 59	397	77	78		D	C000D	F
		FO	SR_FO_BLK1_MODE	1	8	3 11 19 27 35 43 51 59	398	78	79		D	C000E	0
		FO	SR_FO_BLK2_MODE	1	8	3 11 19 27 35 43 51 59	399	79	80		D	C000E	1
		FO	SR_FO_BLK3_MODE	1	8	3 11 19 27 35 43 51 59	400	80	81		D	C000E	2
		FO	SR_FO_BLK4_MODE	1	8	3 11 19 27 35 43 51 59	401	81	82		D	C000E	3
		FR	CR_FRA_EEP_WRE	1	8	3 11 19 27 35 43 51 59	402	82	83		D	C0011	F
		FR	CR_FRB_EEP_WRE	1	8	3 11 19 27 35 43 51 59	403	83	84		D	C0012	0
		FR	CR_FR_A_ON	1	8	3 11 19 27 35 43 51 59	404	84	85		D	C0011	D
		FR	CR_FR_A_RESET	1	8	3 11 19 27 35 43 51 59	405	85	86		D	C0011	E
		FR	CR_FR_B_ON	1	8	3 11 19 27 35 43 51 59	406	86	87		D	C0012	2
		FR	CR_FR_B_RESET	1	8	3 11 19 27 35 43 51 59	407	87	88		D	C0012	3
		FR	CS_FR_DAY_RATE	1	8	3 11 19 27 35 43 51 59	408	88	89		SW	na	na
		FR	CS_FR_DELAY_BB	7	8	3 11 19 27 35 43 51 59	409	89	96		SW	na	na
		FR	CS_FR_DELAY_EA	7	8	3 11 19 27 35 43 51 59	416	96	103		SW	na	na
		FR	CS_FR_DELAY_SD	7	8	3 11 19 27 35 43 51 59	423	103	110		SW	na	na
		FR	CS_FR_DELAY_SP	7	8	3 11 19 27 35 43 51 59	430	110	117		SW	na	na
		FR	CS_FR_DELAY_SR	7	8	3 11 19 27 35 43 51 59	437	117	124		SW	na	na
21		SR	CR_SR_LAMPS_LOW	1	8	3 11 19 27 35 43 51 59	444	124	125		SW	na	na
		FR	SR_FR_A_MODELONG	1	8	3 11 19 27 35 43 51 59	445	125	126		D	C0011	C
		FR	SR_FR_B_MODELONG	1	8	3 11 19 27 35 43 51 59	446	126	127		D	C0012	1
22	**447**	**FR**	**SS_FR_SPARE**	**1**	**8**	**3 11 19 27 35 43 51 59**	**447**	**127**	**128**	**8**	SW	na	na
22	**320**	FR	SS_FR_SPARE	1	8	4 12 20 28 36 44 52 60	320	0	1		SW	na	na
21,26		FR	SS_FR_PKT_TYPE	1	8	4 12 20 28 36 44 52 60	321	1	2		SW	na	na
		FR	SS_FR_RESET_SRC	3	8	4 12 20 28 36 44 52 60	322	2	5		SW	na	na
22		FR	SS_FR_SPARE	1	8	4 12 20 28 36 44 52 60	325	5	6		SW	na	na
30		PC	CS_PC_3132_SRISE	8	8	4 12 20 28 36 44 52 60	326	6	14		SW	na	na
30		PC	CS_PC_3132_SFALL	8	8	4 12 20 28 36 44 52 60	334	14	22		SW	na	na
30		PC	CS_PC_3334_SRISE	8	8	4 12 20 28 36 44 52 60	342	22	30		SW	na	na

TABLE 20-4. MODIS TELEMETRY FRAME DEFINITION

See Notes below for how 1553 bus telemetry frame was developed. True sample periods are 1.024 sec, 8.192 sec & 65.536 sec.

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pfm chg#	FB	1 Subsystem	2 Mnemonic Name	3 # of Bits	4 Sample Period	5 Major Cycle (0 - 63)	6 Major Cyc Start Bit	7 Group Start Bit	8 Cum Group Bits Used	9 Group 16bit Words	10 Tlmy Type	11 HW Addr Write/Read	12 HW Data Loc
30		PC	CS_PC_3334_SFALL	8	8	4 12 20 28 36 44 52 60	350	30	38		SW	na	na
30		PC	CS_PC_3536_SRISE	8	8	4 12 20 28 36 44 52 60	358	38	46		SW	na	na
30		PC	CS_PC_3536_SFALL	8	8	4 12 20 28 36 44 52 60	366	46	54		SW	na	na
		PC	CR_PCLWA_ECAL_ON	1	8	4 12 20 28 36 44 52 60	374	54	55		D	C000C	1
		PC	CR_PCLWB_ECAL_ON	1	8	4 12 20 28 36 44 52 60	375	55	56		D	C000C	3
		PC	CR_PCLW_A_ON	1	8	4 12 20 28 36 44 52 60	376	56	57		D	C000C	0
		PC	CR_PCLW_B_ON	1	8	4 12 20 28 36 44 52 60	377	57	58		D	C000C	2
		PS	CR_PS1SHDN_ENA_M	1	8	4 12 20 28 36 44 52 60	378	58	59		D	C000C	8
		PS	CR_PS2SHDN_ENA_M	1	8	4 12 20 28 36 44 52 60	379	59	60		D	C000C	F
		PV	CR_PVLWA_CSUB_ON	1	8	4 12 20 28 36 44 52 60	380	60	61		D	C000F	8
		PV	CR_PVLWA_ECAL_ON	1	8	4 12 20 28 36 44 52 60	381	61	62		D	C000C	A
		PV	CR_PVLWB_CSUB_ON	1	8	4 12 20 28 36 44 52 60	382	62	63		D	C000F	9
		PV	CR_PVLWB_ECAL_ON	1	8	4 12 20 28 36 44 52 60	383	63	64		D	C000D	3
		PV	CR_PVLW_A_ON	1	8	4 12 20 28 36 44 52 60	384	64	65		D	C000C	9
		PV	CR_PVLW_B_ON	1	8	4 12 20 28 36 44 52 60	385	65	66		D	C000D	2
		PV	CR_PVLW_S_DELAYH	8	8	4 12 20 28 36 44 52 60	386	66	74		SW	na	na
		PV	CR_PVNIRA_ECALON	1	8	4 12 20 28 36 44 52 60	394	74	75		D	C000C	7
		PV	CR_PVNIRB_ECALON	1	8	4 12 20 28 36 44 52 60	395	75	76		D	C000D	1
		PV	CR_PVNIR_A_ON	1	8	4 12 20 28 36 44 52 60	396	76	77		D	C000C	6
		PV	CR_PVNIR_B_ON	1	8	4 12 20 28 36 44 52 60	397	77	78		D	C000D	0
3		PV	CR_PVNIR_S_DELYH	8	8	4 12 20 28 36 44 52 60	398	78	86		SW	na	na
		PV	CR_PVSMA_CSUB_ON	1	8	4 12 20 28 36 44 52 60	406	86	87		D	C000F	A
		PV	CR_PVSMA_ECAL_ON	1	8	4 12 20 28 36 44 52 60	407	87	88		D	C000C	C
		PV	CR_PVSMB_CSUB_ON	1	8	4 12 20 28 36 44 52 60	408	88	89		D	C000F	B
		PV	CR_PVSMB_ECAL_ON	1	8	4 12 20 28 36 44 52 60	409	89	90		D	C000D	5
		PV	CR_PVSM_A_ON	1	8	4 12 20 28 36 44 52 60	410	90	91		D	C000C	B
		PV	CR_PVSM_B_ON	1	8	4 12 20 28 36 44 52 60	411	91	92		D	C000D	4
		PV	CR_PVSM_S_DELAYH	8	8	4 12 20 28 36 44 52 60	412	92	100		SW	na	na
		PV	CR_PVVISA_ECALON	1	8	4 12 20 28 36 44 52 60	420	100	101		D	C000C	5
31		PV	CR_PVVISB_ECALON	1	8	4 12 20 28 36 44 52 60	421	101	102		D	C000C	E
		PV	CR_PVVIS_A_ON	1	8	4 12 20 28 36 44 52 60	422	102	103		D	C000C	4
31		PV	CR_PVVIS_B_ON	1	8	4 12 20 28 36 44 52 60	423	103	104		D	C000C	D
3		PV	CR_PVVIS_S_DELYH	8	8	4 12 20 28 36 44 52 60	424	104	112		SW	na	na
		PV	CR_PV_A_MEM_RAM	1	8	4 12 20 28 36 44 52 60	432	112	113		D	C0012	6
		PV	CR_PV_B_MEM_RAM	1	8	4 12 20 28 36 44 52 60	433	113	114		D	C0012	7
		PV	CR_PV_ECAL_ENA_A	1	8	4 12 20 28 36 44 52 60	434	114	115		D	C000D	6
		PV	CR_PV_ECAL_ENA_B	1	8	4 12 20 28 36 44 52 60	435	115	116		D	C000D	7
		PV	VR_PVLW_VCALH	8	8	4 12 20 28 36 44 52 60	436	116	124		SW	na	na
		FR	CS_FR_PC_DCR_ON	1	8	4 12 20 28 36 44 52 60	444	124	125		SW	na	na
		FR	CS_FR_PV_DCR_ON	1	8	4 12 20 28 36 44 52 60	445	125	126		SW	na	na

TABLE 20-4. MODIS TELEMETRY FRAME DEFINITION

See Notes below for how 1553 bus telemetry frame was developed. True sample periods are 1.024 sec, 8.192 sec & 65.536 sec.

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pfm chg#	1 FB	Subsystem	2 Mnemonic Name	3 # of Bits	4 Sample Period	5 Major Cycle (0 - 63)								6 Major Cyc Start Bit	7 Group Start Bit	8 Cum Group Bits Used	9 Group 16bit Words	10 Tlmy Type	11 HW Addr Write/Read	12 HW Data Loc
	447	**XX**	**8 SEC FRAME FILL**	**2**	**8**	**4**	**12**	**20**	**28**	**36**	**44**	**52**	**60**	**446**	**126**	**128**	**8**			
	320	PV	VR_PVNIR_VCALH	8	8	5	13	21	29	37	45	53	61	320	0	8		SW	na	na
		PV	VR_PVSM_VCALH	8	8	5	13	21	29	37	45	53	61	328	8	16		SW	na	na
		PV	VR_PVVIS_VCALH	8	8	5	13	21	29	37	45	53	61	336	16	24		SW	na	na
		RC	CR_RC_CFPA_T1SET	1	8	5	13	21	29	37	45	53	61	344	24	25		D	C000F	4
		RC	CR_RC_CFPA_T3SET	1	8	5	13	21	29	37	45	53	61	345	25	26		D	C000F	5
		RC	CR_RC_CSHTR_ON	1	8	5	13	21	29	37	45	53	61	346	26	27		D	C000F	0
		RC	CR_RC_CSTLM_ON	1	8	5	13	21	29	37	45	53	61	347	27	28		D	C000F	1
		RC	CR_RC_ISHTR_ON	1	8	5	13	21	29	37	45	53	61	348	28	29		D	C000F	6
		RC	CR_RC_ISTLM_ON	1	8	5	13	21	29	37	45	53	61	349	29	30		D	C000F	7
		RC	CR_RC_LWHTR_ON	1	8	5	13	21	29	37	45	53	61	350	30	31		D	C000F	E
		RC	CR_RC_LWTLM_ON	1	8	5	13	21	29	37	45	53	61	351	31	32		D	C000F	F
		RC	CR_RC_OSHTR_ON	1	8	5	13	21	29	37	45	53	61	352	32	33		D	C000F	2
		RC	CR_RC_OSTLM_ON	1	8	5	13	21	29	37	45	53	61	353	33	34		D	C000F	3
		RC	CR_RC_SMHTR_ON	1	8	5	13	21	29	37	45	53	61	354	34	35		D	C000F	C
		RC	CR_RC_SMTLM_ON	1	8	5	13	21	29	37	45	53	61	355	35	36		D	C000F	D
		SA	CR_SA_A_HI_GAIN	1	8	5	13	21	29	37	45	53	61	356	36	37		D	C000E	8
		SA	CR_SA_A_SCAN_ON	1	8	5	13	21	29	37	45	53	61	357	37	38		D	C000E	6
		SA	CR_SA_B_HI_GAIN	1	8	5	13	21	29	37	45	53	61	358	38	39		D	C000E	B
		SA	CR_SA_B_SCAN_ON	1	8	5	13	21	29	37	45	53	61	359	39	40		D	C000E	9
		SA	SR_SA_A_PH_LOCK	1	8	5	13	21	29	37	45	53	61	360	40	41		D	C000E	7
		SA	SR_SA_B_PH_LOCK	1	8	5	13	21	29	37	45	53	61	361	41	42		D	C000E	A
		SM	CR_SM_SDSM_A_ON	1	8	5	13	21	29	37	45	53	61	362	42	43		D	40005	C
		SM	CR_SM_SDSM_B_ON	1	8	5	13	21	29	37	45	53	61	363	43	44		D	40005	D
		SR	CR_SR_A_ON	1	8	5	13	21	29	37	45	53	61	364	44	45		D	40005	A
		SR	CR_SR_B_ON	1	8	5	13	21	29	37	45	53	61	365	45	46		D	40005	B
		SR	CR_SR_SISFB_RAD	1	8	5	13	21	29	37	45	53	61	366	46	47		DCE	C0001	3
18,23		SR	CR_SR_L_SHDN_ENA	1	8	5	13	21	29	37	45	53	61	367	47	48		DCE	C0001	4
		SR	IR_SR_10WLA_CURH	12	8	5	13	21	29	37	45	53	61	368	48	60		SW	na	na
		SR	IR_SR_10WLB_CURH	12	8	5	13	21	29	37	45	53	61	380	60	72		SW	na	na
		SR	IR_SR_1WLA_CURH	12	8	5	13	21	29	37	45	53	61	392	72	84		SW	na	na
		SR	IR_SR_1WLB_CURH	12	8	5	13	21	29	37	45	53	61	404	84	96		SW	na	na
38		SR	TA_SR_IR_SRC_A	12	8	5	13	21	29	37	45	53	61	416	96	108		A	C0003/C0004	55F3
38		SR	TA_SR_IR_SRC_B	12	8	5	13	21	29	37	45	53	61	428	108	120		A	C0003/C0004	4EF3
38	**447**	**XX**	**8 SEC FRAME FILL**	**8**	**8**	**5**	**13**	**21**	**29**	**37**	**45**	**53**	**61**	**440**	**120**	**128**	**8**			
1	320	XX	FRAME FILL	9	8	6	14	22	30	38	46	54	62	320	0	9		A	C0003/C0004	56F3
		SR	TP_SR_GRAT_ELEX	9	8	6	14	22	30	38	46	54	62	329	9	18		P	C0003/C0004	139B
		SR	TP_SR_GRAT_MOTOR	9	8	6	14	22	30	38	46	54	62	338	18	27		P	C0003/C0004	141B
		SR	TP_SR_LAMP_RING	9	8	6	14	22	30	38	46	54	62	347	27	36		P	C0003/C0004	119B
		SR	TP_SR_MIR2_DET	9	8	6	14	22	30	38	46	54	62	356	36	45		P	C0003/C0004	131B

TABLE 20-4. MODIS TELEMETRY FRAME DEFINITION

See Notes below for how 1553 bus telemetry frame was developed. True sample periods are 1.024 sec, 8.192 sec & 65.536 sec. *5/97*

pfm chg#	FB	1 Subsystem	2 Mnemonic Name	3 # of Bits	4 Sample Period	5 Major Cycle (0 - 63)	6 Major Cyc Start Bit	7 Group Start Bit	8 Cum Group Bits Used	9 Group 16bit Words	10 Tlmy Type	11 HW Addr Write/Read	12 HW Data Loc
		SR	VR_SR_LAMPS_H	12	8	6 14 22 30 38 46 54 62	365	45	57		SW	na	na
		SR	VR_SR_SRC_A_RADH	12	8	6 14 22 30 38 46 54 62	377	57	69		SW	na	na
		SR	VR_SR_SRC_B_RADH	12	8	6 14 22 30 38 46 54 62	389	69	81		SW	na	na
		TG	CR_TG_A_ON	1	8	6 14 22 30 38 46 54 62	401	81	82		D	C0010	C
		TG	CR_TG_A_RESET	1	8	6 14 22 30 38 46 54 62	402	82	83		D	C0010	D
		TG	CR_TG_B_ON	1	8	6 14 22 30 38 46 54 62	403	83	84		D	C0011	0
		TG	CR_TG_B_RESET	1	8	6 14 22 30 38 46 54 62	404	84	85		D	C0011	1
16		FR	CS_FR_ENC_DELTA	14	8	6 14 22 30 38 46 54 62	405	85	99		SW	na	na
20		SR	CS_SR_USE_L10WX1	4	8	6 14 22 30 38 46 54 62	419	99	103		SW	na	na
20		SR	CS_SR_USE_L10WX2	4	8	6 14 22 30 38 46 54 62	423	103	107		SW	na	na
20		SR	CS_SR_USE_L10WX3	4	8	6 14 22 30 38 46 54 62	427	107	111		SW	na	na
20		SR	CS_SR_USE_L1WX1	2	8	6 14 22 30 38 46 54 62	431	111	113		SW	na	na
20	**447**	**XX**	**8_SEC FRAME FILL**	**15**	**8**	**6 14 22 30 38 46 54 62**	**433**	**113**	**128**	**8**			
1,38	**320**	SR	TA_SR_SRC_A_SIPD	12	8	7 15 23 31 39 47 55 63	320	0	12		A	C0003/C0004	5673
1,38		SR	TA_SR_SRC_B_SIPD	12	8	7 15 23 31 39 47 55 63	332	12	24		A	C0003/C0004	56F3
1,38	**447**	**XX**	**8_SEC FRAME FILL**	**104**	**8**	**7 15 23 31 39 47 55 63**	**344**	**24**	**128**	**8**			
	448	AO	TP_AO_LWIR_LENS	12	65	0	448	0	12		P	C0003/C0004	315B
		AO	TP_AO_LWIR_OBJ	12	65	0	460	12	24		P	C0003/C0004	31DB
		AO	TP_AO_PX_NZ_CORN	12	65	0	472	24	36		P	C0003/C0004	335B
		AO	TP_AO_SMIR_LENS	12	65	0	484	36	48		P	C0003/C0004	325B
		AO	TP_AO_SMIR_OBJ	12	65	0	496	48	60		P	C0003/C0004	32DB
	511	**XX**	**65_SEC_FRAME FILL**	**4**	**65**	**0**	**508**	**60**	**64**	**4**			
	448	AO	TP_AO_VNDICH_HSG	12	65	1	448	0	12		P	C0003/C0004	30DB
		CE	TP_CE_CAL2	9	65	1	460	12	21		P	C0003/C0004	21BB
		CP	TP_CP_A_1553	9	65	1	469	21	30		P	C0003/C0004	20BB
		CP	TP_CP_B_1553	9	65	1	478	30	39		P	C0003/C0004	213B
		CP	VR_CP_N11V	8	65	1	487	39	47		A	C0003/C0004	8771
		CP	VR_CP_N5V	8	65	1	495	47	55		A	C0003/C0004	87F1
		CP	VR_CP_P11V	8	65	1	503	55	63		A	C0003/C0004	8671
	511	**XX**	**65_SEC_FRAME FILL**	**1**	**65**	**1**	**511**	**63**	**64**	**4**			
	448	CP	VR_CP_P5V	8	65	2	448	0	8		A	C0003/C0004	86F1
		DR	TP_DR_NAD	9	65	2	456	8	17		P	C0003/C0004	161B
		DR	TP_DR_SDD	9	65	2	465	17	26		P	C0003/C0004	179B
34		DR	TP_DR_SVD	9	65	2	474	26	35		P	C0003/C0004	38EB
		FR	TP_FR_A_ENGINE	9	65	2	483	35	44		P	C0003/C0004	1F2B
		FR	TP_FR_B_ENGINE	9	65	2	492	44	53		P	C0003/C0004	1FAB
		ME	TP_ME_CHAS_TOP	9	65	2	501	53	62		P	C0003/C0004	112B
	511	**XX**	**65_SEC_FRAME FILL**	**2**	**65**	**2**	**510**	**62**	**64**	**4**			
	448	MF	TP_MF_CALBKHD_SR	9	65	3	448	0	9		P	C0003/C0004	11AB
		MF	TP_MF_CVR_OP_SR	9	65	3	457	9	18		P	C0003/C0004	132B

TABLE 20-4. MODIS TELEMETRY FRAME DEFINITION

See Notes below for how 1553 bus telemetry frame was developed. True sample periods are 1.024 sec, 8.192 sec & 65.536 sec. *5/97*

pfm chg#	1	2	3	4	5	6	7	8	9	10	11	12
FB	Subsystem	Mnemonic Name	# of Bits	Sample Period	Major Cycle (0 - 63)	Major Cyc Start Bit	Group Start Bit	Cum Group Bits Used	Group 16bit Words	Tlmy Type	HW Addr Write/Read	HW Data Loc
	MF	TP_MF_NAD_APT_NX	9	65	3	466	18	27		P	C0003/C0004	1EAB
	MF	TP_MF_NAD_APT_NY	9	65	3	475	27	36		P	C0003/C0004	14AB
	MF	TP_MF_NX_AOBKHD	9	65	3	484	36	45		P	C0003/C0004	122B
	MF	TP_MF_PX_AOBKHD	9	65	3	493	45	54		P	C0003/C0004	12AB
	MF	TP_MF_SV_PORT	9	65	3	502	54	63		P	C0003/C0004	152B
511	**XX**	**65_SEC_FRAME FILL**	**1**	**65**	**3**	**511**	**63**	**64**	**4**			
448	MF	TP_MF_TOP_BY_KM2	9	65	4	448	0	9		P	C0003/C0004	142B
	MF	TP_MF_YZ_CALBKHD	9	65	4	457	9	18		P	C0003/C0004	1DAB
	MF	TP_MF_Z_BKHD_BB	9	65	4	466	18	27		P	C0003/C0004	1E2B
	PC	TA_PC_B31_MUX	9	65	4	475	27	36		APC	C0003/C0004	0070
	PC	TA_PC_B32_MUX	9	65	4	484	36	45		APC	C0003/C0004	00F0
	PC	TA_PC_B33_MUX	9	65	4	493	45	54		APC	C0003/C0004	0170
	PC	TA_PC_B34_MUX	9	65	4	502	54	63		APC	C0003/C0004	01F0
511	**XX**	**65_SEC_FRAME FILL**	**1**	**65**	**4**	**511**	**63**	**64**	**4**			
448	PC	TA_PC_B35_MUX	9	65	5	448	0	9		APC	C0003/C0004	0270
	PC	TA_PC_B36_MUX	9	65	5	457	9	18		APC	C0003/C0004	02F0
	PC	TP_PC_CLAM_MNT	9	65	5	466	18	27		P	C0003/C0004	109B
	PC	VR_PC_B31_GND	8	65	5	475	27	35		APC	C0003/C0004	0070
	PC	VR_PC_B31_RN12V	8	65	5	483	35	43		APC	C0003/C0004	0070
	PC	VR_PC_B31_RN5V	8	65	5	491	43	51		APC	C0003/C0004	0070
	PC	VR_PC_B31_RP12V	8	65	5	499	51	59		APC	C0003/C0004	0070
511	**XX**	**65_SEC_FRAME FILL**	**5**	**65**	**5**	**507**	**59**	**64**	**4**			
448	PC	VR_PC_B31_RP5V	8	65	6	448	0	8		APC	C0003/C0004	0070
	PC	VR_PC_B32_GND	8	65	6	456	8	16		APC	C0003/C0004	00F0
	PC	VR_PC_B32_RN12V	8	65	6	464	16	24		APC	C0003/C0004	00F0
	PC	VR_PC_B32_RN5V	8	65	6	472	24	32		APC	C0003/C0004	00F0
	PC	VR_PC_B32_RP12V	8	65	6	480	32	40		APC	C0003/C0004	00F0
	PC	VR_PC_B32_RP5V	8	65	6	488	40	48		APC	C0003/C0004	00F0
	PC	VR_PC_B33_GND	8	65	6	496	48	56		APC	C0003/C0004	0170
511	**PC**	**VR_PC_B33_RN12V**	**8**	65	6	504	56	**64**	**4**	APC	C0003/C0004	0170
448	PC	VR_PC_B33_RN5V	8	65	7	448	0	8		APC	C0003/C0004	0170
	PC	VR_PC_B33_RP12V	8	65	7	456	8	16		APC	C0003/C0004	0170
	PC	VR_PC_B33_RP5V	8	65	7	464	16	24		APC	C0003/C0004	0170
	PC	VR_PC_B34_GND	8	65	7	472	24	32		APC	C0003/C0004	01F0
	PC	VR_PC_B34_RN12V	8	65	7	480	32	40		APC	C0003/C0004	01F0
	PC	VR_PC_B34_RN5V	8	65	7	488	40	48		APC	C0003/C0004	01F0
	PC	VR_PC_B34_RP12V	8	65	7	496	48	56		APC	C0003/C0004	01F0
511	**XX**	**65_SEC_FRAME FILL**	**8**	**65**	**7**	**504**	**56**	**64**	**4**			
448	PC	VR_PC_B34_RP5V	8	65	8	448	0	8		APC	C0003/C0004	01F0
	PC	VR_PC_B35_GND	8	65	8	456	8	16		APC	C0003/C0004	0270

TABLE 20-4. MODIS TELEMETRY FRAME DEFINITION

See Notes below for how 1553 bus telemetry frame was developed. True sample periods are 1.024 sec, 8.192 sec & 65.536 sec. *5/97*

pfm chg#	FB	1 Subsystem	2 Mnemonic Name	3 # of Bits	4 Sample Period	5 Major Cycle (0 - 63)	6 Major Cyc Start Bit	7 Group Start Bit	8 Cum Group Bits Used	9 Group 16bit Words	10 Tlmy Type	11 HW Addr Write/Read	12 HW Data Loc
		PC	VR_PC_B35_RN12V	8	65	8	464	16	24		APC	C0003/C0004	0270
		PC	VR_PC_B35_RN5V	8	65	8	472	24	32		APC	C0003/C0004	0270
		PC	VR_PC_B35_RP12V	8	65	8	480	32	40		APC	C0003/C0004	0270
		PC	VR_PC_B35_RP5V	8	65	8	488	40	48		APC	C0003/C0004	0270
		PC	VR_PC_B36_GND	8	65	8	496	48	56		APC	C0003/C0004	02F0
	511	**XX**	**65_SEC_FRAME FILL**	**8**	**65**	**8**	**504**	**56**	**64**	**4**			
	448	PC	VR_PC_B36_RN12V	8	65	9	448	0	8		APC	C0003/C0004	02F0
		PC	VR_PC_B36_RN5V	8	65	9	456	8	16		APC	C0003/C0004	02F0
		PC	VR_PC_B36_RP12V	8	65	9	464	16	24		APC	C0003/C0004	02F0
		PC	VR_PC_B36_RP5V	8	65	9	472	24	32		APC	C0003/C0004	02F0
		PS	TP_PS1_CVTR_SW	9	65	9	480	32	41		P	C0003/C0004	22BB
		PS	TP_PS1_DIODE_OUT	9	65	9	489	41	50		P	C0003/C0004	233B
		PS	TP_PS1_DWNREG_SW	9	65	9	498	50	59		P	C0003/C0004	223B
	511	**XX**	**65_SEC_FRAME FILL**	**5**	**65**	**9**	**507**	**59**	**64**	**4**			
	448	PS	TP_PS1_PRELOAD	9	65	10	448	0	9		P	C0003/C0004	23BB
		PS	TP_PS2_CVTR_SW	9	65	10	457	9	18		P	C0003/C0004	263B
		PS	TP_PS2_DIODE_OUT	9	65	10	466	18	27		P	C0003/C0004	26BB
		PS	TP_PS2_DWNREG_SW	9	65	10	475	27	36		P	C0003/C0004	25BB
		PS	TP_PS2_PRELOAD	9	65	10	484	36	45		P	C0003/C0004	273B
		PS	VR_PS1_N15V_A1ME	8	65	10	493	45	53		A	C0003/C0004	5978
		PS	VR_PS1_N15V_A2AF	8	65	10	501	53	61		A	C0003/C0004	5A79
11,27	**511**	**CP**	**CS_CP_MODIS_MOD**	**3**	**65**	**10**	**509**	**61**	**64**	**4**	SW	na	na
	448	PS	VR_PS1_N15V_A3AS	8	65	11	448	0	8		A	C0003/C0004	5B7A
		PS	VR_PS1_N30V_A1ME	8	65	11	456	8	16		A	C0003/C0004	5C78
		PS	VR_PS1_N8V_A2	8	65	11	464	16	24		A	C0003/C0004	5D79
		PS	VR_PS1_P15V_A1ME	8	65	11	472	24	32		A	C0003/C0004	59F8
		PS	VR_PS1_P15V_A2AF	8	65	11	480	32	40		A	C0003/C0004	5AF9
		PS	VR_PS1_P15V_A3AS	8	65	11	488	40	48		A	C0003/C0004	5BFA
		PS	VR_PS1_P30V_A1	8	65	11	496	48	56		A	C0003/C0004	5CF8
37	**511**	**PS**	**VR_PS1_P5_6V_D1**	**8**	**65**	**11**	**504**	**56**	**64**	**4**	A	C0003/C0004	587B
	448	PS	VR_PS1_P88V_A1ME	8	65	12	448	0	8		A	C0003/C0004	5D78
		PS	VR_PS1_P8V_A2	8	65	12	456	8	16		A	C0003/C0004	5DF9
		PS	VR_PS1_P8V_N1ME	8	65	12	464	16	24		A	C0003/C0004	5878
		PS	VR_PS2_N15V_A1ME	8	65	12	472	24	32		A	C0003/C0004	717C
		PS	VR_PS2_N15V_A2AF	8	65	12	480	32	40		A	C0003/C0004	727D
		PS	VR_PS2_N15V_A3AS	8	65	12	488	40	48		A	C0003/C0004	737E
		PS	VR_PS2_N30V_A1ME	8	65	12	496	48	56		A	C0003/C0004	747C
	511	**PS**	**VR_PS2_N8V_A2**	**8**	**65**	**12**	**504**	**56**	**64**	**4**	A	C0003/C0004	757D
	448	PS	VR_PS2_P15V_A1ME	8	65	13	448	0	8		A	C0003/C0004	71FC
		PS	VR_PS2_P15V_A2AF	8	65	13	456	8	16		A	C0003/C0004	72FD

TABLE 20-4. MODIS TELEMETRY FRAME DEFINITION

See Notes below for how 1553 bus telemetry frame was developed. True sample periods are 1.024 sec, 8.192 sec & 65.536 sec.

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pim chg#	FB	1 Subsystem	2 Mnemonic Name	3 # of Bits	4 Sample Period	5 Major Cycle (0 - 63)	6 Major Cyc Start Bit	7 Group Start Bit	8 Cum Group Bits Used	9 Group 16bit Words	10 Tlmy Type	11 HW Addr Write/Read	12 HW Data Loc
		PS	VR_PS2_P15V_A3AS	8	65	13	464	16	24		A	C0003/C0004	73FE
		PS	VR_PS2_P30V_A1	8	65	13	472	24	32		A	C0003/C0004	74FC
37		PS	VR_PS2_P5_6V_D1	8	65	13	480	32	40		A	C0003/C0004	707F
		PS	VR_PS2_P88V_A1ME	8	65	13	488	40	48		A	C0003/C0004	757C
		PS	VR_PS2_P8V_A2	8	65	13	496	48	56		A	C0003/C0004	75FD
	511	**PS**	**VR_PS2_P8V_N1ME**	**8**	**65**	**13**	**504**	**56**	**64**	**4**	A	C0003/C0004	70FC
	448	PV	TA_PVLW_PWB4_10	9	65	14	448	0	9		APV	C0003/C0004	0371
		PV	TA_PVNIR_PWB2_8	9	65	14	457	9	18		APV	C0003/C0004	0371
		PV	TA_PVNIR_PWB3_9	9	65	14	466	18	27		APV	C0003/C0004	0371
		PV	TA_PVSM_PWB5_11	9	65	14	475	27	36		APV	C0003/C0004	0371
		PV	TA_PVSM_PWB6_12	9	65	14	484	36	45		APV	C0003/C0004	0371
		PV	TA_PVVIS_PWB1_7	9	65	14	493	45	54		APV	C0003/C0004	0371
		PV	VR_PVLW_P30V	8	65	14	502	54	62		APV	C0003/C0004	0371
	511	**XX**	**65_SEC_FRAME FILL**	**2**	**65**	**14**	**510**	**62**	**64**	**4**			
	448	PV	VR_PVLW_RN11V	8	65	15	448	0	8		APV	C0003/C0004	0371
		PV	VR_PVLW_RN5V	8	65	15	456	8	16		APV	C0003/C0004	0371
		PV	VR_PVLW_RP11V	8	65	15	464	16	24		APV	C0003/C0004	0371
		PV	VR_PVLW_RP5V	8	65	15	472	24	32		APV	C0003/C0004	0371
		PV	VR_PVNIR_P30V	8	65	15	480	32	40		APV	C0003/C0004	0371
		PV	VR_PVNIR_P5VD3_9	8	65	15	488	40	48		APV	C0003/C0004	0371
		PV	VR_PVNIR_RN11V28	8	65	15	496	48	56		APV	C0003/C0004	0371
	511	**PV**	**VR_PVNIR_RN11V39**	**8**	**65**	**15**	**504**	**56**	**64**	**4**	APV	C0003/C0004	0371
	448	PV	VR_PVNIR_RN5V2_8	8	65	16	448	0	8		APV	C0003/C0004	0371
		PV	VR_PVNIR_RN5V3_9	8	65	16	456	8	16		APV	C0003/C0004	0371
		PV	VR_PVNIR_RP11V28	8	65	16	464	16	24		APV	C0003/C0004	0371
		PV	VR_PVNIR_RP11V39	8	65	16	472	24	32		APV	C0003/C0004	0371
		PV	VR_PVNIR_RP5V2_8	8	65	16	480	32	40		APV	C0003/C0004	0371
		PV	VR_PVNIR_RP5V3_9	8	65	16	488	40	48		APV	C0003/C0004	0371
		PV	VR_PVSM_P30V	8	65	16	496	48	56		APV	C0003/C0004	0371
	511	**PV**	**VR_PVSM_P5VD6_12**	**8**	**65**	**16**	**504**	**56**	**64**	**4**	APV	C0003/C0004	0371
	448	PV	VR_PVSM_RN11V511	8	65	17	448	0	8		APV	C0003/C0004	0371
		PV	VR_PVSM_RN11V612	8	65	17	456	8	16		APV	C0003/C0004	0371
		PV	VR_PVSM_RN5V5_11	8	65	17	464	16	24		APV	C0003/C0004	0371
		PV	VR_PVSM_RN5V6_12	8	65	17	472	24	32		APV	C0003/C0004	0371
		PV	VR_PVSM_RP11V511	8	65	17	480	32	40		APV	C0003/C0004	0371
		PV	VR_PVSM_RP11V612	8	65	17	488	40	48		APV	C0003/C0004	0371
		PV	VR_PVSM_RP5V5_11	8	65	17	496	48	56		APV	C0003/C0004	0371
	511	**PV**	**VR_PVSM_RP5V6_12**	**8**	**65**	**17**	**504**	**56**	**64**	**4**	APV	C0003/C0004	0371
	448	PV	VR_PVVIS_P30V	8	65	18	448	0	8		APV	C0003/C0004	0371
		PV	VR_PVVIS_RN11V	8	65	18	456	8	16		APV	C0003/C0004	0371

TABLE 20-4. MODIS TELEMETRY FRAME DEFINITION

See Notes below for how 1553 bus telemetry frame was developed. True sample periods are 1.024 sec, 8.192 sec & 65.536 sec.

5/97

pfm chg#	FB	1 Subsystem	2 Mnemonic Name	3 # of Bits	4 Sample Period	5 Major Cycle (0 - 63)	6 Major Cyc Start Bit	7 Group Start Bit	8 Cum Group Bits Used	9 Group 16bit Words	10 Tlmy Type	11 HW Addr Write/Read	12 HW Data Loc
		PV	VR_PVVIS_RN5V	8	65	18	464	16	24		APV	C0003/C0004	0371
		PV	VR_PVVIS_RP11V	8	65	18	472	24	32		APV	C0003/C0004	0371
		PV	VR_PVVIS_RP5V	8	65	18	480	32	40		APV	C0003/C0004	0371
		RC	TA_RC_CS	12	65	18	488	40	52		A	C0003/C0004	64F5
	511	**RC**	**TA_RC_CS_OG**	**12**	**65**	**18**	**500**	**52**	**64**	**4**	A	C0003/C0004	5BF5
	448	RC	TA_RC_IS	12	65	19	448	0	12		A	C0003/C0004	6575
		RC	TA_RC_IS_OG	12	65	19	460	12	24		A	C0003/C0004	5CF5
		RC	TA_RC_OS_OG	12	65	19	472	24	36		A	C0003/C0004	63F5
		RC	TP_RC_MNT_RING	12	65	19	484	36	48		P	C0003/C0004	33DB
17		RC	TP_RC_SPARE	12	65	19	496	48	60		P	C0003/C0004	396B
	511	**XX**	**65_SEC_FRAME FILL**	**4**	**65**	**19**	**508**	**60**	**64**	**4**			
7	**448**	RC	TP_RC_SPARE	12	65	20	448	0	12		P	C0003/C0004	39EB
39		SA	SA_SPARE	8	65	20	460	12	20		A	C0003/C0004	50F0
39		SA	SA_SPARE	8	65	20	468	20	28		A	C0003/C0004	5371
		SA	TP_SA_A_MTR	9	65	20	476	28	37		P	C0003/C0004	345B
6,25		SA	SS_SA_SPARE	9	65	20	485	37	46		SW	na	na
28,35		SA	TP_SA_SPARE	12	65	20	494	46	58		P	C0003/C0004	35DB
	511	**XX**	**65_SEC_FRAME FILL**	**6**	**65**	**20**	**506**	**58**	**64**	**4**			
	448	SA	TP_SA_RCT1_MIR	12	65	21	448	0	12		P	C0003/C0004	365B
28,35		SA	TP_SA_SPARE	12	65	21	460	12	24		P	C0003/C0004	36DB
		SA	TP_SA_RCT2_MIR	12	65	21	472	24	36		P	C0003/C0004	375B
39		SA	SA_SPARE	8	65	21	484	36	44		A	C0003/C0004	5270
14		SA	VR_SA_A_MTR_TORQ	10	65	21	492	44	54		A	C0003/C0004	507B
14		SA	VR_SA_A_RN11V	8	65	21	502	54	62		A	C0003/C0004	51F0
14	**511**	**XX**	**65_SEC_FRAME FILL**	**2**	**65**	**21**	**510**	**62**	**64**	**4**			
	448	SA	VR_SA_A_RP11V	8	65	22	448	0	8		A	C0003/C0004	5170
39		SA	SA_SPARE	8	65	22	456	8	16		A	C0003/C0004	54F1
14		SA	VR_SA_B_MTR_TORQ	10	65	22	464	16	26		A	C0003/C0004	52F1
14		SA	VR_SA_B_RN11V	8	65	22	474	26	34		A	C0003/C0004	5470
14		SA	VR_SA_B_RP11V	8	65	22	482	34	42		A	C0003/C0004	53F1
17		SD	TP_SD_SPARE	9	65	22	490	42	51		P	C0003/C0004	111B
12,14		SM	TP_SM_DET_AMP3	9	65	22	499	51	60		P	C0003/C0004	151B
14	**511**	**XX**	**65_SEC_FRAME FILL**	**4**	**65**	**22**	**508**	**60**	**64**	**4**			
	448	SR	TP_SR_MONO_CHAS1	9	65	23	448	0	9		P	C0003/C0004	149B
		SR	TP_SR_MONO_CHAS2	9	65	23	457	9	18		P	C0003/C0004	129B
		SR	TP_SR_SNOUT	9	65	23	466	18	27		P	C0003/C0004	121B
38		SS	TP_SS_SPARE	9	65	23	475	27	36		P	C0003/C0004	2A4B
		TC	VR_TC_CSCKT_PV	8	65	23	484	36	44		A	C0003/C0004	5C75
		TC	VR_TC_ISCKT_PV	8	65	23	492	44	52		A	C0003/C0004	5D75
		TC	VR_TC_LWCKT_NV	8	65	23	500	52	60		A	C0003/C0004	6275

TABLE 20-4. MODIS TELEMETRY FRAME DEFINITION

See Notes below for how 1553 bus telemetry frame was developed. True sample periods are 1.024 sec, 8.192 sec & 65.536 sec.

5/97

pfm chg#	FB	1 Subsystem	2 Mnemonic Name	3 # of Bits	4 Sample Period	5 Major Cycle (0 - 63)	6 Major Cyc Start Bit	7 Group Start Bit	8 Cum Group Bits Used	9 Group 16bit Words	10 Tlmy Type	11 HW Addr Write/Read	12 HW Data Loc
	511	**XX**	**65_SEC_FRAME FILL**	**4**	**65**	**23**	**508**	**60**	**64**	**4**			
	448	TC	VR_TC_LWCKT_PV	8	65	24	448	0	8		A	C0003/C0004	61F5
15,29		TC	SS_TC_SPARE	8	65	24	456	8	16		SW	na	na
		TC	VR_TC_OSCKT_PV	8	65	24	464	16	24		A	C0003/C0004	6475
		TC	VR_TC_SMCKT_NV	8	65	24	472	24	32		A	C0003/C0004	6175
		TC	VR_TC_SMCKT_PV	8	65	24	480	32	40		A	C0003/C0004	60F5
15,29		TC	SS_TC_SPARE	8	65	24	488	40	48		SW	na	na
		TC	VR_TC_VISCKT_NV	8	65	24	496	48	56		A	C0003/C0004	6375
	511	**TC**	**VR_TC_VISCKT_PV**	**8**	**65**	**24**	**504**	**56**	**64**	**4**	A	C0003/C0004	62F5
	448	TE	TP_TE_FOLD_MIR	9	65	25	448	0	9		P	C0003/C0004	2ACB
		TE	TP_TE_PRI_MIR	9	65	25	457	9	18		P	C0003/C0004	2B4B
		TE	TP_TE_SEC_MIR	9	65	25	466	18	27		P	C0003/C0004	2BCB
		TM	TP_TM_ANLG_CKT	9	65	25	475	27	36		P	C0003/C0004	27BB
		TM	VR_TM_REF_ACT1_1	12	65	25	484	36	48		A	C0003/C0004	85F0
		TM	VR_TM_REF_ACT1_2	12	65	25	496	48	60		A	C0003/C0004	8570
	511	**XX**	**65_SEC_FRAME FILL**	**4**	**65**	**25**	**508**	**60**	**64**	**4**			
	448	TM	VR_TM_REF_ACT1_3	12	65	26	448	0	12		A	C0003/C0004	84F0
		TM	VR_TM_REF_ACT2_1	12	65	26	460	12	24		A	C0003/C0004	8FF0
		TM	VR_TM_REF_ACT2_2	12	65	26	472	24	36		A	C0003/C0004	8F70
21		TM	VR_TM_REF_ACT3_1	12	65	26	484	36	48		A	C0003/C0004	97F0
21		TM	VR_TM_REF_ACT4_1	12	65	26	496	48	60		A	C0003/C0004	9FF0
	511	**XX**	**65_SEC_FRAME FILL**	**4**	**65**	**26**	**508**	**60**	**64**	**4**			
	448	TM	VR_TM_REF_ACT5_1	12	65	27	448	0	12		A	C0003/C0004	A7F0
		TM	VR_TM_REF_ACT5_2	12	65	27	460	12	24		A	C0003/C0004	A770
		TM	VR_TM_REF_ACT5_3	12	65	27	472	24	36		A	C0003/C0004	A6F0
		TM	VR_TM_REF_ACT6_1	12	65	27	484	36	48		A	C0003/C0004	AFF0
5		TM	VR_TM_REF_ACT6_3	12	65	27	496	48	60		A	C0003/C0004	AF70
	511	**XX**	**65_SEC_FRAME FILL**	**4**	**65**	**27**	**508**	**60**	**64**	**4**			
21	**448**	TM	VR_TM_REF_ACT7_1	12	65	28	448	0	12		A	C0003/C0004	B7F0
		TM	VR_TM_REF_BB_1	12	65	28	460	12	24		P	C0003/C0004	068B
		TM	VR_TM_REF_BB_2	12	65	28	472	24	36		P	C0003/C0004	070B
		TM	VR_TM_REF_BB_3	12	65	28	484	36	48		P	C0003/C0004	078B
10		TM	VR_TM_REF_PRT1	12	65	28	496	48	60		P	C0003/C0004	386B
	511	**XX**	**65_SEC_FRAME FILL**	**4**	**65**	**28**	**508**	**60**	**64**	**4**			
	448	TM	VR_TM_REF_PSV1	12	65	29	448	0	12		P	C0003/C0004	101B
		TM	VR_TM_REF_PSV2	12	65	29	460	12	24		P	C0003/C0004	182B
		TM	VR_TM_REF_PSV3	12	65	29	472	24	36		P	C0003/C0004	203B
		TM	VR_TM_REF_PSV4	12	65	29	484	36	48		P	C0003/C0004	286B
		TM	VR_TM_REF_PSV5	12	65	29	496	48	60		P	C0003/C0004	305B
	511	**XX**	**65_SEC_FRAME FILL**	**4**	**65**	**29**	**508**	**60**	**64**	**4**			

TABLE 20-4. MODIS TELEMETRY FRAME DEFINITION

See Notes below for how 1553 bus telemetry frame was developed. True sample periods are 1.024 sec, 8.192 sec & 65.536 sec. *5/97*

pfm chg#	1 FB	1 Subsystem	2 Mnemonic Name	3 # of Bits	4 Sample Period	5 Major Cycle (0 - 63)	6 Major Cyc Start Bit	7 Group Start Bit	8 Cum Group Bits Used	9 Group 16bit Words	10 Tlmy Type	11 HW Addr Write/Read	12 HW Data Loc
10	448	TM	VR_TM_REF_ACTGND	12	65	30	448	0	12		P	C0003/C0004	B870
4		AO	TA_AO_VIS_FPA	12	65	30	460	12	24		A	C0003/C0004	57F5
4		AO	TA_AO_NIR_FPA	12	65	30	472	24	36		A	C0003/C0004	5F75
8,15		RC	VR_RC_LW_FPA_HTR	10	65	30	484	36	46		A	C0003/C0004	6075
8,15		RC	VR_RC_SM_FPA_HTR	10	65	30	494	46	56		A	C0003/C0004	65F5
	511	**XX**	**65_SEC_FRAME FILL**	**8**	**65**	**30**	**504**	**56**	**64**	**4**			
10	448	TM	VR_TM_REF_PRT2	12	65	31	448	0	12		P	C0003/C0004	3CEB
10		TM	VR_TM_REF_PSV6	12	65	31	460	12	24		P	C0003/C0004	24BB
10		TM	VR_TM_REF_PSV7	12	65	31	472	24	36		P	C0003/C0004	2CCB
10		TM	VR_TM_REF_PSV8	12	65	31	484	36	48		P	C0003/C0004	34DB
	511	**XX**	**65_SEC_FRAME FILL**	**16**	**65**	**31**	**496**	**48**	**64**	**4**			
39	448	SA	IR_SA_A_ECDR_LED	12	65	32	448	0	12		A	C0003/C0004	50F0
39		SA	IR_SA_B_ECDR_LED	12	65	32	460	12	24		A	C0003/C0004	5371
39		SA	VR_SA_A_ECDR_MON	12	65	32	472	24	36		A	C0003/C0004	5270
39		SA	VR_SA_B_ECDR_MON	12	65	32	484	36	48		A	C0003/C0004	54F1
39	**511**	**XX**	**65_SEC_FRAME FILL**	**16**	**65**	**32**	**496**	**48**	**64**	**4**			
21	**448**	**XX**	**65_SEC_FRAME FILL**	**64**	**65**	**33 thru 63 31 Maj Cyc Spare**	**448**	**0**	**64**	**4**			
	466	*<--Total HK items including 29 Spares, but w/o frame fill items. Also, excludes pt-pt S/C 18DS & 9PS tlmy items.*											

NOTES:

Per the EOS-AM 1553 bus activity schedule, the MODIS HK telemetry is transferred during Minor Cycle 72 (see Figure 16). The frame structure has been established by the following guidelines:

1. Sort by Sample Period, then move CP to front of 1 sec samples only, then sort by Subsys and then Name.

2. Partition groups by 16-bit words: 20 words to 1 sec samples, 8 words to 8 sec samples & 4 words to 65 sec samples.

3. Frame fill bits are used to complete 16-bit boundaries, but none are specifically assigned to internal spares from the bottom of Table 20-2A.

Major Cycle 512 Bit Boundaries

MAJ CYC 0			MAJ CYC 63
0		1 sec samples	0
	20W	20W x 16b/W = 320 bits	
319		repeats every major cycle	319
320		8 sec samples	320
	8W	8W x 16b/W = 128 bits	
447		repeats every 8 major cycles	447
448		65 sec samples	448
	4W	4W x 16b/W = 64 bits	
511		unique each major cycle	511

T20-4 PF Change History Notes. Chg #s relate to Chg #s by table except for [#s], which are general.

1. 8/7/95 Deleted extra space in TA_SR_SRC_A_SIPD & TA_SR_SRC_B_SIPD to meet 16 charcter name count.
2. 8/7/95 Chg SS_CP_MODE_CHG_GO to SS_CP_MODECHG_GO to match 16 ch in T20-2.
3. 8/7/95 Chg CR_PVNIR_S_DELAYH to CR_PVNIR_S_DELYH and CR_PVVIS_S_DELAYH to CR_PVVIS_S_DELYH to match 16 ch in T20-2.
4. 8/13/95 Chg NIR/VIS FPA subsys from WF to AO; TA_WF_VIS_FPA & TA_WF_NIR_FPA to TA_AO_VIS_FPA & TA_AO_NIR_FPA.
5. 8/13/95 Chg VR_TM_REF_ACT6_2 to VR_TM_REF_ACT6_3 because of particular internal Ref 3 used.
6. 10/5/95 Chg TP_SA_B_MTR to TP_SA_SPARE. (9-bit cnt was not enough to use as VR_TM_REF_PSV8)
7. 10/7/95 Chg TP_RC_OS_WH to TP_RC_SPARE. Maj Cyc 20.
8. 10/8/95 Chg subsys relation of VR_TC_LW_FPA_HTR to VR_RC_LW_FPA_HTR and VR_TC_SM_FPA_HTR to VR_RC_SM_FPA_HTR.

TABLE 20-4. MODIS TELEMETRY FRAME DEFINITION

See Notes below for how 1553 bus telemetry frame was developed. True sample periods are 1.024 sec, 8.192 sec & 65.536 sec. *5/97*

pfm chg#	1 FB	2 Subsystem	2 Mnemonic Name	3 # of Bits	4 Sample Period	5 Major Cycle (0 - 63)	6 Major Cyc Start Bit	7 Group Start Bit	8 Cum Group Bits Used	9 Group 16bit Words	10 Tlmy Type	11 HW Addr Write/Read	12 HW Data Loc

9. 11/4/95 Chg CR_FO_BLK1,2,3,4_RESET's to CR_FO_SPARE's.
10. 11/5/95 Add new VR_TM_REFs: 1) Chg VR_TM_REF_GND to VR_TM_REF_ACTGND, 2) Chg VR_TM_REF_PRT to VR_TM_REF_PRT1, add 3) VR_TM_REF_PRT2, 4) VR_TM_REF_PSV6, 5) VR_TM_REF_PSV7 & 6)VR_TM_REF_PSV8.
11. 11/5/95 Add new 3bit tlmy CS_CP_MODIS_XX in place of 65 sec Maj Cyc 10 Fill.
12. 11/24/95 TP_SM_SDSM_GEDET to TP_SM_DET_AMP3.
13. 11/27/95 Chg names on TP_DR_MTRs 1) to TP_DR_NAD_FS from TP_DR_NAD_MTR, 2) to TP_DR_SVD_FS from TP_DR_SVD_MTR, 3) to TP_DR_SPARE from TP_DR_SDD_MTR.
14. 12/3/95 Increased the # of bits on Frame 21 VR_SA_A_MTR_TORQ and Frame 22 VR_SA_B_MTR_TORQ from 8 bits to 10 bits. Ripples frame location of every pt below them to the FILL BITS, which are each decreased by 2 bits.
15. 12/3/95 Chg frame location & increase # of bits on VR_RC_LW_FPA_HTR to Frame 30 from Frame 24, to 10 bits from 8 bits. Same for VR_RC_SM_FPA_HTR. Also, chg prior Frame 24 locations to 8-bit VR_RC_SPARE(2pl). Note Frame 24 FILL BITS remain the same, but Frame 30 FILL BITS decrease.
16. 2/29/96 Add new 14-bit CS_FR_ENC_DELTA to end of 8-sec sample group at maj cyc 6. Fill bits reduces from 43 to 29.
17. 2/29/96 Chg TP_SD_TEMP to TP_SD_SPARE & TP_RC_OS_FIN to TP_RC_SPARE.
18. 2/2/96 Minor name chg from CR_SR_SISOV_ENA to CR_SR_SISLOV_ENA.
19. 3/25/96 Collective chg for tlmy chged to Spares. 1) CR_DR_SDS_CLSD to CR_DR_Spare, 2) CR_SR_SIS_OFF to 1-sec CR_SR_SPARE.
20. 3/25/96 Collective new added tlmy: 1) CS_SR_LAMPS to 1-sec, 2) CS_SR_USE_L10WX1 to 8-sec, 3) CS_SR_USE_L10WX2 to 8-sec, 4) CS_SR_USE_L10WX3 to 8-sec, 5) CS_SR_USE_L1WX1 to 8-sec, readjust Frame Fill, 6) SS_CP_LAST_EVENT to 1-sec, 7) SS_FR_LAST_EVENT to 1-sec, 8) add 1-sec CS_FR_OFFSETTAB & reduce FRAME FILL, [4/6/96 see Chg#24 update 9) CS_FR_PCDCRDBG 8-sec, 10) CS_FR_PCDCRPOST 8-sec, 11) CS_FR_PCDCRPRE 8-sec] & reduce FRAME FILL.
21. 3/25/96 Revised tlmy: 1) chg CS_FR_SPARE 1-bit, 8-sec to CR_SR_LAMPS_LOW, 2) chg SS_CP_STATUS_02 to SS_CP_SCAN_EST 8-sec, 3) chg SS_CP_STATUS_10 to SS_CP_UART_RESET 8-sec, 4) chg SS_CP_STATUS_11 to SS_CP_UART_HUNT 8-sec, 5) chg SS_CP_STATUS_12 to SS_CP_UART_SYNC 8-sec, 6) chg SS_CP_STATUS_13 to SS_CP_UART_NORM, 7) moved 4 time code words 65-sec samples to 1-sec samples and turned 65-sec slots into Frame Fill bits, 8) chg 1-sec CS_SR_SPARE to CS_FR_BBRADTAB, 9) chg 1-sec CS_CP_SPARE to CS_FR_GAINTAB, 10) minor name chg from 8-sec SS_FR_PKT_TEST to SS_FR_SCI_PKT, 11) minor name chg addon to 3 VR_TM_REF_ACTX_1 words, [4/2/96 reinstate12) chg TP_SA_RCT1_HSG to TP_SA_SPARE 65-SEC, 13) chg TP_SA_RCT2_HSG to TP_SA_SPARE 65-sec], 14) chg CR_FO_SPARE to CS_FR_SCI_NORMAL 8-sec, [4/6/96, see update inChg#24, 15) Repartition 16-bit SS_CP_STATUS_04 into 2 4-bit words SS_CP_LOG_STATE & SS_FR_LOG_STATE].
22. 3/28/96 Chg 6 CP/FR to SS_CP_SPARE or SS_FR_SPARE: SS_CP_MEMPRO_ERR, SS_FR_MEMPRO_ERR, SS_CP_PARITY_ERR, SS_FR_PARITY_ERR, SS_CP_TEST_RES & SS_FR_TEST_RES. All 1-bit, 8 sec.
23. 4/3/96 Chg 8-sec name CR_SR_SISLOV_ENA to CR_SR_L_SHDN_ENA to match T20-2A.
24. 4/6/96 Reshuffle some recent reframing in Chg 20 & 21 into SS_CP_STATUS_03 slots & reactivate SS_CP_STATUS_04. Framefill from Chg#21 still good. Reshuffle 1) SS_CP_LOG_STATE, 2) SS_FR_LOG_STATE, 3) CS_FR_PCDCRDBG, 4) CS_FR_PCDCRPOST, 5) CS_FR_PCDCRPRE, & 6) SS_CP_STATUS_04 in place of SS_CP_STATUS_03.
25. 4/6/96 Chg 3 names to a SS_XX_SPARE (SW) & clean up Col 10,11,12 for items still carried as a spare frame location that used to have HW addresses when they were active (MajCyc 20, start bit485; MajCyc24, Start bit456 & MajCyc24, Start bit 488).

TABLE 20-4. MODIS TELEMETRY FRAME DEFINITION

See Notes below for how 1553 bus telemetry frame was developed. True sample periods are 1.024 sec, 8.192 sec & 65.536 sec. *5/97*

pfm chg#	FB	1 Subsystem	2 Mnemonic Name	3 # of Bits	4 Sample Period	5 Major Cycle (0 - 63)	6 Major Cyc Start Bit	7 Group Start Bit	8 Cum Group Bits Used	9 Group 16bit Words	10 Tlmy Type	11 HW Addr Write/Read	12 HW Data Loc

26. 4/6/96 4/6/96 Chg FR26 name to SS_FR_PKT_TYPE from SS_FR_SCI_PKT to be compatible with other new cmds/tlmy.
27. 4/8/96 Minor name chg to CS_CP_MODIS_MOD from CS_CP_MODIS_XX. Same chg in T20-2A.
28. 4/24/96 Revise Chg Note#21 to again chg 2 pts back to spares: TP_SA_SPARE was TP_SA_RCT1_HSG & TP_SA_SPARE was TP_SA_RCT2_HSG.
29. 5/3/96 slight name revision to Chg#25, the Spare's subsys relation s/b TC, not RC, to SS_TC_SPARE.

----------Changes since 151840 initial 5/96 release----------

30. 8/7/96 Chg name of 6 8-sec Maj Cyc 4 PC items. Typically,CR_PCB31_S_DELAY & CR_PCB32_S_DELAY became CS_PC_3132_SRISE and CS_PC_3132_SFALL band-pair sets.
31. 8/12/96 Correct Col 11 interchanged HW Address locations on CR_PVVISB_ECALON & CR_PVVIS_B_ON.
32. 8/15/96 Add two new words to 1-sec samples SS_CP_MACRO_ID and SS_CP_MACRO_ON.
33. 8/15/96 Chg 8-sec items to spares. Was CS_CP_PK_PWR, CS_FR_PCDCRDBG, CS_FR_PCDCRPOST, & CS_FR_PCDCRPRE.
34. 8/18/96 In 2nd 65-sec samples, correct Col 12 HW Data Loc of TP_DR_SVD to 38EB from 30EB to match T20-2A.
35. 8/19/96 In 20th 65-sec samples, chg 2 pts to spares: TP_SA_SPARE was TP_SA_RCT1_HSG & TP_SA_SPARE was TP_SA_RCT2_HSG.
36. 10/17/96 Re-activate FR_SPARE 8-sec sample (maj cyc 1) to be SS_FR_SCIABNORM.
37. 10/21/96 Correct names for VR_PS1_P5.6V_D1 & VR_PS2_P5.6V_D1 to be VR_PS1_P5_6V_D1 & VR_PS2_P5_6V_D1 to be consistent with OASIS convention
38. 4/97 Multiple EO1122D Incorporations for Rev B. See EO1122D (released 970305) for details of bit increase for several words and name chg & spare chg.
39. 4/97 Direct Rev B chg to increase bits from 8 to 12 and relocate to Maj Cyc 32: 1) IR_SA_A_ECDR_LED, 2) IR_SA_B_ECDR_LED, 3) VR_SA_A_ECDR_MON and VR_SA_B_ECDR_MON.

TABLE 20-5. MODIS ACTIVE ANALOG TELEMETRY/ENGINEERING LIMITS & EQUATIONS

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• See bottom Notes. • Equations are 5th order polynomial form: EU = C0 + C1(DN) + C2(DN)^2 + C3(DN)^3 + C4(DN)^4 + C5(DN)^5.

pf chg#	1 Subsys	2 Telemetry Mnemonic Name	3 # of Bits	4 Approx Tlmy Range	5 Eng Units	6a Red Low	6b Yellow Low	6c Yellow High	6d Red High	7a Eq #	7b C0	7c C1	7d C2	7e C3	7f C4	7g C5	8 Type /Use	9 Use	10 Ref EU SF/Nom
											Telemetry DN to Eng Units Equation Coefficients								
3,13,20	AO	TA_AO_NIR_FPA	12	-43 to 85	°C	-25	-15	40	50	TA08p	-5.7755E+1	3.5526E-2	2.8295E-6	-1.2865E-9	1.5373E-13	0	A	H	Teq
3,13,20	AO	TA_AO_VIS_FPA	12	-43 to 85	°C	-25	-15	40	50	TA09p	-5.8957E+1	3.5611E-2	2.7192E-6	-1.2548E-9	1.4924E-13	0	A	H	Teq
2,26,38	BB	IR_BB_HTRA_CURH	8	0 to 1.5	A	-0.10	-0.05	1.30	1.40	IR01ap	-1.5660E+0	1.2319E-2	0	0	0	0	A	H	0.625A/V
2,26,39	BB	IR_BB_HTRA_CURR	8	0 to 1.5	A	-0.10	-0.05	1.30	1.40	IR01ap	-1.5660E+0	1.2319E-2	0	0	0	0	A	E	0.625A/V
2,26,38	BB	IR_BB_HTRB_CURH	8	0 to 1.5	A	-0.10	-0.05	1.30	1.40	IR01bp	-1.5133E+0	1.1933E-2	0	0	0	0	A	H	0.606A/V
2,26,39	BB	IR_BB_HTRB_CURR	8	0 to 1.5	A	-0.10	-0.05	1.30	1.40	IR01bp	-1.5133E+0	1.1933E-2	0	0	0	0	A	E	0.606A/V
12	CP	VR_CP_N11V	8	-13.6 to 0	V	-11.60	-11.30	-10.70	-10.40	VR01	-1.3587E+1	1.0615E-1	0	0	0	0	A	H	5.4347V/V;-11.0V
12	CP	VR_CP_N5V	8	-6.3 to 0	V	-5.90	-5.70	-5.20	-4.90	VR02	-6.2655E+0	4.8949E-2	0	0	0	0	A	H	2.5064V/V;-5.4V
12	CP	VR_CP_P11V	8	0 to 13.6	V	10.40	10.70	11.30	11.60	VR01	-1.3587E+1	1.0615E-1	0	0	0	0	A	H	5.4347V/V;11.0V
12,38	CP	VR_CP_P5V	8	0 to 6.3	V	4.90	5.10	5.70	5.90	VR02	-6.2655E+0	4.8949E-2	0	0	0	0	A	H	2.5064V/V;5.4V
21,36	PC	TA_PC_B31_MUX	9	-25 to 50	°C	-24	-10	45	48	TA01p	5.0125E+1	-7.8916E-1	5.4339E-3	-2.0630E-5	3.7567E-8	-2.5848E-11	A	H	Teq
21,36	PC	TA_PC_B32_MUX	9	-25 to 50	°C	-24	-10	45	48	TA01p	5.0125E+1	-7.8916E-1	5.4339E-3	-2.0630E-5	3.7567E-8	-2.5848E-11	A	H	Teq
21,36	PC	TA_PC_B33_MUX	9	-25 to 50	°C	-24	-10	45	48	TA01p	5.0125E+1	-7.8916E-1	5.4339E-3	-2.0630E-5	3.7567E-8	-2.5848E-11	A	H	Teq
21,36	PC	TA_PC_B34_MUX	9	-25 to 50	°C	-24	-10	45	48	TA01p	5.0125E+1	-7.8916E-1	5.4339E-3	-2.0630E-5	3.7567E-8	-2.5848E-11	A	H	Teq
21,36	PC	TA_PC_B35_MUX	9	-25 to 50	°C	-24	-10	45	48	TA01p	5.0125E+1	-7.8916E-1	5.4339E-3	-2.0630E-5	3.7567E-8	-2.5848E-11	A	H	Teq
21,36	PC	TA_PC_B36_MUX	9	-25 to 50	°C	-24	-10	45	48	TA01p	5.0125E+1	-7.8916E-1	5.4339E-3	-2.0630E-5	3.7567E-8	-2.5848E-11	A	H	Teq
10,23	PC	VR_PC_B31C01_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B31C02_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B31C03_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B31C04_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B31C05_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B31C06_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B31C07_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B31C08_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B31C09_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B31C10_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
	PC	VR_PC_B31_GND	8	-2.5 to 2.5	V	-0.75	-0.50	0.50	0.75	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	H	1.0V/V;0.0V
	PC	VR_PC_B31_RN12V	8	-15 to 0	V	-12.75	-12.50	-11.50	-11.25	VR04	-1.4975E+1	1.1699E-1	0	0	0	0	APC	H	5.9899V/V;-12.0V
	PC	VR_PC_B31_RN5V	8	-7.5 to 0	V	-5.50	-5.25	-4.75	-4.50	VR05	-7.5100E+0	5.8672E-2	0	0	0	0	APC	H	3.0040V/V;-5V
	PC	VR_PC_B31_RP12V	8	0 to 15	V	11.25	11.50	12.50	12.75	VR04	-1.4975E+1	1.1699E-1	0	0	0	0	APC	H	5.9899V/V;+12.0V
	PC	VR_PC_B31_RP5V	8	0 to 7.5	V	4.50	4.75	5.25	5.50	VR05	-7.5100E+0	5.8672E-2	0	0	0	0	APC	H	3.0040V/V;5V
10,23	PC	VR_PC_B32C01_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B32C02_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B32C03_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B32C04_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B32C05_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B32C06_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B32C07_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B32C08_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B32C09_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V

TABLE 20-5. MODIS ACTIVE ANALOG TELEMETRY/ENGINEERING LIMITS & EQUATIONS

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• **See bottom Notes.** • **Equations are 5th order polynomial form: EU = C0 + C1(DN) + C2(DN)^2 + C3(DN)^3 + C4(DN)^4 + C5(DN)^5.**

pf chg#	1 Subsys	2 Telemetry Mnemonic Name	3 # of Bits	4 Approx Tlmy Range	5 Eng Units	6a Red Low	6b Yellow Low	6c Yellow High	6d Red High	7a Eq #	7b C0	7c C1	7d C2	7e C3	7f C4	7g C5	8 Type /Use	9 Use	10 Ref EU SF/Nom
												Telemetry DN to Eng Units Equation Coefficients							
10,23	PC	VR_PC_B32C10_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
	PC	VR_PC_B32_GND	8	-2.5 to 2.5	V	-0.75	-0.50	0.50	0.75	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	H	1.0V/V;0.0V
	PC	VR_PC_B32_RN12V	8	-15 to 0	V	-12.75	-12.50	-11.50	-11.25	VR04	-1.4975E+1	1.1699E-1	0	0	0	0	APC	H	5.9899V/V;-12.0V
	PC	VR_PC_B32_RN5V	8	-7.5 to 0	V	-5.50	-5.25	-4.75	-4.50	VR05	-7.5100E+0	5.8672E-2	0	0	0	0	APC	H	3.0040V/V; -5V
	PC	VR_PC_B32_RP12V	8	0 to 15	V	11.25	11.50	12.50	12.75	VR04	-1.4975E+1	1.1699E-1	0	0	0	0	APC	H	5.9899V/V;+12.0V
	PC	VR_PC_B32_RP5V	8	0 to 7.5	V	4.50	4.75	5.25	5.50	VR05	-7.5100E+0	5.8672E-2	0	0	0	0	APC	H	3.0040V/V;5V
10,23	PC	VR_PC_B33C01_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B33C02_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B33C03_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B33C04_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B33C05_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B33C06_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B33C07_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B33C08_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B33C09_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B33C10_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
	PC	VR_PC_B33_GND	8	-2.5 to 2.5	V	-0.75	-0.50	0.50	0.75	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	H	1.0V/V;0.0V
	PC	VR_PC_B33_RN12V	8	-15 to 0	V	-12.75	-12.50	-11.50	-11.25	VR04	-1.4975E+1	1.1699E-1	0	0	0	0	APC	H	5.9899V/V;-12.0V
	PC	VR_PC_B33_RN5V	8	-7.5 to 0	V	-5.50	-5.25	-4.75	-4.50	VR05	-7.5100E+0	5.8672E-2	0	0	0	0	APC	H	3.0040V/V;-5V
	PC	VR_PC_B33_RP12V	8	0 to 15	V	11.25	11.50	12.50	12.75	VR04	-1.4975E+1	1.1699E-1	0	0	0	0	APC	H	5.9899V/V;+12.0V
	PC	VR_PC_B33_RP5V	8	0 to 7.5	V	4.50	4.75	5.25	5.50	VR05	-7.5100E+0	5.8672E-2	0	0	0	0	APC	H	3.0040V/V;5V
10,23	PC	VR_PC_B34C01_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B34C02_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B34C03_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B34C04_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B34C05_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B34C06_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B34C07_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B34C08_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B34C09_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B34C10_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
	PC	VR_PC_B34_GND	8	-2.5 to 2.5	V	-0.75	-0.50	0.50	0.75	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	H	1.0V/V;0.0V
	PC	VR_PC_B34_RN12V	8	-15 to 0	V	-12.75	-12.50	-11.50	-11.25	VR04	-1.4975E+1	1.1699E-1	0	0	0	0	APC	H	5.9899V/V;-12.0V
	PC	VR_PC_B34_RN5V	8	-7.5 to 0	V	-5.50	-5.25	-4.75	-4.50	VR05	-7.5100E+0	5.8672E-2	0	0	0	0	APC	H	3.0040V/V;-5V
	PC	VR_PC_B34_RP12V	8	0 to 15	V	11.25	11.50	12.50	12.75	VR04	-1.4975E+1	1.1699E-1	0	0	0	0	APC	H	5.9899V/V;+12.0V
	PC	VR_PC_B34_RP5V	8	0 to 7.5	V	4.50	4.75	5.25	5.50	VR05	-7.5100E+0	5.8672E-2	0	0	0	0	APC	H	3.0040V/V;5V
10,23	PC	VR_PC_B35C01_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B35C02_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B35C03_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B35C04_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V

TABLE 20-5. MODIS ACTIVE ANALOG TELEMETRY/ENGINEERING LIMITS & EQUATIONS

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• See bottom Notes. • Equations are 5th order polynomial form: EU = C0 + C1(DN) + C2(DN)^2 + C3(DN)^3 + C4(DN)^4 + C5(DN)^5.

pf chg#	1 Subsys	2 Telemetry Mnemonic Name	3 # of Bits	4 Approx Tlmy Range	5 Eng Units	6a Red Low	6b Yellow Low	6c Yellow High	6d Red High	7a Eq #	7b C0	7c C1	7d C2	7e C3	7f C4	7g C5	8 Type /Use	9 Use	10 Ref EU SF/Nom
												Telemetry DN to Eng Units Equation Coefficients							
10,23	PC	VR_PC_B35C05_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B35C06_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B35C07_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B35C08_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B35C09_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B35C10_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
	PC	VR_PC_B35_GND	8	-2.5 to 2.5	V	-0.75	-0.50	0.50	0.75	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	H	1.0V/V;0.0V
	PC	VR_PC_B35_RN12V	8	-15 to 0	V	-12.75	-12.50	-11.50	-11.25	VR04	-1.4975E+1	1.1699E-1	0	0	0	0	APC	H	5.9899V/V;-12.0V
	PC	VR_PC_B35_RN5V	8	-7.5 to 0	V	-5.50	-5.25	-4.75	-4.50	VR05	-7.5100E+0	5.8672E-2	0	0	0	0	APC	H	3.0040V/V;-5V
	PC	VR_PC_B35_RP12V	8	0 to 15	V	11.25	11.50	12.50	12.75	VR04	-1.4975E+1	1.1699E-1	0	0	0	0	APC	H	5.9899V/V;+12.0V
	PC	VR_PC_B35_RP5V	8	0 to 7.5	V	4.50	4.75	5.25	5.50	VR05	-7.5100E+0	5.8672E-2	0	0	0	0	APC	H	3.0040V/V;5V
10,23	PC	VR_PC_B36C01_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B36C02_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B36C03_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B36C04_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B36C05_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B36C06_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B36C07_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B36C08_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B36C09_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
10,23	PC	VR_PC_B36C10_DCR	8	-2.5 to 2.5	V	-	-	-	-	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	E	1.0V/V;0.0V
	PC	VR_PC_B36_GND	8	-2.5 to 2.5	V	-0.75	-0.50	0.50	0.75	VR03	-2.5000E+0	1.9531E-2	0	0	0	0	APC	H	1.0V/V; 0.0V
	PC	VR_PC_B36_RN12V	8	-15 to 0	V	-12.75	-12.50	-11.50	-11.25	VR04	-1.4975E+1	1.1699E-1	0	0	0	0	APC	H	5.9899V/V;-12.0V
	PC	VR_PC_B36_RN5V	8	-7.5 to 0	V	-5.50	-5.25	-4.75	-4.50	VR05	-7.5100E+0	5.8672E-2	0	0	0	0	APC	H	3.0040V/V;-5V
	PC	VR_PC_B36_RP12V	8	0 to 15	V	11.25	11.50	12.50	12.75	VR04	-1.4975E+1	1.1699E-1	0	0	0	0	APC	H	5.9899V/V;+12.0V
	PC	VR_PC_B36_RP5V	8	0 to 7.5	V	4.50	4.75	5.25	5.50	VR05	-7.5100E+0	5.8672E-2	0	0	0	0	APC	H	3.0040V/V;5V
25,38	PS	IR_PS1_INPUT_CUR	10	0 to 2.5	A	-0.30	-0.20	2.000	2.375	IR02ap	-4.2577E+0	8.3973E-3	-6.8084E-7	0	0	0	A	H	1.5A/V
25,38	PS	IR_PS2_INPUT_CUR	10	0 to 2.5	A	-0.30	-0.20	2.000	2.375	IR02bp	-4.4232E+0	8.6432E-3	-6.5924E-7	0	0	0	A	H	1.5A/V
9	PS	VR_PS1_N15V_A1ME	8	-20.4 to 0	Vdc	-16.4	-16.2	-13.9	-13.7	VR06	-2.0380E+1	1.5922E-1	0	0	0	0	A	H	8.15195V/V;-15.6V
1,9	PS	VR_PS1_N15V_A2AF	8	-20.4 to 0	Vdc	-17.8	-17.6	-14.5	-14.3	VR06	-2.0380E+1	1.5922E-1	0	0	0	0	A	H	8.15195V/V;-15.6V
9	PS	VR_PS1_N15V_A3AS	8	-20.4 to 0	Vdc	-17.8	-17.6	-15.0	-14.8	VR06	-2.0380E+1	1.5922E-1	0	0	0	0	A	H	8.15195V/V;-15.6V
9	PS	VR_PS1_N30V_A1ME	8	-37.5 to 0	Vdc	-34.3	-34.1	-28.9	-28.7	VR07	-3.7456E+1	2.9262E-1	0	0	0	0	A	H	14.98239V/V;-30V
9	PS	VR_PS1_N8V_A2	8	-11.8 to 0	Vdc	-9.7	-9.5	-7.9	-7.7	VR08	-1.1835E+1	9.2464E-2	0	0	0	0	A	H	4.73417V/V;-8.5V
9	PS	VR_PS1_P15V_A1ME	8	0 to 20.4	Vdc	13.7	13.9	16.2	16.4	VR06	-2.0380E+1	1.5922E-1	0	0	0	0	A	H	8.15195V/V;15.6V
9	PS	VR_PS1_P15V_A2AF	8	0 to 20.4	Vdc	14.7	14.9	17.6	17.8	VR06	-2.0380E+1	1.5922E-1	0	0	0	0	A	H	8.15195V/V;15.6V
9	PS	VR_PS1_P15V_A3AS	8	0 to 20.4	Vdc	14.7	14.9	18.2	18.4	VR06	-2.0380E+1	1.5922E-1	0	0	0	0	A	H	8.15195V/V;15.6V
9,38	PS	VR_PS1_P30V_A1	8	0 to 37.5	Vdc	28.5	29.0	34.7	34.9	VR07	-3.7456E+1	2.9262E-1	0	0	0	0	A	H	14.98239V/V;30V
30,37	PS	VR_PS1_P5_6V_D1	8	0 to 6.3	Vdc	5.5	5.6	6.0	6.1	VR09	-6.2658E+0	4.8952E-2	0	0	0	0	A	H	2.50632V/V;5.6V
9	PS	VR_PS1_P88V_A1ME	8	0 to 124	Vdc	77.0	79.0	111.0	113.0	VR10	-1.2389E+2	9.6785E-1	0	0	0	0	A	H	49.554V/V;88V
9	PS	VR_PS1_P8V_A2	8	0 to 11.8	Vdc	7.7	7.9	9.5	9.7	VR08	-1.1835E+1	9.2464E-2	0	0	0	0	A	H	4.73417V/V;8.5V

TABLE 20-5. MODIS ACTIVE ANALOG TELEMETRY/ENGINEERING LIMITS & EQUATIONS

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• See bottom Notes. • Equations are 5th order polynomial form: EU = C0 + C1(DN) + C2(DN)^2 + C3(DN)^3 + C4(DN)^4 + C5(DN)^5.

pf chg#	1 Subsys	2 Telemetry Mnemonic Name	3 # of Bits	4 Approx Tlmy Range	5 Eng Units	6a Red Low	6b Yellow Low	6c Yellow High	6d Red High	7a Eq #	7b C0	7c C1	7d C2	7e C3	7f C4	7g C5	8 Type /Use	9 Use	10 Ref EU SF/Nom
												Telemetry DN to Eng Units Equation Coefficients							
9	PS	VR_PS1_P8V_N1ME	8	0 to 11.8	Vdc	7.7	7.9	11.1	11.3	VR08	-1.1835E+1	9.2464E-2	0	0	0	0	A	H	4.73417V/V;8.5V
9	PS	VR_PS2_N15V_A1ME	8	-20.4 to 0	Vdc	-16.4	-16.2	-13.9	-13.7	VR06	-2.0380E+1	1.5922E-1	0	0	0	0	A	H	8.15195V/V;-15.6V
1,9	PS	VR_PS2_N15V_A2AF	8	-20.4 to 0	Vdc	-17.8	-17.6	-14.5	-14.3	VR06	-2.0380E+1	1.5922E-1	0	0	0	0	A	H	8.15195V/V;-15.6V
9	PS	VR_PS2_N15V_A3AS	8	-20.4 to 0	Vdc	-17.8	-17.6	-15.0	-14.8	VR06	-2.0380E+1	1.5922E-1	0	0	0	0	A	H	8.15195V/V;-15.6V
9	PS	VR_PS2_N30V_A1ME	8	-37.5 to 0	Vdc	-34.3	-34.1	-28.9	-28.7	VR07	-3.7456E+1	2.9262E-1	0	0	0	0	A	H	14.98239V/V;-30V
9	PS	VR_PS2_N8V_A2	8	-11.8 to 0	Vdc	-9.7	-9.5	-7.9	-7.7	VR08	-1.1835E+1	9.2464E-2	0	0	0	0	A	H	4.73417V/V;-8.5V
9	PS	VR_PS2_P15V_A1ME	8	0 to 20.4	Vdc	13.7	13.9	16.2	16.4	VR06	-2.0380E+1	1.5922E-1	0	0	0	0	A	H	8.15195V/V;15.6V
9	PS	VR_PS2_P15V_A2AF	8	0 to 20.4	Vdc	14.7	14.9	17.6	17.8	VR06	-2.0380E+1	1.5922E-1	0	0	0	0	A	H	8.15195V/V;15.6V
9	PS	VR_PS2_P15V_A3AS	8	0 to 20.4	Vdc	14.7	14.9	18.2	18.4	VR06	-2.0380E+1	1.5922E-1	0	0	0	0	A	H	8.15195V/V;15.6V
9,38	PS	VR_PS2_P30V_A1	8	0 to 37.5	Vdc	28.5	29.0	34.7	34.9	VR07	-3.7456E+1	2.9262E-1	0	0	0	0	A	H	14.98239V/V;30V
30,37	PS	VR_PS2_P5_6V_D1	8	0 to 6.3	Vdc	5.5	5.6	6.0	6.1	VR09	-6.2658E+0	4.8952E-2	0	0	0	0	A	H	2.50632V/V;5.6V
9	PS	VR_PS2_P88V_A1ME	8	0 to 124	Vdc	77.0	79.0	111.0	113.0	VR10	-1.2389E+2	9.6785E-1	0	0	0	0	A	H	49.554V/V;88V
9	PS	VR_PS2_P8V_A2	8	0 to 11.8	Vdc	7.7	7.9	9.5	9.7	VR08	-1.1835E+1	9.2464E-2	0	0	0	0	A	H	4.73417V/V;8.5V
9	PS	VR_PS2_P8V_N1ME	8	0 to 11.8	Vdc	7.7	7.9	11.1	11.3	VR08	-1.1835E+1	9.2464E-2	0	0	0	0	A	H	4.73417V/V;8.5V
17,24,38	PV	CR_PVLW_S_DELAY	8	0 to 210	µs	-4	-2	37	41	CR01	-2.0995E+2	1.6403E+0	0	0	0	0	APV	E	87.7µs/V;0-41µs
17,24,38	PV	CR_PVLW_S_DELAYH	8	0 to 210	µs	-4	-2	37	41	CR01	-2.0995E+2	1.6403E+0	0	0	0	0	APV	H	87.7µs/V;0-41µs
17,24,38	PV	CR_PVNIR_S_DELAY	8	0 to 210	µs	-4	-2	162	166	CR01	-2.0995E+2	1.6403E+0	0	0	0	0	APV	E	87.7µs/V;0-166µs
17,24,38	PV	CR_PVNIR_S_DELYH	8	0 to 210	µs	-4	-2	162	166	CR01	-2.0995E+2	1.6403E+0	0	0	0	0	APV	H	87.7µs/V;0-166µs
17,24,38	PV	CR_PVSM_S_DELAY	8	0 to 210	µs	-4	-2	162	166	CR01	-2.0995E+2	1.6403E+0	0	0	0	0	APV	E	87.7µs/V;0-166µs
17,24,38	PV	CR_PVSM_S_DELAYH	8	0 to 210	µs	-4	-2	162	166	CR01	-2.0995E+2	1.6403E+0	0	0	0	0	APV	H	87.7µs/V;0-166µs
17,24,38	PV	CR_PVVIS_S_DELAY	8	0 to 210	µs	-4	-2	162	166	CR01	-2.0995E+2	1.6403E+0	0	0	0	0	APV	E	87.7µs/V;0-166µs
17,24,38	PV	CR_PVVIS_S_DELYH	8	0 to 210	µs	-4	-2	162	166	CR01	-2.0995E+2	1.6403E+0	0	0	0	0	APV	H	87.7µs/V;0-166µs
17,21,36	PV	TA_PVLW_PWB4_10	9	-19 to 79	°C	-17	-15	50	75	TA02P	-1.8888E+1	4.9724E-1	-2.3834E-3	8.1515E-6	-1.3848E-8	9.2793E-12	APV	H	Teq
17,21,36	PV	TA_PVNIR_PWB2_8	9	-19 to 79	°C	-17	-15	50	75	TA02P	-1.8888E+1	4.9724E-1	-2.3834E-3	8.1515E-6	-1.3848E-8	9.2793E-12	APV	H	Teq
17,21,36	PV	TA_PVNIR_PWB3_9	9	-19 to 79	°C	-17	-15	50	75	TA02P	-1.8888E+1	4.9724E-1	-2.3834E-3	8.1515E-6	-1.3848E-8	9.2793E-12	APV	H	Teq
17,21,36	PV	TA_PVSM_PWB5_11	9	-19 to 79	°C	-17	-15	50	75	TA02P	-1.8888E+1	4.9724E-1	-2.3834E-3	8.1515E-6	-1.3848E-8	9.2793E-12	APV	H	Teq
17,21,36	PV	TA_PVSM_PWB6_12	9	-19 to 79	°C	-17	-15	50	75	TA02P	-1.8888E+1	4.9724E-1	-2.3834E-3	8.1515E-6	-1.3848E-8	9.2793E-12	APV	H	Teq
17,21,36	PV	TA_PVVIS_PWB1_7	9	-19 to 79	°C	-17	-15	50	75	TA02P	-1.8888E+1	4.9724E-1	-2.3834E-3	8.1515E-6	-1.3848E-8	9.2793E-12	APV	H	Teq
17,31	PV	VR_PVLW_ITWKA	8	-4.56 to 0	V	-4.50	-4.45	-2.50	-2.45	V R11	-4.5620E+0	3.5641E-2	0	0	0	0	APV	E	1.8248V/V;-4.45to-2.5
17,31,38	PV	VR_PVLW_P30V	8	0 to 35.8	V	26.00	26.60	31.75	32.00	VR12	-3.5868E+1	2.8022E-1	0	0	0	0	APV	H	14.3472V/V;+30V
	PV	VR_PVLW_RN11V	8	-12.5 to 0	V	-12.25	-12.00	-10.00	-9.75	VR13	-1.2563E+1	9.8146E-2	0	0	0	0	APV	H	5.0251V/V;-11V
	PV	VR_PVLW_RN5V	8	-5.6 to 0	V	-5.4	-5.3	-4.7	-4.6	VR14	-5.6688E+0	4.4287E-2	0	0	0	0	APV	H	2.2675V/V;-5V
	PV	VR_PVLW_RP11V	8	0 to 12.5	V	9.75	10.00	12.00	12.25	VR13	-1.2563E+1	9.8146E-2	0	0	0	0	APV	H	5.0251V/V;+11V
	PV	VR_PVLW_RP5V	8	0 to 5.6	V	4.6	4.7	5.3	5.4	VR14	-5.6688E+0	4.4287E-2	0	0	0	0	APV	H	2.2675V/V;+5V
17	PV	VR_PVLW_VCAL	8	-10 to 10	V	-8.1	-8.0	1.0	1.1	VR15	-1.0040E+1	7.8438E-2	0	0	0	0	APV	E	4.0160V/V;-8 to +1V
17	PV	VR_PVLW_VCALH	8	-10 to 10	V	-8.1	-8.0	1.0	1.1	VR15	-1.0040E+1	7.8438E-2	0	0	0	0	APV	H	4.0160V/V;-8 to +1V
17,31	PV	VR_PVLW_VDDA	8	-10 to 0	V	-9.0	-8.3	-7.7	-7.0	VR15	-1.0040E+1	7.8438E-2	0	0	0	0	APV	E	4.0160V/V;-8.1 to -7.7V
17,31	PV	VR_PVLW_VDDD	8	-10 to 0	V	-9.0	-8.3	-7.7	-7.0	VR15	-1.0040E+1	7.8438E-2	0	0	0	0	APV	E	4.0160V/V;-8.1 to -7.7V
17,31	PV	VR_PVLW_VDDOUT	8	-10 to 0	V	-9.0	-8.3	-7.7	-7.0	VR15	-1.0040E+1	7.8438E-2	0	0	0	0	APV	E	4.0160V/V;-8.1 to -7.7V
	PV	VR_PVLW_VDET	8	-25 to 0	V	-8.2	-8.0	-2.0	-1.8	VR16	-2.5253E+1	1.9729E-1	0	0	0	0	APV	E	10.1010V/V; -8 to -2V

TABLE 20-5. MODIS ACTIVE ANALOG TELEMETRY/ENGINEERING LIMITS & EQUATIONS

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• See bottom Notes. • Equations are 5th order polynomial form: EU = C0 + C1(DN) + C2(DN)^2 + C3(DN)^3 + C4(DN)^4 + C5(DN)^5.

pf chg#	1 Subsys	2 Telemetry Mnemonic Name	3 # of Bits	4 Approx Tlmy Range	5 Eng Units	6a Red Low	6b Yellow Low	6c Yellow High	6d Red High	7a Eq #	7b C0	7c C1	7d C2	7e C3	7f C4	7g C5	8 Type /Use	9 Use	10 Ref EU SF/Nom
												Telemetry DN to Eng Units Equation Coefficients							
31	PV	VR_PVLW_VPWELL	8	-10 to 0	V	-9.0	-8.3	-7.7	-7.0	VR15	-1.0040E+1	7.8438E-2	0	0	0	0	APV	E	4.0160V/V;-9 to -7V
31	PV	VR_PVNIR_ITWKA	8	-4.56 to 0	V	-4.50	-4.45	-2.50	-2.45	V R11	-4.5620E+0	3.5641E-2	0	0	0	0	APV	E	1.8248V/V;-4.5to-2.5
17,31,38	PV	VR_PVNIR_P30V	8	0 to 35.8	V	26.00	26.60	31.75	32.00	VR12	-3.5868E+1	2.8022E-1	0	0	0	0	APV	H	14.3472V/V;+30V
38	PV	VR_PVNIR_P5VD3_9	8	0 to 5.6	V	4.60	4.65	5.30	5.40	VR14	-5.6688E+0	4.4287E-2	0	0	0	0	APV	H	2.2675V/V;-5V
	PV	VR_PVNIR_RN11V28	8	-12.5 to 0	V	-12.25	-12.00	-10.00	-9.75	VR13	-1.2563E+1	9.8146E-2	0	0	0	0	APV	H	5.0251V/V;-11V
	PV	VR_PVNIR_RN11V39	8	-12.5 to 0	V	-12.25	-12.00	-10.00	-9.75	VR13	-1.2563E+1	9.8146E-2	0	0	0	0	APV	H	5.0251V/V; -11V
	PV	VR_PVNIR_RN5V2_8	8	-5.6 to 0	V	-5.4	-5.3	-4.7	-4.6	VR14	-5.6688E+0	4.4287E-2	0	0	0	0	APV	H	2.2675V/V;-5V
	PV	VR_PVNIR_RN5V3_9	8	-5.6 to 0	V	-5.4	-5.3	-4.7	-4.6	VR14	-5.6688E+0	4.4287E-2	0	0	0	0	APV	H	2.2675V/V;-5V
	PV	VR_PVNIR_RP11V28	8	0 to 12.5	V	9.75	10.00	12.00	12.25	VR13	-1.2563E+1	9.8146E-2	0	0	0	0	APV	H	5.0251V/V;+11V
	PV	VR_PVNIR_RP11V39	8	0 to 12.5	V	9.75	10.00	12.00	12.25	VR13	-1.2563E+1	9.8146E-2	0	0	0	0	APV	H	5.0251V/V;+11V
	PV	VR_PVNIR_RP5V2_8	8	0 to 5.6	V	4.6	4.7	5.3	5.4	VR14	-5.6688E+0	4.4287E-2	0	0	0	0	APV	H	2.2675V/V;+5V
	PV	VR_PVNIR_RP5V3_9	8	0 to 5.6	V	4.6	4.7	5.3	5.4	VR14	-5.6688E+0	4.4287E-2	0	0	0	0	APV	H	2.2675V/V;+5V
17	PV	VR_PVNIR_VCAL	8	-10 to 10	V	-8.1	-8.0	1.0	1.1	VR15	-1.0040E+1	7.8438E-2	0	0	0	0	APV	E	4.0160V/V;-8 to +1V
17	PV	VR_PVNIR_VCALH	8	-10 to 10	V	-8.1	-8.0	1.0	1.1	VR15	-1.0040E+1	7.8438E-2	0	0	0	0	APV	H	4.0160V/V;-8 to +1V
17	PV	VR_PVNIR_VD1	8	0 to 25	V	14.8	15.0	16.0	16.5	VR16	-2.5253E+1	1.9729E-1	0	0	0	0	APV	E	10.1010V/V;+15to+16
17,31	PV	VR_PVNIR_VDDA	8	-10 to 0	V	-9.0	-8.3	-7.7	-7.0	VR15	-1.0040E+1	7.8438E-2	0	0	0	0	APV	E	4.0160V/V;-8.1 to -7.7V
17,31	PV	VR_PVNIR_VDDD	8	-10 to 0	V	-9.0	-8.3	-7.7	-7.0	VR15	-1.0040E+1	7.8438E-2	0	0	0	0	APV	E	4.0160V/V;-8.1 to -7.7V
17,31	PV	VR_PVNIR_VDDOUT	8	-10 to 0	V	-9.0	-8.3	-7.7	-7.0	VR15	-1.0040E+1	7.8438E-2	0	0	0	0	APV	E	4.0160V/V;-8.1 to -7.7V
17	PV	VR_PVNIR_VDET	8	0 to 25	V	14.8	15.0	16.0	16.5	VR16	-2.5253E+1	1.9729E-1	0	0	0	0	APV	E	10.1010V/V;+15 to +16
17	PV	VR_PVNIR_VGUARD	8	-2.5 to 0	V	-2.50	-2.00	-1.00	-0.50	VR17	-2.5000E+0	1.9531E-2	0	0	0	0	APV	E	1V/V;-2 to -1V
31	PV	VR_PVNIR_VPWELL	8	-10 to 0	V	-9.0	-8.3	-7.7	-7.0	VR15	-1.0040E+1	7.8438E-2	0	0	0	0	APV	E	4.0160V/V;-9 to -7V
	PV	VR_PVSM_ITWKA	8	-4.6 to 0	V	-4.55	-4.50	-2.50	-2.45	V R11	-4.5620E+0	3.5641E-2	0	0	0	0	APV	E	1.8248V/V;-4.5 to -2.5
17,38	PV	VR_PVSM_P30V	8	0 to 35.8	V	26.00	26.60	31.75	32.00	VR12	-3.5868E+1	2.8022E-1	0	0	0	0	APV	H	14.3472V/V;+30V
38	PV	VR_PVSM_P5VD6_12	8	0 to 5.6	V	4.60	4.65	5.30	5.40	VR14	-5.6688E+0	4.4287E-2	0	0	0	0	APV	H	2.2675V/V;+5V
	PV	VR_PVSM_RN11V511	8	-12.5 to 0	V	-12.25	-12.00	-10.00	-9.75	VR13	-1.2563E+1	9.8146E-2	0	0	0	0	APV	H	5.0251V/V;-11V
	PV	VR_PVSM_RN11V612	8	-12.5 to 0	V	-12.25	-12.00	-10.00	-9.75	VR13	-1.2563E+1	9.8146E-2	0	0	0	0	APV	H	5.0251V/V;-11V
	PV	VR_PVSM_RN5V5_11	8	-5.6 to 0	V	-5.4	-5.3	-4.7	-4.6	VR14	-5.6688E+0	4.4287E-2	0	0	0	0	APV	H	2.2675V/V;-5V
	PV	VR_PVSM_RN5V6_12	8	-5.6 to 0	V	-5.4	-5.3	-4.7	-4.6	VR14	-5.6688E+0	4.4287E-2	0	0	0	0	APV	H	2.2675V/V;-5V
	PV	VR_PVSM_RP11V511	8	0 to 12.5	V	9.75	10.00	12.00	12.25	VR13	-1.2563E+1	9.8146E-2	0	0	0	0	APV	H	5.0251V/V;+11V
	PV	VR_PVSM_RP11V612	8	0 to 12.5	V	9.75	10.00	12.00	12.25	VR13	-1.2563E+1	9.8146E-2	0	0	0	0	APV	H	5.0251V/V;+11V
	PV	VR_PVSM_RP5V5_11	8	0 to 5.6	V	4.6	4.7	5.3	5.4	VR14	-5.6688E+0	4.4287E-2	0	0	0	0	APV	H	2.2675V/V;+5V
	PV	VR_PVSM_RP5V6_12	8	0 to 5.6	V	4.6	4.7	5.3	5.4	VR14	-5.6688E+0	4.4287E-2	0	0	0	0	APV	H	2.2675V/V;+5V
17	PV	VR_PVSM_VCAL	8	-10 to 10	V	-8.1	-8.0	1.0	1.1	VR15	-1.0040E+1	7.8438E-2	0	0	0	0	APV	E	4.0160V/V;-8 to +1V
17	PV	VR_PVSM_VCALH	8	-10 to 10	V	-8.1	-8.0	1.0	1.1	VR15	-1.0040E+1	7.8438E-2	0	0	0	0	APV	H	4.0160V/V;-8 to +1V
17,31	PV	VR_PVSM_VDDA	8	-10 to 0	V	-9.0	-8.3	-7.7	-7.0	VR15	-1.0040E+1	7.8438E-2	0	0	0	0	APV	E	4.0160V/V;-8.1 to -7V
17,31	PV	VR_PVSM_VDDD	8	-10 to 0	V	-9.0	-8.3	-7.7	-7.0	VR15	-1.0040E+1	7.8438E-2	0	0	0	0	APV	E	4.0160V/V;-8.1 to -7V
17,31	PV	VR_PVSM_VDDOUT	8	-10 to 0	V	-9.0	-8.3	-7.7	-7.0	VR15	-1.0040E+1	7.8438E-2	0	0	0	0	APV	E	4.0160V/V;-8.1 to -7V
17	PV	VR_PVSM_VDET	8	-25 to 0	V	-8.2	-8.1	-2.0	-1.8	VR16	-2.5253E+1	1.9729E-1	0	0	0	0	APV	E	10.1010V/V;-8.1 to -2V
31	PV	VR_PVSM_VPWELL	8	-10 to 0	V	-9.0	-8.3	-7.7	-7.0	VR15	-1.0040E+1	7.8438E-2	0	0	0	0	APV	E	4.0160V/V;-9 to -7V
17	PV	VR_PVVIS_ITWKA	8	-4.6 to 0	V	-4.6	-4.5	-2.5	-2.5	V R11	-4.5620E+0	3.5641E-2	0	0	0	0	APV	E	1.8248V/V;-4.5 to -2.5

TABLE 20-5. MODIS ACTIVE ANALOG TELEMETRY/ENGINEERING LIMITS & EQUATIONS

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• See bottom Notes. • Equations are 5th order polynomial form: EU = C0 + C1(DN) + C2(DN)^2 + C3(DN)^3 + C4(DN)^4 + C5(DN)^5.

pf chg#	1 Subsys	2 Telemetry Mnemonic Name	3 # of Bits	4 Approx Tlmy Range	5 Eng Units	6a Red Low	6b Yellow Low	6c Yellow High	6d Red High	7a Eq #	7b C0	7c C1	7d C2	7e C3	7f C4	7g C5	8 Type /Use	9 Use	10 Ref EU SF/Nom
											Telemetry DN to Eng Units Equation Coefficients								
17,30,38	PV	VR_PVVIS_P30V	8	0 to 35.8	V	26.0	26.6	31.8	32.0	VR12	-3.5868E+1	2.8022E-1	0	0	0	0	APV	H	14.3472V/V;+30V
	PV	VR_PVVIS_RN11V	8	-12.5 to 0	V	-12.3	-12.0	-10.0	-9.8	VR13	-1.2563E+1	9.8146E-2	0	0	0	0	APV	H	5.0251V/V;-11V
	PV	VR_PVVIS_RN5V	8	-5.6 to 0	V	-5.4	-5.3	-4.7	-4.6	VR14	-5.6688E+0	4.4287E-2	0	0	0	0	APV	H	2.2675V/V;-5V
	PV	VR_PVVIS_RP11V	8	0 to 12.5	V	9.8	10.0	12.0	12.3	VR13	-1.2563E+1	9.8146E-2	0	0	0	0	APV	H	5.0251V/V;+11V
	PV	VR_PVVIS_RP5V	8	0 to 5.6	V	4.6	4.7	5.3	5.4	VR14	-5.6688E+0	4.4287E-2	0	0	0	0	APV	H	2.2675V/V;+5V
17	PV	VR_PVVIS_VCAL	8	-10 to 10	V	-8.1	-8.0	1.0	1.1	VR15	-1.0040E+1	7.8438E-2	0	0	0	0	APV	E	4.0160V/V;-8 to +1V
17	PV	VR_PVVIS_VCALH	8	-10 to 10	V	-8.1	-8.0	1.0	1.1	VR15	-1.0040E+1	7.8438E-2	0	0	0	0	APV	H	4.0160V/V;-8 to +1V
17	PV	VR_PVVIS_VD1	8	0 to 25	V	14.8	15.0	16.0	16.5	VR16	-2.5253E+1	1.9729E-1	0	0	0	0	APV	E	10.1010V/V;+15 to +16
17,31	PV	VR_PVVIS_VDDA	8	-10 to 0	V	-9.0	-8.3	-7.7	-7.0	VR15	-1.0040E+1	7.8438E-2	0	0	0	0	APV	E	4.0160V/V;-8.1 to -7V
17,31	PV	VR_PVVIS_VDDD	8	-10 to 0	V	-9.0	-8.3	-7.7	-7.0	VR15	-1.0040E+1	7.8438E-2	0	0	0	0	APV	E	4.0160V/V;-8.1 to -7V
17,31	PV	VR_PVVIS_VDDOUT	8	-10 to 0	V	-9.0	-8.3	-7.7	-7.0	VR15	-1.0040E+1	7.8438E-2	0	0	0	0	APV	E	4.0160V/V;-8.1 to -7V
17	PV	VR_PVVIS_VDET	8	0 to 25	V	14.8	15.0	16.0	16.5	VR16	-2.5253E+1	1.9729E-1	0	0	0	0	APV	E	10.1010V/V;+15 to +16
17	PV	VR_PVVIS_VGUARD	8	-2.5 to 0	V	-2.1	-2.0	-1.0	-0.9	VR17	-2.5000E+0	1.9531E-2	0	0	0	0	APV	E	1V/V;-2 to -1V
31	PV	VR_PVVIS_VPWELL	8	-10 to 0	V	-9.0	-8.3	-7.7	-7.0	VR15	-1.0040E+1	7.8438E-2	0	0	0	0	APV	E	4.0160V/V;-9 to -7V
21	RC	TA_RC_CS	12	50 to 100	K	-	-	-	-	TA03hp	-2.6607E+0	2.9239E-2	-1.2789E-6	1.4882E-10	0	0	A	H	Teq
21,38	RC	TA_RC_CS_OG	12	30 to 350	K	54	55	323	325	TA03p	-1.3726E+2	7.5134E-2	-2.7944E-6	3.5353E-9	0	0	A	H	Teq
21	RC	TA_RC_IS	12	90 to 170	K	-	-	-	-	TA04hp	3.1238E+1	2.6812E-2	1.8002E-6	2.8576E-11	0	0	A	H	Teq
21,38	RC	TA_RC_IS_OG	12	30 to 350	K	54	55	323	325	TA04p	-1.4316E+2	8.0885E-2	-4.5854E-6	3.7057E-9	0	0	A	H	Teq
20	RC	TA_RC_LWIR_CFPA	12	80.1 to 85.9	K	81.0	82.5	83.5	85.0	TA06p83	8.0062E+1	1.4493E-3	-6.8684E-9	1.9367E-12	-2.5410E-16	0	A	H	Teq
20	RC	TA_RC_LWIR_CFPA	12	82.1 to 87.9	K	83.0	84.5	85.5	87.0	TA06p85	8.2050E+1	1.4442E-3	-5.6085E-9	1.0498E-12	-1.0151E-16	0	A	H	Teq
20	RC	TA_RC_LWIR_CFPA	12	85.1 to 90.9	K	86.0	87.5	88.5	90.0	TA06p88	8.5048E+1	1.4388E-3	-8.8412E-9	2.5727E-12	-2.9433E-16	0	A	H	Teq
21,38	RC	TA_RC_OS_OG	12	30 to 350	K	54	55	323	325	TA05p	-1.4102E+2	7.9490E-2	-4.3164E-6	3.6498E-9	0	0	A	H	Teq
20	RC	TA_RC_SMIR_CFPA	12	55 to 118	K	81	82.3	83.7	85	TA07p83	4.9970E+1	1.8360E-2	-9.1174E-7	1.7673E-10	-1.3356E-14	0	A	H	Teq
20	RC	TA_RC_SMIR_CFPA	12	55 to 118	K	83	84.3	85.7	87	TA07p85	4.9912E+1	1.8426E-2	-9.6036E-7	1.9249E-10	-1.5208E-14	0	A	H	Teq
20	RC	TA_RC_SMIR_CFPA	12	55 to 118	K	86	87.3	88.7	90	TA07p88	4.9846E+1	1.8413E-2	-9.4652E-7	1.8741E-10	-1.4575E-14	0	A	H	Teq
8,32	RC	VR_RC_LW_FPA_HTR	10	0 to 15.0	Vdc	-	-	-	-	VR21	-1.4970E+1	2.9238E-2	0	0	0	0	A	H	5.988V/V
8,32	RC	VR_RC_SM_FPA_HTR	10	0 to 15.0	Vdc	-	-	-	-	VR21	-1.4970E+1	2.9238E-2	0	0	0	0	A	H	5.988V/V
15,39	SA	IR_SA_A_ECDR_LED	12	0 to 75	mA	10.00	13.00	37.00	40.00	IR03	-7.5000E+1	3.6621E-2	0	0	0	0	A	H	30mA/V;25.5mA
15,39	SA	IR_SA_B_ECDR_LED	12	0 to 75	mA	10.00	13.00	37.00	40.00	IR03	-7.5000E+1	3.6621E-2	0	0	0	0	A	H	30mA/V;25.5mA
15,39	SA	VR_SA_A_ECDR_MON	12	0 to 2.5	Vdc	0.00	1.30	2.30	2.50	VR22	-2.5000E+0	1.2207E-3	0	0	0	0	A	H	1V/V;1.8V
16,40	SA	VR_SA_A_MTR_TORQ	10	0 to 90	IN OZ	0.00	3.50	40.00	80.00	VR18	-9.0000E+1	1.7578E-1	0	0	0	0	A	H	36IN OZ/V;14.4IN OZ
16	SA	VR_SA_A_RN11V	8	-12.6 to 0	Vdc	-12.80	-11.80	-9.80	-8.80	VR19	-1.2600E+1	9.8438E-2	0	0	0	0	A	H	5.04V/V; -10.836V
16,34,38	SA	VR_SA_A_RP11V	8	0 to 12.6	Vdc	8.80	9.80	11.80	12.80	VR19	-1.2600E+1	9.8438E-2	0	0	0	0	A	H	5.04V/V; 10.836V
15,39	SA	VR_SA_B_ECDR_MON	12	0 to 2.5	Vdc	0.00	1.30	2.30	2.50	VR22	-2.5000E+0	1.2207E-3	0	0	0	0	A	H	1V/V;1.8V
16,40	SA	VR_SA_B_MTR_TORQ	10	0 to 90	IN OZ	0.00	3.50	40.00	80.00	VR18	-9.0000E+1	1.7578E-1	0	0	0	0	A	H	36IN OZ/V;14.4IN OZ
16,34	SA	VR_SA_B_RN11V	8	-12.6 to 0	Vdc	-12.80	-11.80	-9.80	-8.80	VR19	-1.2600E+1	9.8438E-2	0	0	0	0	A	H	5.04V/V; -10.836V
16,34,38	SA	VR_SA_B_RP11V	8	0 to 12.6	Vdc	8.80	9.80	11.80	12.80	VR19	-1.2600E+1	9.8438E-2	0	0	0	0	A	H	5.04V/V; 10.836V
7,33	SM	VR_SM01_SMPL1	12	0 to 40.2	mW/cm2-s-µ	-	-	-	-	VR23.1	-1.7450E+0	1.0241E-2	0	0	0	0	A	E	Eq
7,33	SM	VR_SM01_SMPL2	12	0 to 40.2	mW/cm2-s-µ	-	-	-	-	VR23.1	-1.7450E+0	1.0241E-2	0	0	0	0	A	E	Eq
7,33	SM	VR_SM01_SMPL3	12	0 to 40.2	mW/cm2-s-µ	-	-	-	-	VR23.1	-1.7450E+0	1.0241E-2	0	0	0	0	A	E	Eq

TABLE 20-5. MODIS ACTIVE ANALOG TELEMETRY/ENGINEERING LIMITS & EQUATIONS

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• **See bottom Notes.** • **Equations are 5th order polynomial form: EU = C0 + C1(DN) + C2(DN)^2 + C3(DN)^3 + C4(DN)^4 + C5(DN)^5.**

pf chg#	1 Subsys	2 Telemetry Mnemonic Name	3 # of Bits	4 Approx Tlmy Range	5 Eng Units	6a Red Low	6b Yellow Low	6c Yellow High	6d Red High	7a Eq #	7b C0	7c C1	7d C2	7e C3	7f C4	7g C5	8 Type /Use	9 Use	10 Ref EU SF/Nom
											Telemetry DN to Eng Units Equation Coefficients								
7,33	SM	VR_SM02_SMPL1	12	0 to 47.5	mW/cm2-s-µ	-	-	-	-	VR23.2	-1.0777E+0	1.1851E-2	0	0	0	0	A	E	Eq
7,33	SM	VR_SM02_SMPL2	12	0 to 47.5	mW/cm2-s-µ	-	-	-	-	VR23.2	-1.0777E+0	1.1851E-2	0	0	0	0	A	E	Eq
7,33	SM	VR_SM02_SMPL3	12	0 to 47.5	mW/cm2-s-µ	-	-	-	-	VR23.2	-1.0777E+0	1.1851E-2	0	0	0	0	A	E	Eq
7,33	SM	VR_SM03_SMPL1	12	0 to 43.8	mW/cm2-s-µ	-	-	-	-	VR23.3	-9.8478E-1	1.0928E-2	0	0	0	0	A	E	Eq
7,33	SM	VR_SM03_SMPL2	12	0 to 43.8	mW/cm2-s-µ	-	-	-	-	VR23.3	-9.8478E-1	1.0928E-2	0	0	0	0	A	E	Eq
7,33	SM	VR_SM03_SMPL3	12	0 to 43.8	mW/cm2-s-µ	-	-	-	-	VR23.3	-9.8478E-1	1.0928E-2	0	0	0	0	A	E	Eq
7,33	SM	VR_SM04_SMPL1	12	0 to 42.1	mW/cm2-s-µ	-	-	-	-	VR23.4	-9.5525E-1	1.0505E-2	0	0	0	0	A	E	Eq
7,33	SM	VR_SM04_SMPL2	12	0 to 42.1	mW/cm2-s-µ	-	-	-	-	VR23.4	-9.5525E-1	1.0505E-2	0	0	0	0	A	E	Eq
7,33	SM	VR_SM04_SMPL3	12	0 to 42.1	mW/cm2-s-µ	-	-	-	-	VR23.4	-9.5525E-1	1.0505E-2	0	0	0	0	A	E	Eq
7,33	SM	VR_SM05_SMPL1	12	0 to 35.3	mW/cm2-s-µ	-	-	-	-	VR23.5	-8.0260E-1	8.8265E-3	0	0	0	0	A	E	Eq
7,33	SM	VR_SM05_SMPL2	12	0 to 35.3	mW/cm2-s-µ	-	-	-	-	VR23.5	-8.0260E-1	8.8265E-3	0	0	0	0	A	E	Eq
7,33	SM	VR_SM05_SMPL3	12	0 to 35.3	mW/cm2-s-µ	-	-	-	-	VR23.5	-8.0260E-1	8.8265E-3	0	0	0	0	A	E	Eq
7,33	SM	VR_SM06_SMPL1	12	0 to 29.6	mW/cm2-s-µ	-	-	-	-	VR23.6	-4.6302E-1	7.3404E-3	0	0	0	0	A	E	Eq
7,33	SM	VR_SM06_SMPL2	12	0 to 29.6	mW/cm2-s-µ	-	-	-	-	VR23.6	-4.6302E-1	7.3404E-3	0	0	0	0	A	E	Eq
7,33	SM	VR_SM06_SMPL3	12	0 to 29.6	mW/cm2-s-µ	-	-	-	-	VR23.6	-4.6302E-1	7.3404E-3	0	0	0	0	A	E	Eq
7,33	SM	VR_SM07_SMPL1	12	0 to 23.0	mW/cm2-s-µ	-	-	-	-	VR23.7	-5.1367E-1	5.7526E-3	0	0	0	0	A	E	Eq
7,33	SM	VR_SM07_SMPL2	12	0 to 23.0	mW/cm2-s-µ	-	-	-	-	VR23.7	-5.1367E-1	5.7526E-3	0	0	0	0	A	E	Eq
7,33	SM	VR_SM07_SMPL3	12	0 to 23.0	mW/cm2-s-µ	-	-	-	-	VR23.7	-5.1367E-1	5.7526E-3	0	0	0	0	A	E	Eq
7,33	SM	VR_SM08_SMPL1	12	0 to 21.5	mW/cm2-s-µ	-	-	-	-	VR23.8	-5.1982E-1	5.3775E-3	0	0	0	0	A	E	Eq
7,33	SM	VR_SM08_SMPL2	12	0 to 21.5	mW/cm2-s-µ	-	-	-	-	VR23.8	-5.1982E-1	5.3775E-3	0	0	0	0	A	E	Eq
7,33	SM	VR_SM08_SMPL3	12	0 to 21.5	mW/cm2-s-µ	-	-	-	-	VR23.8	-5.1982E-1	5.3775E-3	0	0	0	0	A	E	Eq
7,33	SM	VR_SM09_SMPL1	12	0 to 19.9	mW/cm2-s-µ	-	-	-	-	VR23.9	-4.8203E-1	4.9865E-3	0	0	0	0	A	E	Eq
7,33	SM	VR_SM09_SMPL2	12	0 to 19.9	mW/cm2-s-µ	-	-	-	-	VR23.9	-4.8203E-1	4.9865E-3	0	0	0	0	A	E	Eq
7,33	SM	VR_SM09_SMPL3	12	0 to 19.9	mW/cm2-s-µ	-	-	-	-	VR23.9	-4.8203E-1	4.9865E-3	0	0	0	0	A	E	Eq
18	SR	IR_SR_10WLA_CURH	12	0 to 6.29	A	-	-	-	-	IR04a	-6.2918E+0	3.0723E-3	0	0	0	0	A	H	2.518A/V
18	SR	IR_SR_10WLA_CURR	12	0 to 6.29	A	-	-	-	-	IR04a	-6.2918E+0	3.0723E-3	0	0	0	0	A	E	2.518A/V
18	SR	IR_SR_10WLB_CURH	12	0 to 6.23	A	-	-	-	-	IR04b	-6.2367E+0	3.0454E-3	0	0	0	0	A	H	2.497A/V
18	SR	IR_SR_10WLB_CURR	12	0 to 6.23	A	-	-	-	-	IR04b	-6.2367E+0	3.0454E-3	0	0	0	0	A	E	2.497A/V
18	SR	IR_SR_1WLA_CURH	12	0 to 0.3	A	-	-	-	-	IR05a	-3.1335E-1	1.5308E-4	0	0	0	0	A	H	0.1252A/V
18	SR	IR_SR_1WLA_CURR	12	0 to 0.3	A	-	-	-	-	IR05a	-3.1335E-1	1.5308E-4	0	0	0	0	A	E	0.1252A/V
18	SR	IR_SR_1WLB_CURH	12	0 to 0.3	A	-	-	-	-	IR05b	-3.0780E-1	1.5000E-4	0	0	0	0	A	H	0.1232A/V
18	SR	IR_SR_1WLB_CURR	12	0 to 0.3	A	-	-	-	-	IR05b	-3.0780E-1	1.5000E-4	0	0	0	0	A	E	0.1232A/V
27,38L	SR	TA_SR_IR_SRC_A	12	-20 to120°C	°C	-	-	-	-	TA10p1	1.6800E+2	-1.3621E+0	7.3546E-3	-1.5646E-5	0	0	A	H/E	Teq
27,38L	SR	TA_SR_IR_SRC_A		TA10p1= 0 to 155 DN; TA10p2= 156 to 393 DN						TA10p2	1.2250E+2	-4.2640E-1	8.9321E-4	-7.8780E-7	0	0	A	H/E	Teq
27,38L	SR	TA_SR_IR_SRC_A		TA10p3= 394 to 4095 DN						TA10p3	8.4784E+1	-1.2829E-1	8.0553E-5	-2.5285E-8	0	0	A	H/E	Teq
27,38L	SR	TA_SR_IR_SRC_B	12	Same 3 Eq SF & limits as TA_SR_IR_SRC_A						TA10px	See TA_SR_IR_SRC_A 3-segment Eqs				0	0	A	H/E	Teq
27,38L	SR	TA_SR_SRC_A_SIPD	12	Same 3 Eq SF & limits as TA_SR_IR_SRC_A						TA10px	See TA_SR_IR_SRC_A 3-segment Eqs				0	0	A	H/E	Teq
27,38L	SR	TA_SR_SRC_B_SIPD	12	Same 3 Eq SF & limits as TA_SR_IR_SRC_A						TA10px	See TA_SR_IR_SRC_A 3-segment Eqs				0	0	A	H/E	Teq
29	SR	VR_SR_LAMPS	12	0 to 7	Vdc	-	-	-	-	VR24	-7.0000E+0	3.4180E-3	0	0	0	0	A	E	2.8V/V
29	SR	VR_SR_LAMPS_H	12	0 to 7	Vdc	-	-	-	-	VR24	-7.0000E+0	3.4180E-3	0	0	0	0	A	H	2.8V/V

TABLE 20-5. MODIS ACTIVE ANALOG TELEMETRY/ENGINEERING LIMITS & EQUATIONS

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• See bottom Notes. • Equations are 5th order polynomial form: EU = C0 + C1(DN) + C2(DN)^2 + C3(DN)^3 + C4(DN)^4 + C5(DN)^5.

pl chg#	1 Subsys	2 Telemetry Mnemonic Name	3 # of Bits	4 Approx Tlmy Range	5 Eng Units	6a Red Low	6b Yellow Low	6c Yellow High	6d Red High	7a Eq #	7b C0	7c C1	7d C2	7e C3	7f C4	7g C5	8 Type /Use	9 Use	10 Ref EU SF/Nom
											Telemetry DN to Eng Units Equation Coefficients								
11	SR	VR_SR_SELF_CAL1	12	-2.5 to 2.5	Vdc	-	-	-	-	VR23	-2.5000E+0	1.2207E-3	0	0	0	0	A	E	1V/V
11	SR	VR_SR_SELF_CAL2	12	-2.5 to 2.5	Vdc	-	-	-	-	VR23	-2.5000E+0	1.2207E-3	0	0	0	0	A	E	1V/V
11	SR	VR_SR_SELF_CAL3	12	-2.5 to 2.5	Vdc	-	-	-	-	VR23	-2.5000E+0	1.2207E-3	0	0	0	0	A	E	1V/V
11	SR	VR_SR_SPCT_NORM1	12	-2.5 to 2.5	Vdc	-	-	-	-	VR23	-2.5000E+0	1.2207E-3	0	0	0	0	A	E	1V/V
11	SR	VR_SR_SPCT_NORM2	12	-2.5 to 2.5	Vdc	-	-	-	-	VR23	-2.5000E+0	1.2207E-3	0	0	0	0	A	E	1V/V
11	SR	VR_SR_SPCT_NORM3	12	-2.5 to 2.5	Vdc	-	-	-	-	VR23	-2.5000E+0	1.2207E-3	0	0	0	0	A	E	1V/V
11	SR	VR_SR_SRC_A_RAD	12	-2.5 to 2.5	Vdc	-	-	-	-	VR23	-2.5000E+0	1.2207E-3	0	0	0	0	A	H	1V/V
11	SR	VR_SR_SRC_A_RADH	12	-2.5 to 2.5	Vdc	-	-	-	-	VR23	-2.5000E+0	1.2207E-3	0	0	0	0	A	E	1V/V
11	SR	VR_SR_SRC_B_RAD	12	-2.5 to 2.5	Vdc	-	-	-	-	VR23	-2.5000E+0	1.2207E-3	0	0	0	0	A	H	1V/V
11	SR	VR_SR_SRC_B_RADH	12	-2.5 to 2.5	Vdc	-	-	-	-	VR23	-2.5000E+0	1.2207E-3	0	0	0	0	A	E	1V/V
22	TC	VR_TC_CSCKT_PV	8	0 to 12.5	Vdc	8.50	9.00	11.80	12.50	VR20	-1.2500E+1	9.7656E-2	0	0	0	0	A	H	5V/V;10.8V
22	TC	VR_TC_ISCKT_PV	8	0 to 12.5	Vdc	8.50	9.00	11.80	12.50	VR20	-1.2500E+1	9.7656E-2	0	0	0	0	A	H	5V/V;10.8V
22,35,38	TC	VR_TC_LWCKT_NV	8	-12.5 to 0	Vdc	-12.50	-11.80	-9.80	-9.10	VR20	-1.2500E+1	9.7656E-2	0	0	0	0	A	H	5V/V;-10.8V
22,35,38	TC	VR_TC_LWCKT_PV	8	0 to 12.5	Vdc	9.10	9.80	11.80	12.50	VR20	-1.2500E+1	9.7656E-2	0	0	0	0	A	H	5V/V;10.8V
22	TC	VR_TC_OSCKT_PV	8	0 to 12.5	Vdc	8.50	9.00	11.80	12.50	VR20	-1.2500E+1	9.7656E-2	0	0	0	0	A	H	5V/V;10.8V
22,35,38	TC	VR_TC_SMCKT_NV	8	-12.5 to 0	Vdc	-12.50	-11.80	-9.80	-9.10	VR20	-1.2500E+1	9.7656E-2	0	0	0	0	A	H	5V/V; -10.8V
22	TC	VR_TC_SMCKT_PV	8	0 to 12.5	Vdc	9.10	9.80	11.80	12.50	VR20	-1.2500E+1	9.7656E-2	0	0	0	0	A	H	5V/V;10.8V
22,35,38	TC	VR_TC_VISCKT_NV	8	-12.5 to 0	Vdc	-12.50	-11.80	-9.80	-9.10	VR20	-1.2500E+1	9.7656E-2	0	0	0	0	A	H	5V/V;-10.8V
22	TC	VR_TC_VISCKT_PV	8	0 to 12.5	Vdc	9.10	9.80	11.80	12.50	VR20	-1.2500E+1	9.7656E-2	0	0	0	0	A	H	5V/V;10.8V
14,28	TM	VR_TM_REF_ACT1_1	12	0-2.5	V	0.96	0.98	1.02	1.04	VR22	-2.5000E+0	1.2207E-3	0	0	0	0	A	H	1V/V; 1.000V
14,28	TM	VR_TM_REF_ACT1_2	12	0-2.5	V	0.96	0.98	1.02	1.04	VR22	-2.5000E+0	1.2207E-3	0	0	0	0	A	H	1V/V; 1.000V
14,28	TM	VR_TM_REF_ACT1_3	12	0-2.5	V	0.96	0.98	1.02	1.04	VR22	-2.5000E+0	1.2207E-3	0	0	0	0	A	H	1V/V; 1.000V
14,28	TM	VR_TM_REF_ACT2_1	12	0-2.5	V	0.96	0.98	1.02	1.04	VR22	-2.5000E+0	1.2207E-3	0	0	0	0	A	H	1V/V; 1.000V
14,28	TM	VR_TM_REF_ACT2_2	12	0-2.5	V	0.96	0.98	1.02	1.04	VR22	-2.5000E+0	1.2207E-3	0	0	0	0	A	H	1V/V; 1.000V
14,19,28	TM	VR_TM_REF_ACT3_1	12	0-2.5	V	0.96	0.98	1.02	1.04	VR22	-2.5000E+0	1.2207E-3	0	0	0	0	A	H	1V/V; 1.000V
14,19,28	TM	VR_TM_REF_ACT4_1	12	0-2.5	V	0.96	0.98	1.02	1.04	VR22	-2.5000E+0	1.2207E-3	0	0	0	0	A	H	1V/V; 1.000V
14,28	TM	VR_TM_REF_ACT5_1	12	0-2.5	V	0.96	0.98	1.02	1.04	VR22	-2.5000E+0	1.2207E-3	0	0	0	0	A	H	1V/V; 1.000V
14,28	TM	VR_TM_REF_ACT5_2	12	0-2.5	V	0.96	0.98	1.02	1.04	VR22	-2.5000E+0	1.2207E-3	0	0	0	0	A	H	1V/V; 1.000V
14,28	TM	VR_TM_REF_ACT5_3	12	0-2.5	V	0.96	0.98	1.02	1.04	VR22	-2.5000E+0	1.2207E-3	0	0	0	0	A	H	1V/V; 1.000V
14,28	TM	VR_TM_REF_ACT6_1	12	0-2.5	V	0.96	0.98	1.02	1.04	VR22	-2.5000E+0	1.2207E-3	0	0	0	0	A	H	1V/V; 1.000V
1,14	TM	VR_TM_REF_ACT6_3	12	0-2.5	V	0.96	0.98	1.02	1.04	VR22	-2.5000E+0	1.2207E-3	0	0	0	0	A	H	1V/V; 1.000V
14,19,28	TM	VR_TM_REF_ACT7_1	12	0-2.5	V	0.96	0.98	1.02	1.04	VR22	-2.5000E+0	1.2207E-3	0	0	0	0	A	H	1V/V; 1.000V
5,14,28	TM	VR_TM_REF_ACTGND	12	-2.5 to2.5	V	-0.04	-0.02	0.02	0.40	VR22	-2.5000E+0	1.2207E-3	0	0	0	0	A	H	1V/V; 0.000V

TABLE 20-5. MODIS ACTIVE ANALOG TELEMETRY/ENGINEERING LIMITS & EQUATIONS

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• **See bottom Notes.** • **Equations are 5th order polynomial form: EU = C0 + C1(DN) + C2(DN)^2 + C3(DN)^3 + C4(DN)^4 + C5(DN)^5.**

pt chg#	1 Subsys	2 Telemetry Mnemonic Name	3 # of Bits	4 Approx Tlmy Range	5 Eng Units	6a Red Low	6b Yellow Low	6c Yellow High	6d Red High	7a Eq #	7b C0	7c C1	7d C2	7e C3	7f C4	7g C5	8 Type /Use	9 Use	10 Ref EU SF/Nom
											Telemetry DN to Eng Units Equation Coefficients								

Notes:

1. Table 20-5 provides engineering unit (EU) limits & equations for active analog telemetry items contained both in Table 20-2A housekeeping telemetry and Table 30-5C engineering data. Table 20-6 provides similar data for passive analog telemetry. Column 8 has Type/Use codes to relate the use. "Type" is as defined in Table 20-2A.

2. MODIS active analog telemetry is scaled to fit within the ±2.5V input range of the A/D conversion process. Many signals only use half the range of 0 to +2.5V, or -2.5V. The inverse process to recover EU values, first recovers the telemetry voltage (Vt) typically as Vt = 5(DN/256)-2.5, for 8-bit items, etc, then converts Vt to EU by multiplying by appropriate scale factors. So typically, EU = SF[Vt] = SF[5(DN/256)-2.5], for 8-bit items. For linear telemetry functions only the C0 and C1 terms of the general equation are used. For non-linear items, a curve fit process is used, which results in the use of the higher order terms of the general polynomial equation. All active analog functions are linear except temperature functions.

3. Column 6 limits are somewhat arbitrary in some cases. Also, a number of telemetry items are "just info" items without limits, that will ripple if other prime items go beyond their limits. By definition, the particular MODIS subsystem must be ON for valid telemetry.

4. Columns 7a through 7g relate telemetry equations. 7a Eq# is an equation ID number formulated with the leading 2 characters of the Mnemonic Name. Many signals use the same equations, but not necessarily the same limits.

5. Column 9 contain Mux ID's to identify the particular mux path shown in Figure 20-2. This in turn relates to the TM subsystem reference signals, that use the same mux for lifetime performance tracking.

6. For linear items, Column 10 provides scale factors, which are factors within the C0, C1 coefficients. Also, nominal values are shown for items with nearly constant operating points.

7. Shaded items in Columns 2 & 8 are pt-p items processed directly by the S/C BDU. (The SBRC GSE RTIU emulates the S/C B DU. Except the RTIU processes passive telemetry temperatures by resistance measurements versus normal D/A processing as done by the S/C BDU.)

8. TA_RC_LWIR_CFPA & TA_RC_SMIR_CFPA each have individual temperature equations according to the selected CFPA heater T1, T2, or T3 setpoint as indicated by Table 20-2A CR_RC_CFPA_T1SET and CR_RC_CFPA_T3SET.

PF Change History *Chg #s relate to table Chg #s except for [#s], which are general notes.*

1. 12/16/94 Corrected Col 6 limits on VR_PS2_N15_A2AF to be same as all other -15V forms. Also sorted table like most CTD are sorted - -Subsy, then Name.
2. 2/16/95 Chg SF on IR_BB_HTRA/B_CURRH from 0.5A/V to 0.578A/V.
3. 3/18/95 entered SF for NIR & VIS FPA's.
4. 3/24/95 PC & PV Eq's TA01 & TA02 to be based on 9-bits instead of 8. Also chged limits per R.Choo 3/20/95 markup.
5. 4/14/95 Chged IR_PS1_INPUT_CUR based on emperical comparison to PIC PS current meter. Divided present factor by 1.5795 then applied -0.12672 offset.
6. 5/16/95 Revise Eq on VR_SA_A_MTR_TORQ as Joe K said factor s/b 70in oz/volt instead of original 35in oz/volt.
7. 1/5/96 Add range, no-limits, equation to SM typical 27 places VR_SM_VR SM0x_SMPLx.
8. 12/3/95 Increase bits from 8 to 10 for VR_RC_LW_FPA_HTR & VR_RC_SM_FPA_HTR.
9. 5/3/96 Revise PS1/PS2 voltage limits.
10. 5/5/96 Add range, no-limits, equation to PC typical 60 places VR_PC_B31C01_DCR .

TABLE 20-5. MODIS ACTIVE ANALOG TELEMETRY/ENGINEERING LIMITS & EQUATIONS

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• See bottom Notes. • Equations are 5th order polynomial form: EU = C0 + C1(DN) + C2(DN)^2 + C3(DN)^3 + C4(DN)^4 + C5(DN)^5.

pf chg#	1 Subsys	2 Telemetry Mnemonic Name	3 # of Bits	4 Approx Tlmy Range	5 Eng Units	6a Red Low	6b Yellow Low	6c Yellow High	6d Red High	7a Eq #	7b C0	7c C1	7d C2	7e C3	7f C4	7g C5	8 Type /Use	9 Use	10 Ref EU SF/Nom
											Telemetry DN to Eng Units Equation Coefficients								

11. 5/6/96 Add range, no-limits, equation to SR typical 3 places VR_SR_SELF_CALx, 3 places VR_SR_SPCT_NORMx, & 4 places VR_SR_SRC_x_RAD,H.
12. 5/6/96 Revise limits, 4 places, on VR_CP_P5V, VR_CP_N5V, VR_CP_P11V & VR_CP_N11V.
13. 5/6/96 prior 8/13/95 T20-2A change to relation of VIS & NIR FPAs from WF subsys to AO subsys. New names are TA_AO_VIS_FPA & TA_AO_NIR_FPA.
14. 5/6/92 Revise range, limits & Eqs at 14 places for VR_TM_REF_ACTxxx. Although names start with VR, values are ΔDN from ideal. Initial ambient test values will be baseline to compare temperature environment and subsequent life values.

————————Chgs since 5/96 151840 Initial Release————————

15. 5/14/96 Limit chgs to SA subsys items.
16. 5/14/96 SF & limit chgs to SA subsys items.
17. 8/3/96 Alarm chgs to PV from KAS 7/23/96.
18. 8/13/96 SRCA 10W & 1W lamp current scale factors. No alarm limits.
19. 8/18/96 3 minor name corrections to match T20-2A names: VR_TM_REF_ACT3 to VR_TM_REF_ACT3_1, VR_TM_REF_ACT4 to VR_TM_REF_ACT4_1 and VR_TM_REF_ACT7 to VR_TM_REF_ACT7_1.
20. 8/24/96 revise VIS, NIR, SMIR & LWIR FPA temperature equations & limits to PF values.
21. 8/25/96 revise PC, PV, RC_CS, RC_CS_OG, RC_IS, RC_IS_OG & RC_OS_OG eqs & limits.
22. 8/25/96 revise limits on VR_TC_XXCKT_XV subsystem (prior SF Eqs ok).
23. 8/25/96 revise SFs on all VR_PC_B3XCXX_DCR for -2.5 to +2.5V instead of -3.3 to +3.3V. No limits listed.
24. 8/25/96 revise SF on CR_PVXX_S_DELAY,H.
25. 8/28/96 revise IR_PS1_INPUT_CURR & IR_PS2_INPUT_CURR SF Eqs.
26. 8/29/96 revise IR_BB_HTRA_CURH & IR_BB_HTRB_CURR SF Eqs & limits.
27. 9/2/956 defined SF Eqs for 4 SRCA TA_SR_Temps SiPd & IR Source Htrs. No limits defined.
28. 9/13/96 Cancel Chg#14 & return 14 VR_TM_REF_ACT_X words to voltage scale factor instead of delta DN. New limits.
29. 9/15/96 Add SF w/o limits to VR_SR_LAMPS,H.
30. 9/15/96 Revise limits on VR_PS1_P5.6V_D1 &VR_PS2_P5.6V_D1 to reflect chg in nominal 5.6V to 5.8V. Name remains same.
31. 9/15/96 Additional PV limit chgs after K.S. review of Chg#17 PV chgs.
32. 9/15/96 Deleted limits on VR_RC_LW_FPA_HTR & VR_RC_SM_FPA_HTR.
33. 9/16/96 Add individual SFs for 9 VR_SM0X_SMPLY SDSM detectors x 3 samples/each. No limits.
34. 9/21/96 Correction to VR_SA_B_RP11V & VR_SA_B_RN11V to have same SF as VR_SA_A_RP11V & VR_SA_A_RN11V. Also, make VR_SA_A_RP11V limits the same as VR_SA_B_RP11V limits.
35. 9/21/96 Revise 4 VR_TC_XXCKT_P/NV to have same SFs as other 5 ckts.
36. 9/30/96 Revised limits on 6 TA_PC_B#X_MUX & on 6 TA_PVXX_PWBX_Y.
37. 10/21/96 Correct names for VR_PS1_P5.6V_D1 & VR_PS2_P5.6V_D1 to be VR_PS1_P5_6V_D1 & VR_PS2_P5_6V_D1 to be consistent with OASIS convention.
38. 5/97 Multiple EO1122D Incorporations for Rev B. See EO1122D (released 970305) for details of bit increase for several words and name chg & spare chg.

38L. These items have either false don't care limits, or equation segments extended, to prevent OASIS from inserting default zero values, or, equation scale factor defaults to DN units.

39. 5/97 Direct Rev B revise SF's to match chg to increase bits from 8 to 12 and relocate to Maj Cyc 32: 1) IR_SA_A_ECDR_LED, 2) IR_SA_B_ECDR_LED, 3) VR_SA_A_ECDR_MON and VR_SA_B_ECDR_MON.
40. 5/97 Direct Rev B chg to increase Yellow & Red High Limits on VR_SA_A_MTR_TORQ & VR_SA_B_MTR_TORQ.

TABLE 20-6. MODIS PASSIVE ANALOG TELEMETRY/ENGINEERING LIMITS & EQUATIONS

• See bottom Notes. • Equations are 5th order polynomial form: EU = C0 + C1(DN) + C2(DN)^2 + C3(DN)^3 + C4(DN)^4 + C5(DN)^5. 5/97

pfm chg#	1 Subsys	2 Mnemonic Name	3 # of Bits	4 Tlmy Range	5 Units	6a Red Low	6b Yellow Low	6c Yellow High	6d Red High	7a Eq #	7b C0	7c C1	7d C2	7e C3	7f C4	7g C5	8 Type	9 Use	10 Ref EU SF/Nom
8	AO	TP_AO_LWIR_LENS	12	-23 to +85	°C	-	-	-	-	TP01p	8.6953E+1	-7.0286E-2	4.1191E-5	-1.6989E-8	3.6372E-12	-3.2037E-16	PT	H	Teq
8	AO	TP_AO_LWIR_OBJ	12	-23 to +85	°C	-	-	-	-	TP01p	8.6953E+1	-7.0286E-2	4.1191E-5	-1.6989E-8	3.6372E-12	-3.2037E-16	PT	H	Teq
8	AO	TP_AO_PX_NZ_CORN	12	-23 to +85	°C	-	-	-	-	TP01p	8.6953E+1	-7.0286E-2	4.1191E-5	-1.6989E-8	3.6372E-12	-3.2037E-16	PT	H	Teq
	AO	TP_AO_PZ_BY_RC	8	-50 to +78	°C	-25	-10	40	60	TP3AS3	1.5814E+4	-1.0498E+1	2.3287E-3	-1.7282E-7	0	0	PS	H	Teq
	AO	TP_AO_PZ_BY_RC	-	TP3AS3 = 4918-4383Ω; TP3AS2 = 4382-1306Ω-->						TP3AS2	9.9635E+1	-5.0770E-2	1.1950E-5	-1.4379E-9	0	0	PS	H	Teq
	AO	TP_AO_PZ_BY_RC	-	(5kΩTS//4.99kΩ) TP3AS1 = 1305 -558Ω-->						TP3AS1	1.2653E+2	-1.1382E-1	6.2135E-5	-1.5009E-8	0	0	PS	H	Teq
22	AO	TP_AO_PZ_BY_RC	8	-50 to +78	°C	-25	-10	40	60	TP3BS1	1.3459E+02	-2.7364E+00	3.4233E-02	-1.8161E-04	0	0	PS	H	Teq
22	AO	TP_AO_PZ_BY_RC	-	S/C BDU - TP3BS1 = 0-63DN; TP3BS2 = 64-217DN;						TP3BS2	9.9616E+01	-9.9126E-01	4.5569E-03	-1.0711E-05	0	0	PS	H	Teq
22	AO	TP_AO_PZ_BY_RC	-	TP3BS3 = 218-255DN						TP3BS3	1.4432E+04	-1.8780E+02	8.1667E-01	-1.1884E-03	0	0	PS	H	Teq
8	AO	TP_AO_SMIR_LENS	12	-23 to +85	°C	-	-	-	-	TP01p	8.6953E+1	-7.0286E-2	4.1191E-5	-1.6989E-8	3.6372E-12	-3.2037E-16	PT	H	Teq
8	AO	TP_AO_SMIR_OBJ	12	-23 to +85	°C	-	-	-	-	TP01p	8.6953E+1	-7.0286E-2	4.1191E-5	-1.6989E-8	3.6372E-12	-3.2037E-16	PT	H	Teq
8	AO	TP_AO_VNDICH_HSG	12	-23 to +85	°C	-	-	-	-	TP01p	8.6953E+1	-7.0286E-2	4.1191E-5	-1.6989E-8	3.6372E-12	-3.2037E-16	PT	H	Teq
1,12	BB	TP_BB_TEMP01H	12	270 to 320	K	-	-	-	-	TP07a2.1	3.2149E+02	-4.5613E-02	2.7031E-05	-8.2454E-09	0	0	PB	H,E	Teq
12	BB	TP_BB_TEMP01H		TP07a2.2= 1002 to 4095 DN; TP07a2.1= 0 to 1001 DN						TP07a2.2	3.1388E+02	-2.3756E-02	4.9645E-06	-4.4776E-10	0	0	PB	H,E	Teq
1,12	BB	TP_BB_TEMP02H	12	270 to 320	K	-	-	-	-	TP08a2.1	3.2096E+02	-4.5841E-02	2.7804E-05	-8.7430E-09	0	0	PB	H,E	Teq
12	BB	TP_BB_TEMP02H		TP08a2.2= 973 to 4095 DN; TP08a2.1= 0 to 972 DN						TP08a2.2	3.1360E+02	-2.4077E-02	5.1364E-06	-4.7341E-10	0	0	PB	H,E	Teq
1,12	BB	TP_BB_TEMP03H	12	270 to 320	K	-	-	-	-	TP09a2.1	3.2129E+02	-4.6095E-02	2.7752E-05	-8.6448E-09	0	0	PB	H,E	Teq
12	BB	TP_BB_TEMP03H		TP09a2.2= 981 to 4095 DN; TP09a2.1= 0 to 980 DN						TP09a2.2	3.1385E+02	-2.4235E-02	5.1631E-06	-4.7541E-10	0	0	PB	H,E	Teq
1,12	BB	TP_BB_TEMP04H	12	270 to 320	K	-	-	-	-	TP10a2.1	3.2119E+02	-4.5896E-02	2.7620E-05	-8.5990E-09	0	0	PB	H,E	Teq
12	BB	TP_BB_TEMP04H		TP010a2.2= 981 to 4095 DN; TP10a2.1= 0 to 980 DN						TP10a2.2	3.1377E+02	-2.4126E-02	5.1343E-06	-4.7207E-10	0	0	PB	H,E	Teq
1,12	BB	TP_BB_TEMP05H	12	270 to 320	K	-	-	-	-	TP11a2.1	3.2108E+02	-4.5833E-02	2.7647E-05	-8.6434E-09	0	0	PB	H,E	Teq
12	BB	TP_BB_TEMP05H		TP011a2.2= 977 to 4095 DN; TP11a2.1= 0 to 976 DN						TP11a2.2	3.1367E+02	-2.4061E-02	5.1122E-06	-4.6910E-10	0	0	PB	H,E	Teq
1,12	BB	TP_BB_TEMP06H	12	270 to 320	K	-	-	-	-	TP12a2.1	3.2096E+02	-4.5818E-02	2.7803E-05	-8.7576E-09	0	0	PB	H,E	Teq
12	BB	TP_BB_TEMP06H		TP012a2.2= 973 to 4095 DN; TP12a2.1= 0 to 972 DN						TP12a2.2	3.1360E+02	-2.4060E-02	5.1286E-06	-4.7219E-10	0	0	PB	H,E	Teq
12	BB	TP_BB_TEMP07H	12	270 to 320	K	-	-	-	-	TP13a2.1	3.2142E+02	-4.5588E-02	2.6953E-05	-8.2021E-09	0	0	PB	H,E	Teq
1,12	BB	TP_BB_TEMP07H		TP013a2.2= 997 to 4095 DN; TP13a2.1= 0 to 996 DN						TP13a2.2	3.1385E+02	-2.3845E-02	4.9990E-06	-4.5218E-10	0	0	PB	H,E	Teq
12	BB	TP_BB_TEMP08H	12	270 to 320	K	-	-	-	-	TP14a2.1	3.2130E+02	-4.5651E-02	2.7165E-05	-8.3387E-09	0	0	PB	H,E	Teq
1,12	BB	TP_BB_TEMP08H		TP014a2.2= 991 to 4095 DN; TP14a2.1= 0 to 990 DN						TP14a2.2	3.1380E+02	-2.3929E-02	5.0425E-06	-4.5851E-10	0	0	PB	H,E	Teq
12	BB	TP_BB_TEMP09H	12	270 to 320	K	-	-	-	-	TP15a2.1	3.2124E+02	-4.5710E-02	2.7401E-05	-8.4730E-09	0	0	PB	H,E	Teq
1,12	BB	TP_BB_TEMP09H		TP015a2.2= 990 to 4095 DN; TP15a2.1= 0 to 989 DN						TP15a2.2	3.1384E+02	-2.4014E-02	5.0844E-06	-4.6418E-10	0	0	PB	H,E	Teq
12	BB	TP_BB_TEMP10H	12	270 to 320	K	-	-	-	-	TP16a2.1	3.2098E+02	-4.5697E-02	2.7486E-05	-8.5568E-09	0	0	PB	H,E	Teq
1,12	BB	TP_BB_TEMP10H		TP016a2.2= 1066 to 4095 DN; TP16a2.1= 0 to 1065 DI						TP16a2.2	3.1267E+02	-2.2773E-02	4.5963E-06	-4.0376E-10	0	0	PB	H,E	Teq
12	BB	TP_BB_TEMP11H	12	270 to 320	K	-	-	-	-	TP17a2.1	3.2105E+02	-4.6757E-02	3.0349E-05	-1.0704E-08	0	0	PB	H,E	Teq
1,12	BB	TP_BB_TEMP11H		TP017a2.2= 881 to 4095 DN; TP17a2.1= 0 to 880 DN						TP17a2.2	3.1360E+02	-2.4084E-02	5.1284E-06	-4.7160E-10	0	0	PB	H,E	Teq
12	BB	TP_BB_TEMP12H	12	270 to 320	K	-	-	-	-	TP18a2.1	3.2126E+02	-4.5616E-02	2.7178E-05	-8.3546E-09	0	0	PB	H,E	Teq
1,12	BB	TP_BB_TEMP12H		TP018a2.2= 991 to 4095 DN; TP18a2.1= 0 to 990 DN						TP18a2.2	3.1378E+02	-2.3904E-02	5.0344E-06	-4.5731E-10	0	0	PB	H,E	Teq
12	BB	TP_BB_TEMP01H	12	270 to 320	K	-	-	-	-	TP07b2.1	3.2133E+02	-4.5591E-02	2.7155E-05	-8.3449E-09	0	0	PB	H,E	Teq

TABLE 20-6. MODIS PASSIVE ANALOG TELEMETRY/ENGINEERING LIMITS & EQUATIONS

• See bottom Notes. • Equations are 5th order polynomial form: EU = C0 + C1(DN) + C2(DN)^2 + C3(DN)^3 + C4(DN)^4 + C5(DN)^5. 5/97

pfm chg#	1 Subsys	2 Mnemonic Name	3 # of Bits	4 Tlmy Range	5 Units	6a Red Low	6b Yellow Low	6c Yellow High	6d Red High	7a Eq #	7b C0	7c C1	7d C2	7e C3	7f C4	7g C5	8 Type	9 Use	10 Ref EU SF/Norm
1,12	BB	TP_BB_TEMP01H		TP07b2.2= 996 to 4095 DN; TP07b2.1= 0 to 995 DN						TP07b2.2	3.1379E+02	-2.3798E-02	4.9918E-06	-4.5212E-10	0	0	PB	H,E	Teq
12	BB	TP_BB_TEMP02H	12	270 to 320	K	-	-	-	-	TP08b2.1	3.2079E+02	-4.5777E-02	2.7854E-05	-8.8060E-09	0	0	PB	H,E	Teq
1,12	BB	TP_BB_TEMP02H		TP08b2.2= 967 to 4095 DN; TP08b2.1= 0 to 966 DN						TP08b2.2	3.1351E+02	-2.4119E-02	5.1647E-06	-4.7801E-10	0	0	PB	H,E	Teq
12	BB	TP_BB_TEMP03H	12	270 to 320	K	-	-	-	-	TP09b2.1	3.2112E+02	-4.6036E-02	2.7820E-05	-8.7197E-09	0	0	PB	H,E	Teq
1,12	BB	TP_BB_TEMP03H		TP09b2.2= 974 to 4095 DN; TP09b2.1= 0 to 973 DN						TP09b2.2	3.1376E+02	-2.4283E-02	5.1947E-06	-4.8053E-10	0	0	PB	H,E	Teq
12	BB	TP_BB_TEMP04H	12	270 to 320	K	-	-	-	-	TP10b2.1	3.2103E+02	-4.5865E-02	2.7742E-05	-8.7042E-09	0	0	PB	H,E	Teq
1,12	BB	TP_BB_TEMP04H		TP010b2.2= 974 to 4095 DN; TP10b2.1= 0 to 973 DN						TP10b2.2	3.1368E+02	-2.4169E-02	5.1636E-06	-4.7683E-10	0	0	PB	H,E	Teq
12	BB	TP_BB_TEMP05H	12	270 to 320	K	-	-	-	-	TP11b2.1	3.2092E+02	-4.5816E-02	2.7797E-05	-8.7632E-09	0	0	PB	H,E	Teq
1,12	BB	TP_BB_TEMP05H		TP011b2.2= 970 to 4095 DN; TP11b2.1= 0 to 969 DN						TP11b2.2	3.1359E+02	-2.4112E-02	5.1443E-06	-4.7420E-10	0	0	PB	H,E	Teq
12	BB	TP_BB_TEMP06H	12	270 to 320	K	-	-	-	-	TP12b2.1	3.2080E+02	-4.5765E-02	2.7866E-05	-8.8247E-09	0	0	PB	H,E	Teq
1,12	BB	TP_BB_TEMP06H		TP012b2.2= 967 to 4095 DN; TP12b2.1= 0 to 966 DN						TP12b2.2	3.1351E+02	-2.4107E-02	5.1591E-06	-4.7709E-10	0	0	PB	H,E	Teq
12	BB	TP_BB_TEMP07H	12	270 to 320	K	-	-	-	-	TP13b2.1	3.2125E+02	-4.5568E-02	2.7084E-05	-8.3070E-09	0	0	PB	H,E	Teq
1,12	BB	TP_BB_TEMP07H		TP013b2.2= 1082 to 4095 DN; TP13b2.1= 0 to 1081 DI						TP13b2.2	3.1286E+02	-2.2699E-02	4.5486E-06	-3.9656E-10	0	0	PB	H,E	Teq
12	BB	TP_BB_TEMP08H	12	270 to 320	K	-	-	-	-	TP14b2.1	3.2114E+02	-4.5607E-02	2.7232E-05	-8.4057E-09	0	0	PB	H,E	Teq
1,12	BB	TP_BB_TEMP08H		TP014b2.2= 1075 to 4095 DN; TP14b2.1= 0 to 1074 DI						TP14b2.2	3.1279E+02	-2.2753E-02	4.5780E-06	-4.0083E-10	0	0	PB	H,E	Teq
12	BB	TP_BB_TEMP09H	12	270 to 320	K	-	-	-	-	TP15b2.1	3.2107E+02	-4.5675E-02	2.7509E-05	-8.5678E-09	0	0	PB	H,E	Teq
1,12	BB	TP_BB_TEMP09H		TP015b2.2= 1074 to 4095 DN; TP15b2.1= 0 to 1073 DI						TP15b2.2	3.1275E+02	-2.2731E-02	4.5758E-06	-4.0091E-10	0	0	PB	H,E	Teq
12	BB	TP_BB_TEMP10H	12	270 to 320	K	-	-	-	-	TP16b2.1	3.2082E+2	-4.5661E-2	2.7587E-5	-8.6468E-9	0	0	PB	H,E	Teq
1,12	BB	TP_BB_TEMP10H		TP016b2.2= 1059 to 4095 DN; TP16b2.1= 0 to 1058 DI						TP16b2.2	3.1259E+2	-2.2821E-2	4.6251E-6	-4.0818E-10	0	0	PB	H,E	Teq
12	BB	TP_BB_TEMP11H	12	270 to 320	K	-	-	-	-	TP17b2.1	3.2081E+2	-4.5732E-2	2.7666E-5	-8.6937E-9	0	0	PB	H,E	Teq
1,12	BB	TP_BB_TEMP11H		TP017b2.2= 1056 to 4095 DN; TP17b2.1= 0 to 1055 DI						TP17b2.2	3.1260E+2	-2.2909E-2	4.6568E-6	-4.1218E-10	0	0	PB	H,E	Teq
12	BB	TP_BB_TEMP12H	12	270 to 320	K	-	-	-	-	TP18b2.1	3.2110E+02	-4.5609E-02	2.7336E-05	-8.4727E-09	0	0	PB	H,E	Teq
1,12	BB	TP_BB_TEMP12H		TP018b2.2= 1075 to 4095 DN; TP18b2.1= 0 to 1074 DI						TP18b2.2	3.1276E+02	-2.2710E-02	4.5621E-06	-3.9863E-10	0	0	PB	H,E	Teq
(2),9,22L	CE	TP_CE_CAL2	9	-23 to +85	°C	-15	-14	80	85	TP02p	8.6954E+01	-5.6241E-01	2.6375E-03	-8.7030E-06	1.4904E-08	-1.0501E-11	PT	H	Teq
9,22L	CP	TP_CP_A_1553	9	-23 to +85	°C	-15	-14	80	85	TP02p	8.6954E+01	-5.6241E-01	2.6375E-03	-8.7030E-06	1.4904E-08	-1.0501E-11	PT	H	Teq
9,22L	CP	TP_CP_B_1553	9	-23 to +85	°C	-15	-14	80	85	TP02p	8.6954E+01	-5.6241E-01	2.6375E-03	-8.7030E-06	1.4904E-08	-1.0501E-11	PT	H	Teq
9,18	DR	TP_DR_NAD	9	-57 to +85	°C	-	-	-	-	TP06p1	8.7909E+01	-5.8636E-01	2.4209E-03	-4.7463E-06	0	0	PT	H	Teq
9,18	DR	TP_DR_NAD	9	TP06p1=0 to 222 DN; TP06p2=223 to 485 DN						TP06p2	1.3169E+02	-8.7223E-01	2.3562E-03	-2.5618E-06	0	0	PT	H	Teq
9,18	DR	TP_DR_NAD	9	TP06p3=486 to 512 DN						TP06p3	1.2702E+05	-7.7642E+02	1.5828E+00	-1.0764E-03	0	0	PT	H	Teq
5,10	DR	TP_DR_NAD_FS	9	-35 to +110	°C	-	-	-	-	TP04ps2	1.6149E+02	-1.0711E+00	2.5257E-03	-2.3161E-06	0	0	PT	H	Teq
5,10	DR	TP_DR_NAD_FS	9	TP04ps2 = 512 to 155 DN; TP04ps1 = 154 to 117 DN						TP04ps1	4.3952E+03	-8.7796E+01	5.9743E-01	-1.3673E-03	0	0	PT	H	Teq
9,18	DR	TP_DR_SDD	9	-57 to +85	°C	-	-	-	-	TP06p1	8.7909E+01	-5.8636E-01	2.4209E-03	-4.7463E-06	0	0	PT	H	Teq
9,18	DR	TP_DR_SDD	9	TP06p1=0 to 222 DN; TP06p2=223 to 485 DN						TP06p2	1.3169E+02	-8.7223E-01	2.3562E-03	-2.5618E-06	0	0	PT	H	Teq
9,18	DR	TP_DR_SDD	9	TP06p3=486 to 512 DN						TP06p3	1.2702E+05	-7.7642E+02	1.5828E+00	-1.0764E-03	0	0	PT	H	Teq
11	DR	TP_DR_SVD	9	-200 to +140	°C	-	-	-	-	TP05p	-2.1161E+02	6.4543E-01	9.8391E-05	0	0	0	PP	H	Teq
5,10	DR	TP_DR_SVD_FS	9	-35 to +110	°C	-	-	-	-	TP04ps2	1.6149E+02	-1.0711E+00	2.5257E-03	-2.3161E-06	0	0	PT	H	Teq
5,10	DR	TP_DR_SVD_FS	9	TP04ps2 = 512 to 155 DN; TP04ps1 = 154 to 117 DN						TP04ps1	4.3952E+03	-8.7796E+01	5.9743E-01	-1.3673E-03	0	0	PT	H	Teq

TABLE 20-6. MODIS PASSIVE ANALOG TELEMETRY/ENGINEERING LIMITS & EQUATIONS

• See bottom Notes. • Equations are 5th order polynomial form: EU = C0 + C1(DN) + C2(DN)^2 + C3(DN)^3 + C4(DN)^4 + C5(DN)^5. 5/97

pfm chg#	1 Subsys	2 Mnemonic Name	3 # of Bits	4 Tlmy Range	5 Units	6a Red Low	6b Yellow Low	6c Yellow High	6d Red High	7a Eq #	7b C0	7c C1	7d C2	7e C3	7f C4	7g C5	8 Type	9 Use	10 Ref EU SF/Nom
9,22L	FR	TP_FR_A_ENGINE	9	-23 to +85	°C	-15	-14	80	85	TP02p	8.6954E+01	-5.6241E-01	2.6375E-03	-8.7030E-06	1.4904E-08	-1.0501E-11	PT	H	Teq
9,22L	FR	TP_FR_B_ENGINE	9	-23 to +85	°C	-15	-14	80	85	TP02p	8.6954E+01	-5.6241E-01	2.6375E-03	-8.7030E-06	1.4904E-08	-1.0501E-11	PT	H	Teq
9	ME	TP_ME_CHAS_TOP	9	-23 to +85	°C	-	-	-	-	TP02p	8.6954E+01	-5.6241E-01	2.6375E-03	-8.7030E-06	1.4904E-08	-1.0501E-11	PT	H	Teq
	ME	TP_ME_NX_HTSINK	8	-50 to +78	°C	-30	-10	50	55	TP3AS3	1.5814E+4	-1.0498E+1	2.3287E-3	-1.7282E-7	0	0	PS	H	Teq
	ME	TP_ME_NX_HTSINK	8	TP3AS3 = 4918-4383Ω; TP3AS2 = 4382-1306Ω-->						TP3AS2	9.9635E+1	-5.0770E-2	1.1950E-5	-1.4379E-9	0	0	PS	H	Teq
	ME	TP_ME_NX_HTSINK	8	(5kΩTS//4.99kΩ) TP3AS1 = 1305 -558Ω-->						TP3AS1	1.2653E+2	-1.1382E-1	6.2135E-5	-1.5009E-8	0	0	PS	H	Teq
22	ME	TP_ME_NX_HTSINK	8	-50 to +78	°C	-30	-10	50	55	TP3BSX	S/C same 3-segment equations as TP_AO_PZ_BY_RC.				0	0	PS	H	Teq
	ME	TP_ME_PSRADIATOR	8	-50 to +78	°C	-25	-5	40	50	TP3AS3	1.5814E+4	-1.0498E+1	2.3287E-3	-1.7282E-7	0	0	PS	H	Teq
	ME	TP_ME_PSRADIATOR	8	TP3AS3 = 4918-4383Ω; TP3AS2 = 4382-1306Ω-->						TP3AS2	9.9635E+1	-5.0770E-2	1.1950E-5	-1.4379E-9	0	0	PS	H	Teq
	ME	TP_ME_PSRADIATOR	8	(5kΩTS//4.99kΩ) TP3AS1 = 1305 -558Ω-->						TP3AS1	1.2653E+2	-1.1382E-1	6.2135E-5	-1.5009E-8	0	0	PS	H	Teq
22	ME	TP_ME_PSRADIATOR	8	-50 to +78	°C	-25	-5	40	50	TP3BSX	S/C same 3-segment equations as TP_AO_PZ_BY_RC.				0	0	PS	H	Teq
19	MF	TP_MF_OB_BLKHD	8	-50 to +78	°C	-25	-10	40	60	TP3AS3	1.5814E+4	-1.0498E+1	2.3287E-3	-1.7282E-7	0	0	PS	H	Teq
19	MF	TP_MF_OB_BLKHD	8	TP3AS3 = 4918-4383Ω; TP3AS2 = 4382-1306Ω-->						TP3AS2	9.9635E+1	-5.0770E-2	1.1950E-5	-1.4379E-9	0	0	PS	H	Teq
19	MF	TP_MF_OB_BLKHD	8	(5kΩTS//4.99kΩ) TP3AS1 = 1305 -558Ω-->						TP3AS1	1.2653E+2	-1.1382E-1	6.2135E-5	-1.5009E-8	0	0	PS	H	Teq
19,22	MF	TP_MF_OB_BLKHD	8	-50 to +78	°C	-25	-10	40	60	TP3BSX	S/C same 3-segment equations as TP_AO_PZ_BY_RC.				0	0	PS	H	Teq
9,19	MF	TP_MF_NX_AOBKHD	9	-23 to +85	°C	-	-	-	-	TP02p	8.6954E+01	-5.6241E-01	2.6375E-03	-8.7030E-06	1.4904E-08	-1.0501E-11	PT	H	Teq
9,19	MF	TP_MF_PX_AOBKHD	9	-23 to +85	°C	-	-	-	-	TP02p	8.6954E+01	-5.6241E-01	2.6375E-03	-8.7030E-06	1.4904E-08	-1.0501E-11	PT	H	Teq
9,21	MF	TP_MF_Z_BKHD_BB	9	-23 to +85	°C	-	-	-	-	TP02p	8.6954E+01	-5.6241E-01	2.6375E-03	-8.7030E-06	1.4904E-08	-1.0501E-11	PT	H	Teq
9	MF	TP_MF_CALBKHD_SR	9	-23 to +85	°C	-	-	-	-	TP02p	8.6954E+01	-5.6241E-01	2.6375E-03	-8.7030E-06	1.4904E-08	-1.0501E-11	PT	H	Teq
9,21	MF	TP_MF_YZ_CALBKHD	9	-23 to +85	°C	-	-	-	-	TP02p	8.6954E+01	-5.6241E-01	2.6375E-03	-8.7030E-06	1.4904E-08	-1.0501E-11	PT	H	Teq
9	MF	TP_MF_CVR_OP_SR	9	-23 to +85	°C	-	-	-	-	TP02p	8.6954E+01	-5.6241E-01	2.6375E-03	-8.7030E-06	1.4904E-08	-1.0501E-11	PT	H	Teq
9	MF	TP_MF_NAD_APT_NX	9	-23 to +85	°C	-	-	-	-	TP02p	8.6954E+01	-5.6241E-01	2.6375E-03	-8.7030E-06	1.4904E-08	-1.0501E-11	PT	H	Teq
9	MF	TP_MF_NAD_APT_NY	9	-23 to +85	°C	-	-	-	-	TP02p	8.6954E+01	-5.6241E-01	2.6375E-03	-8.7030E-06	1.4904E-08	-1.0501E-11	PT	H	Teq
9	MF	TP_MF_SV_PORT	9	-23 to +85	°C	-	-	-	-	TP02p	8.6954E+01	-5.6241E-01	2.6375E-03	-8.7030E-06	1.4904E-08	-1.0501E-11	PT	H	Teq
	MF	TP_MF_TOP_BY_KM1	8	-50 to +78	°C	-25	-10	40	60	TP3AS3	1.5814E+4	-1.0498E+1	2.3287E-3	-1.7282E-7	0	0	PS	H	Teq
	MF	TP_MF_TOP_BY_KM1	8	TP3AS3 = 4918-4383Ω; TP3AS2 = 4382-1306Ω-->						TP3AS2	9.9635E+1	-5.0770E-2	1.1950E-5	-1.4379E-9	0	0	PS	H	Teq
	MF	TP_MF_TOP_BY_KM1	8	(5kΩTS//4.99kΩ) TP3AS1 = 1305 -558Ω-->						TP3AS1	1.2653E+2	-1.1382E-1	6.2135E-5	-1.5009E-8	0	0	PS	H	Teq
22	MF	TP_MF_TOP_BY_KM1	8	-50 to +78	°C	-25	-10	40	60	TP3BSX	S/C same 3-segment equations as TP_AO_PZ_BY_RC.				0	0	PS	H	Teq
9	MF	TP_MF_TOP_BY_KM2	9	-23 to +85	°C	-	-	-	-	TP02p	8.6954E+01	-5.6241E-01	2.6375E-03	-8.7030E-06	1.4904E-08	-1.0501E-11	PT	H	Teq
	MF	TP_MF_TOP_BY_KM3	8	-50 to +78	°C	-25	-10	40	60	TP3AS3	1.5814E+4	-1.0498E+1	2.3287E-3	-1.7282E-7	0	0	PS	H	Teq
	MF	TP_MF_TOP_BY_KM3	8	TP3AS3 = 4918-4383Ω; TP3AS2 = 4382-1306Ω-->						TP3AS2	9.9635E+1	-5.0770E-2	1.1950E-5	-1.4379E-9	0	0	PS	H	Teq
	MF	TP_MF_TOP_BY_KM3	8	(5kΩTS//4.99kΩ) TP3AS1 = 1305 -558Ω-->						TP3AS1	1.2653E+2	-1.1382E-1	6.2135E-5	-1.5009E-8	0	0	PS	H	Teq
22	MF	TP_MF_TOP_BY_KM3	8	-50 to +78	°C	-25	-10	40	60	TP3BSX	S/C same 3-segment equations as TP_AO_PZ_BY_RC.				0	0	PS	H	Teq
	PC	TP_PCFAM_RADIATR	8	-50 to +78	°C	-25	-10	50	60	TP3AS3	1.5814E+4	-1.0498E+1	2.3287E-3	-1.7282E-7	0	0	PS	H	Teq
	PC	TP_PCFAM_RADIATR	8	TP3AS3 = 4918-4383Ω; TP3AS2 = 4382-1306Ω-->						TP3AS2	9.9635E+1	-5.0770E-2	1.1950E-5	-1.4379E-9	0	0	PS	H	Teq
	PC	TP_PCFAM_RADIATR	8	(5kΩTS//4.99kΩ) TP3AS1 = 1305 -558Ω-->						TP3AS1	1.2653E+2	-1.1382E-1	6.2135E-5	-1.5009E-8	0	0	PS	H	Teq
22	PC	TP_PCFAM_RADIATR	8	-50 to +78	°C	-25	-10	50	60	TP3BSX	S/C same 3-segment equations as TP_AO_PZ_BY_RC.				0	0	PS	H	Teq

TABLE 20-6. MODIS PASSIVE ANALOG TELEMETRY/ENGINEERING LIMITS & EQUATIONS

• See bottom Notes. • Equations are 5th order polynomial form: EU = C0 + C1(DN) + C2(DN)^2 + C3(DN)^3 + C4(DN)^4 + C5(DN)^5. 5/97

1	2		3	4	5	6a	6b	6c	6d	7a	7b	7c	7d	7e	7f	7g	8	9	10
pfm chg#	Subsys	Mnemonic Name	# of Bits	Tlmy Range	Units	Red Low	Yellow Low	Yellow High	Red High	Eq #	C0	C1	C2	C3	C4	C5	Type	Use	Ref EU SF/Nom
9,22L	PC	TP_PC_CLAM_MNT	9	-23 to +85	°C	-9	-8	65	75	TP02p	8.6954E+01	-5.6241E-01	2.6375E-03	-8.7030E-06	1.4904E-08	-1.0501E-11	PT	H	Teq
9,15,22L	PS	TP_PS1_CVTR_SW	9	-23 to +85	°C	-15	-14	64	73	TP02p	8.6954E+01	-5.6241E-01	2.6375E-03	-8.7030E-06	1.4904E-08	-1.0501E-11	PT	H	Teq
9,15,22L	PS	TP_PS1_DIODE_OUT	9	-23 to +85	°C	-15	-14	64	73	TP02p	8.6954E+01	-5.6241E-01	2.6375E-03	-8.7030E-06	1.4904E-08	-1.0501E-11	PT	H	Teq
9	PS	TP_PS1_DWNREG_SW	9	-23 to +85	°C	-	-	-	-	TP02p	8.6954E+01	-5.6241E-01	2.6375E-03	-8.7030E-06	1.4904E-08	-1.0501E-11	PT	H	Teq
9	PS	TP_PS1_PRELOAD	9	-23 to +85	°C	-	-	-	-	TP02p	8.6954E+01	-5.6241E-01	2.6375E-03	-8.7030E-06	1.4904E-08	-1.0501E-11	PT	H	Teq
9,15,22L	PS	TP_PS2_CVTR_SW	9	-23 to +85	°C	-15	-14	64	73	TP02p	8.6954E+01	-5.6241E-01	2.6375E-03	-8.7030E-06	1.4904E-08	-1.0501E-11	PT	H	Teq
9,15,22L	PS	TP_PS2_DIODE_OUT	9	-23 to +85	°C	-15	-14	64	73	TP02p	8.6954E+01	-5.6241E-01	2.6375E-03	-8.7030E-06	1.4904E-08	-1.0501E-11	PT	H	Teq
9	PS	TP_PS2_DWNREG_SW	9	-23 to +85	°C	-	-	-	-	TP02p	8.6954E+01	-5.6241E-01	2.6375E-03	-8.7030E-06	1.4904E-08	-1.0501E-11	PT	H	Teq
9	PS	TP_PS2_PRELOAD	9	-23 to +85	°C	-	-	-	-	TP02p	8.6954E+01	-5.6241E-01	2.6375E-03	-8.7030E-06	1.4904E-08	-1.0501E-11	PT	H	Teq
	PV	TP_PVSAM_RADIATR	8	-50 to +78	°C	-25	-10	50	60	TP3AS3	1.5814E+4	-1.0498E+1	2.3287E-3	-1.7282E-7	0	0	PS	H	Teq
	PV	TP_PVSAM_RADIATR	-	TP3AS3 = 4918-4383Ω; TP3AS2 = 4382-1306Ω-->						TP3AS2	9.9635E+1	-5.0770E-2	1.1950E-5	-1.4379E-9	0	0	PS	H	Teq
	PV	TP_PVSAM_RADIATR	-	(5kΩTS//4.99kΩ) TP3AS1 = 1305 -558Ω-->						TP3AS1	1.2653E+2	-1.1382E-1	6.2135E-5	-1.5009E-8	0	0	PS	H	Teq
22	PV	TP_PVSAM_RADIATR	8	-50 to +78	°C	-25	-10	50	60	TP3BSX	S/C same 3-segment equations as TP_AO_PZ_BY_RC.				0	0	PS	H	Teq
(3,6),8	RC	TP_RC_MNT_RING	12	-23 to +85	°C	-	-	-	-	TP01p	8.6953E+1	-7.0286E-2	4.1191E-5	-1.6989E-8	3.6372E-12	-3.2037E-16	PT	H	Teq
9,22L	SA	TP_SA_A_MTR	9	-23 to +85	°C	-15	-14	45	60	TP02p	8.6954E+01	-5.6241E-01	2.6375E-03	-8.7030E-06	1.4904E-08	-1.0501E-11	PT	H	Teq
8	SA	TP_SA_RCT1_MIR	12	-23 to +85	°C	-	-	-	-	TP01p	8.6953E+1	-7.0286E-2	4.1191E-5	-1.6989E-8	3.6372E-12	-3.2037E-16	PT	H	Teq
(6),8	SA	TP_SA_RCT2_MIR	12	-23 to +85	°C	-	-	-	-	TP01p	8.6953E+1	-7.0286E-2	4.1191E-5	-1.6989E-8	3.6372E-12	-3.2037E-16	PT	H	Teq
9	SM	TP_SM_DET_AMP3	9	-23 to +85	°C	-	-	-	-	TP02p	8.6954E+01	-5.6241E-01	2.6375E-03	-8.7030E-06	1.4904E-08	-1.0501E-11	PT	H	Teq
9	SR	TP_SR_GRAT_ELEX	9	-23 to +85	°C	-	-	-	-	TP02p	8.6954E+01	-5.6241E-01	2.6375E-03	-8.7030E-06	1.4904E-08	-1.0501E-11	PT	H	Teq
9	SR	TP_SR_GRAT_MOTOR	9	-23 to +85	°C	-	-	-	-	TP02p	8.6954E+01	-5.6241E-01	2.6375E-03	-8.7030E-06	1.4904E-08	-1.0501E-11	PT	H	Teq
13,22	SR	TP_SR_LAMP_RING	9	-23 to +110	°C	-9	-8	90	95	TP02aps2	9.4990E+01	-4.7071E-01	1.0437E-03	-1.1288E-06	0	0	PT	H	Teq
13	SR	TP_SR_LAMP_RING	9	TP02aps2= 95 to 512 DN; TP02aps1= 21 to 94 DN						TP02aps1	1.4804E+02	-2.2403E+00	2.2177E-02	-8.9202E-05	0	0	PT	H	Teq
9	SR	TP_SR_MIR2_DET	9	-23 to +85	°C	-	-	-	-	TP02p	8.6954E+01	-5.6241E-01	2.6375E-03	-8.7030E-06	1.4904E-08	-1.0501E-11	PT	H	Teq
9	SR	TP_SR_MONO_CHAS1	9	-23 to +85	°C	-	-	-	-	TP02p	8.6954E+01	-5.6241E-01	2.6375E-03	-8.7030E-06	1.4904E-08	-1.0501E-11	PT	H	Teq
9	SR	TP_SR_MONO_CHAS2	9	-23 to +85	°C	-	-	-	-	TP02p	8.6954E+01	-5.6241E-01	2.6375E-03	-8.7030E-06	1.4904E-08	-1.0501E-11	PT	H	Teq
9	SR	TP_SR_SNOUT	9	-23 to +85	°C	-	-	-	-	TP02p	8.6954E+01	-5.6241E-01	2.6375E-03	-8.7030E-06	1.4904E-08	-1.0501E-11	PT	H	Teq
9	TE	TP_TE_FOLD_MIR	9	-23 to +85	°C	-	-	-	-	TP02p	8.6954E+01	-5.6241E-01	2.6375E-03	-8.7030E-06	1.4904E-08	-1.0501E-11	PT	H	Teq
9	TE	TP_TE_PRI_MIR	9	-23 to +85	°C	-	-	-	-	TP02p	8.6954E+01	-5.6241E-01	2.6375E-03	-8.7030E-06	1.4904E-08	-1.0501E-11	PT	H	Teq
9	TE	TP_TE_SEC_MIR	9	-23 to +85	°C	-	-	-	-	TP02p	8.6954E+01	-5.6241E-01	2.6375E-03	-8.7030E-06	1.4904E-08	-1.0501E-11	PT	H	Teq
9,22L	TM	TP_TM_ANLG_CKT	9	-23 to +85	°C	-15	-14	80	85	TP02p	8.6954E+01	-5.6241E-01	2.6375E-03	-8.7030E-06	1.4904E-08	-1.0501E-11	PT	H	Teq
14	TM	VR_TM_REF_BB_1	12	94	DN	-	-	-	-	na	na	na	na	na	na	na	PB	H	raw DN
14	TM	VR_TM_REF_BB_2	12	680	DN	-	-	-	-	na	na	na	na	na	na	na	PB	H	raw DN
14	TM	VR_TM_REF_BB_3	12	3226	DN	-	-	-	-	na	na	na	na	na	na	na	PB	H	raw DN
4,14	TM	VR_TM_REF_PRT1	12	2502	DN	-	-	-	-	na	na	na	na	na	na	na	PP	H	raw DN
4,14	TM	VR_TM_REF_PRT2	12	1072	DN	-	-	-	-	na	na	na	na	na	na	na	PP	H	raw DN
14	TM	VR_TM_REF_PSV1	12	1311	DN	-	-	-	-	na	na	na	na	na	na	na	PT	H	raw DN
14	TM	VR_TM_REF_PSV2	12	1311	DN	-	-	-	-	na	na	na	na	na	na	na	PT	H	raw DN

TABLE 20-6. MODIS PASSIVE ANALOG TELEMETRY/ENGINEERING LIMITS & EQUATIONS

• See bottom Notes. • Equations are 5th order polynomial form: EU = C0 + C1(DN) + C2(DN)^2 + C3(DN)^3 + C4(DN)^4 + C5(DN)^5. 5/97

pfm chg#	1 Subsys	2 Mnemonic Name	3 # of Bits	4 Tlmy Range	5 Units	6a Red Low	6b Yellow Low	6c Yellow High	6d Red High	7a Eq #	7b C0	7c C1	7d C2	7e C3	7f C4	7g C5	8 Type	9 Use	10 Ref EU SF/Nom
14	TM	VR_TM_REF_PSV3	12	1311	DN	-	-	-	-	na	na	na	na	na	na	na	PT	H	raw DN
14	TM	VR_TM_REF_PSV4	12	1311	DN	-	-	-	-	na	na	na	na	na	na	na	PT	H	raw DN
14	TM	VR_TM_REF_PSV5	12	1311	DN	-	-	-	-	na	na	na	na	na	na	na	PT	H	raw DN
4,14	TM	VR_TM_REF_PSV6	12	65	DN	-	-	-	-	na	na	na	na	na	na	na	PT	H	raw DN
4,14	TM	VR_TM_REF_PSV7	12	65	DN	-	-	-	-	na	na	na	na	na	na	na	PT	H	raw DN
4,14	TM	VR_TM_REF_PSV8	12	65	DN	-	-	-	-	na	na	na	na	na	na	na	PT	H	raw DN

Notes:

1. Table 20-6 provides engineering unit (EU) limits & equations for passive analog telemetry items contained both in Table 20-2A housekeeping telemetry and Table 30-5D engineering data. Table 20-5 provides similar data for active analog telemetry. Column 8 has Type/Use codes to relate the use. "Type" is as defined in Table 20-2A.

2. All MODIS passive analog telemetry points represent temperature items. The Column 3 bit count is 8, 9, and 12.

3. Column 6 limits are somewhat arbitrary in some cases. Also, a number of telemetry items are "just info" items without limits, that will ripple if other prime items go beyond their limits. MODIS must be ON in order for the CP analog telemetry board to process the listed signals (except for the S/C pt-pt items).

4. Columns 7a through 7g relate telemetry equations. Column 7a Eq# is an equation ID number formulated with the leading 2 characters of the Mnemonic Name. Many signals use the same equations, but not necessarily the same limits. Only the 12 BB temperatures are based on precision calibrated data. The remaining temperatures are based on circuit excitation and A/D conversion with thermistors per GSFC S-311-P-18 or a 405881 PRT.

Note BB temperature equations have unique sets for CPA or CPB. For GSE using OASIS SW, manual GSE A/B selections will follow command selection of CPA or CPB.

5. Column 9 contain Mux ID's to identify the particular mux path shown in Figure 20-2. This in turn relates to the TM subsystem reference signals, that use the same mux for lifetime performance tracking.

6. Boldly bordered groups in Columns 2 and 7a indicate items that use segmented equations. GSE generally needs explicit segment limit ID's to implement switching logic between segments.

7. Shaded items in Columns 2 & 8 are pt-pt items processed directly by the S/C BDU. The SBRC GSE RTIU emulates the S/C BDU. Except the RTIU processes passive telemetry temperatures by resistance measurements versus normal D/A processing as done by the S/C BDU. The S/C set of equations are the ones that have the Eq# as TP#BSX.

TABLE 20-6. MODIS PASSIVE ANALOG TELEMETRY/ENGINEERING LIMITS & EQUATIONS

• See bottom Notes. • Equations are 5th order polynomial form: EU = C0 + C1(DN) + C2(DN)^2 + C3(DN)^3 + C4(DN)^4 + C5(DN)^5. 5/97

pfm chg#	1 2 Subsys Mnemonic Name	3 # of Bits	4 Tlmy Range	5 Units	6a Red Low	6b Yellow Low	6c Yellow High	6d Red High	7a Eq #	7b C0	7c C1	7d C2	7e C3	7f C4	7g C5	8 Type	9 Use	10 Ref EU SF/Nom

T20-6 PF Change History *Chg #s relate to table Chg #s except for [#s], which are general notes.*

1. 11/4/96 Chg range on TP_BB_TEMP03H-12H to 270K to 320K, from 273K to 320K. Chged end limits to Nornal

[2] 11/4/96 Delete TP_BB_TEMP_AVG. Nev er implemented in T20-2 tlmyh list or T20-4 tlmy frame.

[3] 10/7/96 Delete TP_RC_OS_WH. Late Chg History note 11/5.

4. 11/5/96 Revise/add VR_TM_REF's: 1) moved REF_GND to T20-5, 2) revise PRT to PRT1, add 3) PRT2, 4) PSV6, 5) PSV7 & 6) create PSV8 from TP_SA_B_MTR.
5. 11/27/96 Chg names on TP_DR_MTRs 1) to TP_DR_NAD_FS from TP_DR_NAD_MTR, 2) to TP_DR_SVD_FS from TP_DR_SVD_MTR, 3) to TP_DR_SPARE from TP_DR_SDD_MTR.

[6] 2/29/96 delete TP_SD_TEMP, and TP_RC_OS_FIN. Both deleted for PF.

7. 11/24/95 change TP_SM_SDSM_GEDET to TP_SM_DET_AMP3.

----------Chgs since 5/8/96 151840 Initial Release----------

8. 7/28/96 1) replace EM Eq TP01 with PF Eq TP01p & 2) drop all alarm limits.
9. 7/28/96 1) replace EM Eq TP02 & TP04 with PF Eq TP02p & 2) drop most alarm limits.
10. 7/30/96 provide TP_DR_FS Eq TP04ps1& TP04ps2 2 places; no alarm limits specified.
11. 7/31/96 provide TP05p Eq for TP_DR_SVD; no alarm limits.
12. 7/31-8/10/96 enter 2 segment CPA/CPB TP_BB_TEMPxxH Eqs; no alarm limits.
13. 8/5/96 provide new Eq TP02ap (2-segment) for SRCA Lamp ring with alarm limits.
14. 8/5/96 Define 13 VR_TM_REF_XXXX to be raw DN fixed values.
15. 8/5/96 revise High Norm & Alarm limits on TP_PS1_CVTR_SW, TP_PS1_DIODE_OUT, TP_PS2_CVTR_SW and TP_PS2_DIODE_OUT.

[16] 8/5/96 Delete TP_SA_RCT1_HSG and TP_SA_RCT2_HSG. T20-6 doesn't carry spares, but T20-2A does.

[17] 9/6/96 Reversed the segment sequence ID on all segmented equations (boxed items) so that increasing DN corresponds to increasing segment ID number.

18. 9/13/96 Revise TP_DR_NAD & TP_DR_SDD temp SF due to circuit chg. Becomes a 3-segment equation. No limits.
19. 9/20/96 Minor name chgs to match T20-2A names: TP_MF_AOBKHD_NX to TP_MF_NX_AOBKHD,TP_MF_AOBKHD_PX to TP_MF_PX_AOBKHD and TP_MF_AOBKHD_MX to TP_MF_OB_BLKHD.
20. 10/10/96 Delete TP_ME_TB07. (It is carried as spare S/C pt-pt in Table 20-2A, but not in this table.)
21. 10/14/96 Additional minor name chgs (see #19) to match T20-2A, TP_MF_CALBKHD_BB to TP_MF_Z_BKHD_BB and TP_MF_CALBKHD_YZ to TP_MF_YZ_CALBKHD.
22. 4/97 Multiple EO1122D Incorporations for Rev B. See EO1122D (released 970305) for details of bit increase for several words and name chg & spare chg.

22L 4/97 Multiple EO1122D Incorporations for Rev B. These items have either false don't care limits, or equation segments extended, to prevent OASIS from inserting default zero values, or, equation scale factor defaults to DN units.

[23] 4/97 Direct Rev B change to add a sentence to Note 7 to identify the Eq# that relates to the S/C BDU vs the SBRS RTIU.

TABLE 20-7. MODIS DIRECT TELEMETRY PINOUTS/TEST FRAMING

REFERENCE

Sort by RTIU Table #. See Notes for type of reference information provided by this table.

Subsys	Mnemonic Name	MODIS J4 Pin	RTIU Conn/Pin	RTIU Name	RTIU Table #	Start Bit
MF	TP_MF_TOP_BY_KM1	1	J11-01	ANL A1	17	25
MF	TP_MF_TOP_BY_KM1_RTN	2	J11-20	ANL A1 RTN		
AO	TP_AO_PZ_BY_RC	4	J11-02	ANL A2	18	65
AO	TP_AO_PZ_BY_RC_RTN	5	J11-21	ANL A2 RTN		
MF	TP_MF_TOP_BY_KM3	8	J11-03	ANL A3	19	105
MF	TP_MF_TOP_BY_KM3_RTN	9	J11-22	ANL A3 RTN		
MF	TP_MF_OB_BLKHD	13	J11-04	ANL A4	20	145
MF	TP_MF_OB_BLKHD_RTN	14	J11-23	ANL A4 RTN		
ME	TP_ME_NX_HTSINK	16	J11-05	ANL A5	21	185
ME	TP_ME_NX_HTSINK_RTN	17	J11-24	ANL A5 RTN		
ME	TP_ME_SPARE	19	J11-06	ANL A6	22	225
ME	TP_ME_SPARE_RTN	20	J11-25	ANL A6 RTN		
PC	TP_PCFAM_RADIATOR	22	J11-07	ANL A7	23	265
PC	TP_PCFAM_RADIATOR_RTN	23	J11-26	ANL A7 RTN		
PV	TP_PVSAM_RADIATOR	25	J11-08	ANL A8	24	305
PV	TP_PVSAM_RADIATOR_RTN	26	J11-27	ANL A8 RTN		
ME	TP_ME_PSRADIATOR	28	J11-09	ANL A9	25	345
ME	TP_ME_PSRADIATOR_RTN	29	J11-28	ANL A9 RTN		
-	Unwired spare analog channel	na	J11-10	ANL A10	26	385
-	Unwired spare analog chnl rtn	na	J11-29	ANL A10 RTN		
-	Unwired spare analog channel	na	J11-11	ANL A11	27	425
-	Unwired spare analog chnl rtn	na	J11-30	ANL A11 RTN		
DR	CR_DRNAD_1LATCHD	33	J9-01	BLV A1	49	465
DR	CR_DRNAD_1LATCHD_RTN	34	J9-20	BLV A1 RTN		
DR	CR_DRNAD_2LATCHD	35	J9-02	BLV A2	50	505
DR	CR_DRNAD_2LATCHD_RTN	36	J9-21	BLV A2 RTN		
DR	CR_DRSVD_1LATCHD	44	J9-03	BLV A3	51	545
DR	CR_DRSVD_1LATCHD_RTN	45	J9-22	BLV A3 RTN		
DR	CR_DRSVD_2LATCHD	46	J9-04	BLV A4	52	585
DR	CR_DRSVD_2LATCHD_RTN	47	J9-23	BLV A4 RTN		
DR	CR_DRSDD_LATCHD	54	J9-05	BLV A5	53	625
DR	CR_DRSDD_LATCHD_RTN	55	J9-24	BLV A5 RTN		
CP	CR_CP_A_ON_S	56	J9-06	BLV A6	54	665
CP	CR_CP_A_ON_S_RTN	57	J9-25	BLV A6 RTN		
CP	CR_CP_B_ON_S	65	J9-07	BLV A7	55	705
CP	CR_CP_B_ON_S_RTN	66	J9-26	BLV A7 RTN		
CP	CR_WIRED_SPARE	67	J9-08	BLV A8	56	745
CP	CR_WIRED_SPARE_RTN	68	J9-27	BLV A8 RTN		
CP	CR_WIRED_SPARE	75	J9-09	BLV A9	57	785
CP	CR_WIRED_SPARE_RTN	76	J9-28	BLV A9 RTN		
DR	CR_DR_FS_ENABL_S	77	J9-10	BLV A10	58	825
DR	CR_DR_FS_ENABL_S_RTN	78	J9-29	BLV A10 RTN		
PS	CR_PS1_ON	81	J9-11	BLV A11	59	865
PS	CR_PS1_ON_RTN	82	J9-30	BLV A11 RTN		
PS	CR_PS2_ON	84	J9-12	BLV A12	60	905
PS	CR_PS2_ON_RTN	85	J9-31	BLV A12 RTN		
PS	CR_PS1SHDN_ENA_S	86	J9-13	BLV A13	61	945
PS	CR_PS1SHDN_ENA_S_RTN	87	J9-32	BLV A13 RTN		
PS	CR_PS2SHDN_ENA_S	92	J9-14	BLV A14	62	985
PS	CR_PS2SHDN_ENA_S_RTN	93	J9-33	BLV A14 RTN		
PS	CR_PS1SRVHTR_ENA	94	J9-15	BLV A15	63	1025
PS	CR_PS1SRVHTR_ENA_RTN	95	J9-34	BLV A15 RTN		
PS	CR_PS2SRVHTR_ENA	98	J9-16	BLV A16	64	1065
PS	CR_PS2SRVHTR_ENA_RTN	99	J9-35	BLV A16 RTN		

TABLE 20-7. MODIS DIRECT TELEMETRY PINOUTS/TEST FRAMING

REFERENCE

Sort by RTIU Table #. See Notes for type of reference information provided by this table.

Subsys	Mnemonic Name	MODIS J4 Pin	RTIU Conn/Pin	RTIU Name	RTIU Table #	Start Bit
CP	CR_CPA_EEP_WRE_S	59	J10-01	BLV B1	65	1105
CP	CR_CPA_EEP_WRE_S_RTN	60	J10-20	BLV B1 RTN		
CP	CR_CPB_EEP_WRE_S	62	J10-02	BLV B2	66	1145
CP	CR_CPB_EEP_WRE_S_RTN	63	J10-21	BLV B2 RTN		
RTIU	SELF_TEST_RESULT	na	na	SELF TEST	81	1185
RTIU	TEST_JACK	na	na	TEST JACK	82	1225
RTIU	TEMP_1	na	na	TEMP_1	83	1265
RTIU	TEMP_2	na	na	TEMP_2	84	1305
RTIU	TEMP_3	na	na	TEMP_3	85	1345
RTIU	TEMP_4	na	na	TEMP_4	86	1385

NOTES:

1. This table provides a mix of Reference Information. It's main purpose is to provide the SBRS STE RTIU point-point framing defintion. It also includes MODIS J4 and RTIU J9, J10 & J11 pinout data. S/C point-point data is processed by the Bus Data Unit (BDU).

2. The RTIU telemetry frame is a fixed pattern, 1424 bits long with a one sec period . The first 3 bytes contain a 1 byte sync word and a 2 byte definition of number of bytes to follow. Begining at an offset of 25 bits, there are 35 wordsX5bytes. The last byte of each word is a space byte to facilitate CPU or remote terminal control.

3. The majority of the 35 telemetry words are MODIS functions, and the remainder are RTIU functions. The MODIS words routed by RTIU J11 are 8-bit passive analog telemetry (temperatures). The words routed by J9 & J10 are single bit bilevel status telemetry.

APPENDIX C. MODIS SCIENCE AND ENGINEERING DATA

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30.1 SCOPE

Tables in this Appendix are at the back for continuity of limited text.

Appendix C describes MODIS science and engineering data that is sent over the high rate science link with FDDI (FI) encoding to the spacecraft (S/C).

The term "Science Data" pertains to FPA sensor data that is collected over the earth view and four calibrator views. "Engineering Data" relates to subsystem parametric data that is associated with the performance of the science data. Engineering Data is collected by similar processes as the housekeeping telemetry (digital processing, analog processing or SW processing). Some of the engineering data is generated from whichever calibrator is in use. Selected small subsets of housekeeping telemetry is repeated in the engineering data. Also, the current and prior telemetry major cycles are repeated in full in the engineering data.

As noted in Section 1.2, the multiple use of this document for development and test, ICD data definition and operations planning, results in the inclusion of material that is not of interest to all users. Additional specific notes sometimes highlight this in the presentation of tabular data.

The MODIS two-character subsystem abbreviations defined in Figure 11 and Table 10 are used throughout this Appendix along with full names.

30.2 PURPOSE

The primary purpose of this Appendix is to define the contents and structure of the science and engineering data CCSDS packets.

First, a short overview is presented on the acquisition and processing of the FPA sensor data. The sequence of information will be as follows:

a. Revisit the MODIS 1.477 sec scan cycle.

b. Describe FPA sensor layouts, scan patterns and data readout.

c. Briefly overview the formatter block diagram and functions.

d. Describe general CCSDS packet, tailored into science, engineering, and test packets.

30.3 MODIS 1.477 SECOND SCAN CYCLE

The MODIS 1.477 sec scan cycle was described in Section 5.1 in relation to the 1.024 sec 1553 bus command and telemetry cycle, and how the view sectors are located. Figure 13 is repeated here as Figure 30-1 to address relations to FPA sensor science data and engineering data.

The major activities that occur during a scan cycle are indicated on the pie chart portion of Figure 30-1. Some points to emphasize or add, follow:

a. The numbers adjacent to the view sectors indicate the number of formatted frames of data (FD) obtained from each view.

b. A number of activities occur at the end of the earth sector.

c. SDSM or SRCA motors are stepped at the end of earth or between other view sectors. That is, mechanisms are kept quiet during FPA sensor collections.

d. As indicated, there is only one Index pulse per mirror revolution. Side 1 and Side 2 are tracked by encoder and vernier counts for individual sector locations.

e. The SD is defined as the start of the 1.477 sec scan cycle.

f. A Day FD requires 2 science data packets; a Night FD requires just one science data packet. When in Night mode, Night FD's are obtained from the earth view, but full Day FD's (all band data) are obtained from calibrator views.

g. Transmission of science packet FD's begins after 30 unformatted frames of data are collected (30 frames are required for formatting), and continues past the collection point until the FIFO empties.

h. Telemetry collects include telemetry-like engineering data.

i. FPA sensor data collected during the BB view is used to calculate DC restore (DCR) offset values.

j. During SDSM operations, its pointing mirror will generally be stepped between the SD, the SDSM DCR view, and the SUN, and then back again for approximately two minutes. The 9 SDSM detectors are sampled 3X at each SDSM view. Within the same scan cycle, these samples are collected immediately after the SD, SRCA and Space sectors.

k. During SRCA operations, data from its internal source output and reference output, will be collected in near-time proximity to when the FPA sensors view the SRCA.

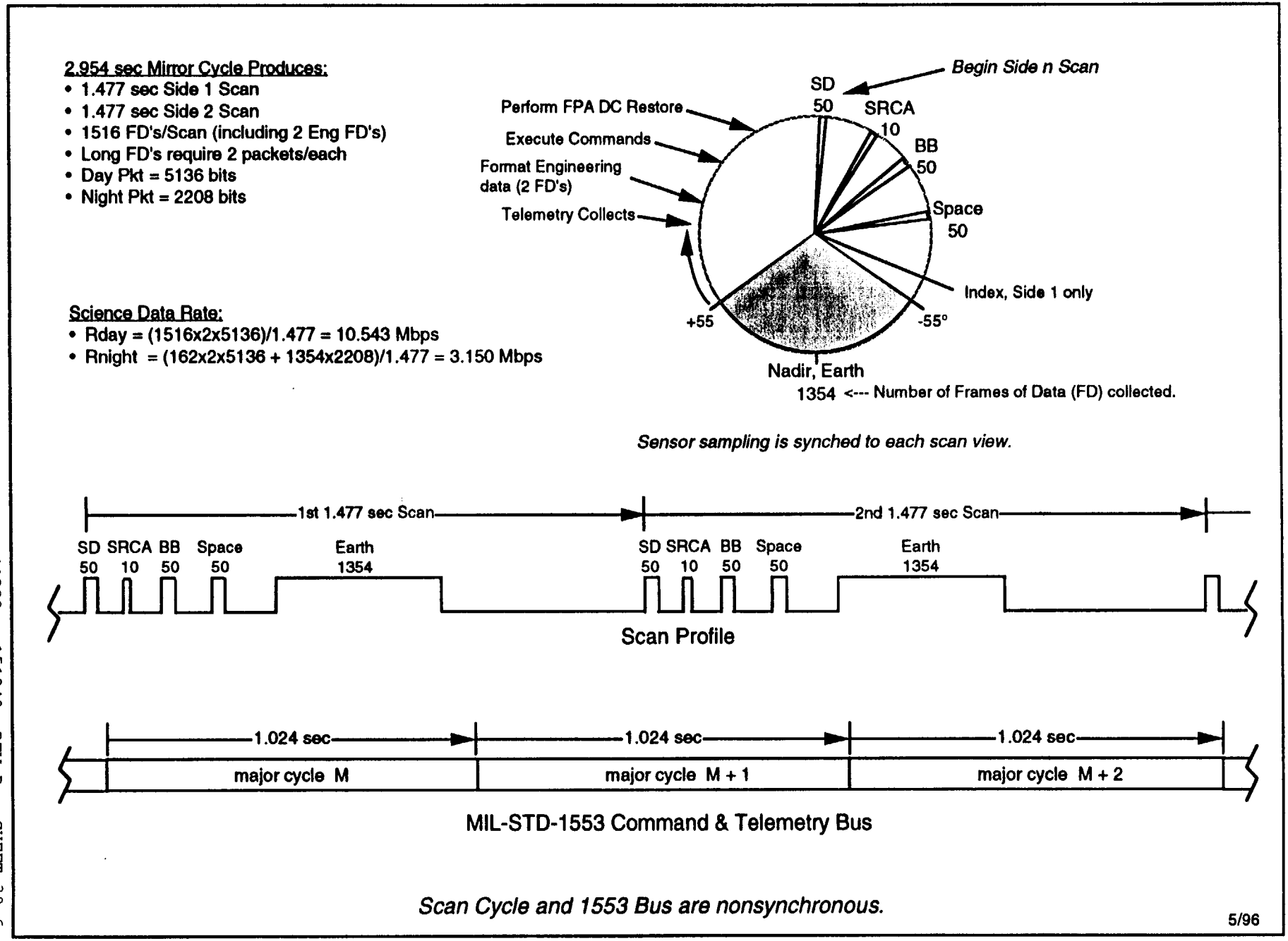


Figure 30-1. Scan Profile Activities (same as Figure 13)

30.4 FPA LAYOUTS, OFFSETS & READOUTS

30.4.1 FPA Layouts/Offsets. Figure 30-2 shows the four FPA layouts. They are drawn approximately to relative scale, but without slight intentional curvature, which minimizes optical distortion effects. The S and T indicate the scan and track direction that the projected ground pattern would travel. Figure 30-3 shows the composite optical overlay of all four FPA's for just 1 of 10 1km IFOV detectors. This illustrates the scan direction registration offsets between the bands. Band 30 is the first to view a scene, and after 29 1km IFOV's Band 32 is the last to view the same scene. This is why it takes 30 frame collects before the Formatter can assemble one formatted frame of data, FD.

30.4.2 FPA Readouts. The signal outputs from the four FPA's are amplified and digitized by the FAM (PC) and SAM (PV) and routed to the Formatter in the MEM as 8 simultaneous serial data streams. The FPA readout order and relative timing is illustrated in Figure 30-4. The FAM and SAM input/output order and timing is the same except for a slight delay difference. Also, inputs are in analog form and outputs are in digital form. The 333.333 µs (3 kHz pixel clock) sample time duration of the figure represents one frame of data (FD), which contains data from all channels of all bands.

The formatter receives 990 samples in an unformatted FD as a result of over-sampling and dual-gains for some bands. It stores 29 unformatted FD's before it can process them with the 30th unformatted FD to produce a formatted FD, which contains 830 samples spatially aligned to view the same ground spot. The scan direction band offsets illustrated in Figure 30-3 are used to provide the formatted FD. The formatted FD is sent over the science link in band number sequence as described in 30.8.

30.5 FORMATTER, FIFO and FDDI OVERVIEW

These three items are discussed together because they function as a digital chain to accept unformatted FPA sensor data, format it, buffer it and send it and engineering data over the high rate science link in CCSDS packets.

30.5.1 Formatter. The formatter provides the following functions:

a. Generate formatted FPA frames of data (FD) from unformatted FPA frames of data.

b. Assemble the formatted frames into CCSDS science data packets.

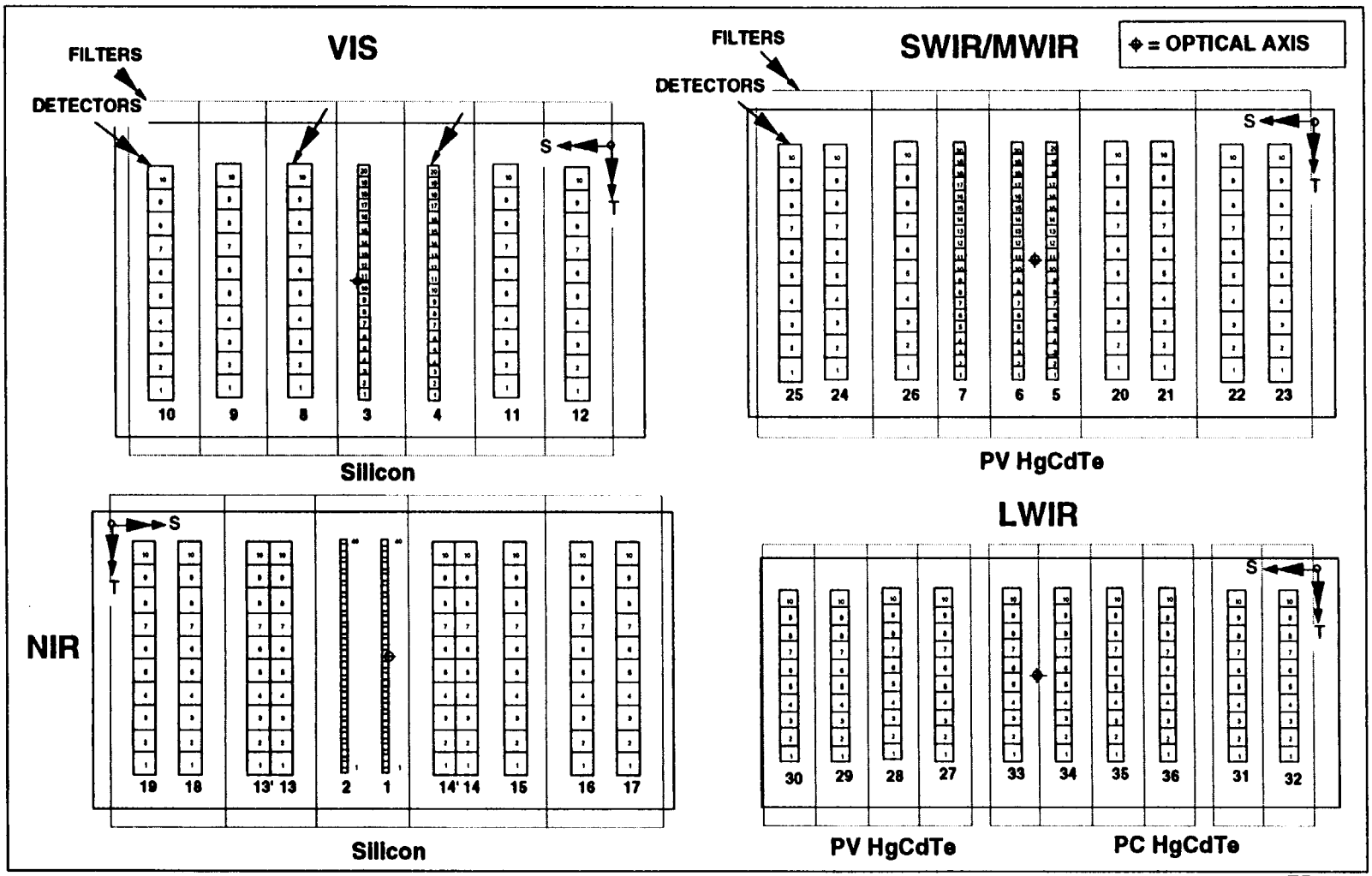
c. Provide a serial bidirectional link to the CP.

d. Generate engineering data packets.

e. Process and generate memory dump packets.

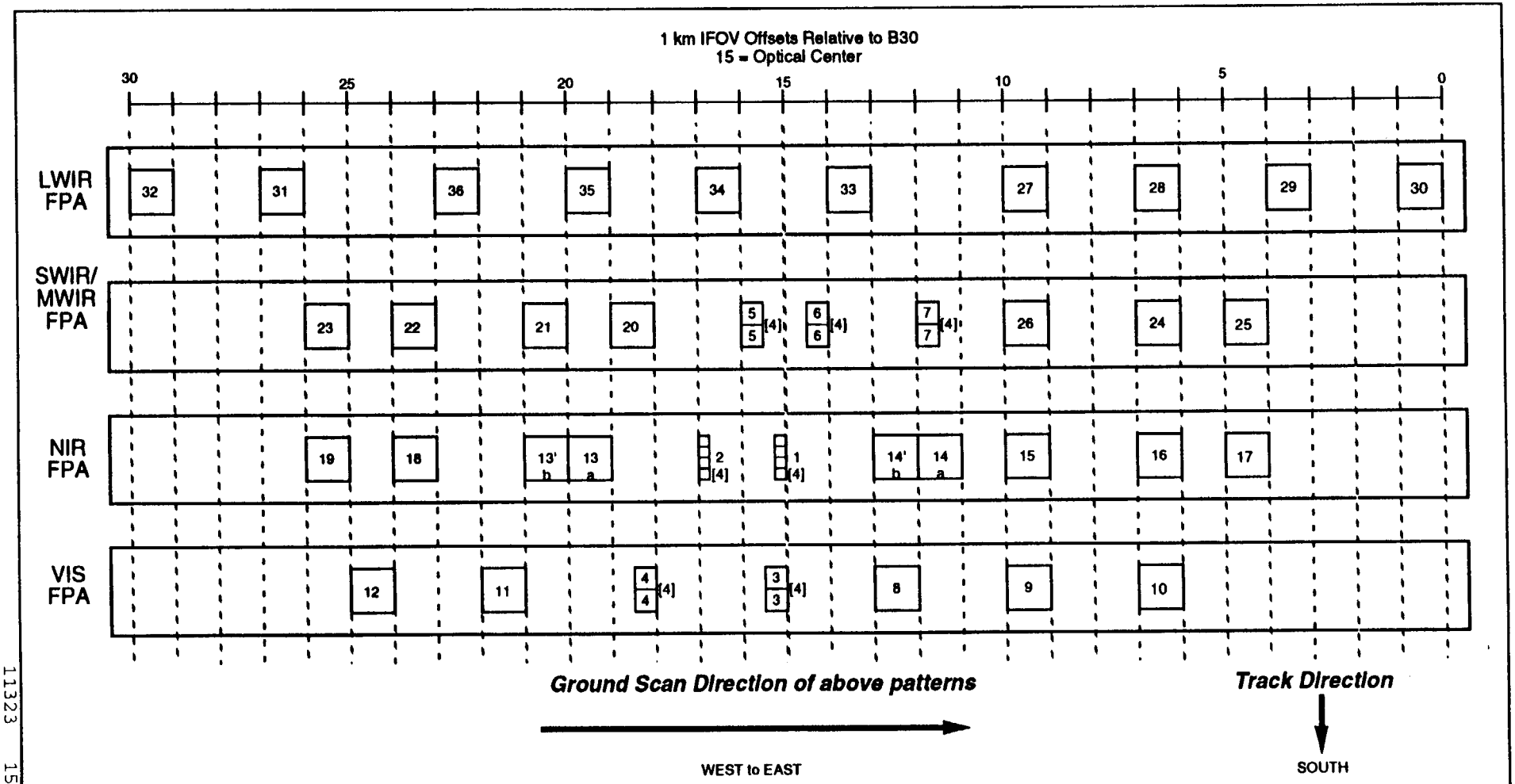
f. Generate test packet to check higher rate link.

g. Track the scan mirror cycle to start and stop collection of data at each scene sector. Provide related synchronization to the timing generator.



- FPAs are to relative scale; different size due to different focal lengths
- Slight intentional curvature to correct for optics distortion is not depicted

Figure 30-2. MODIS FPA Layouts

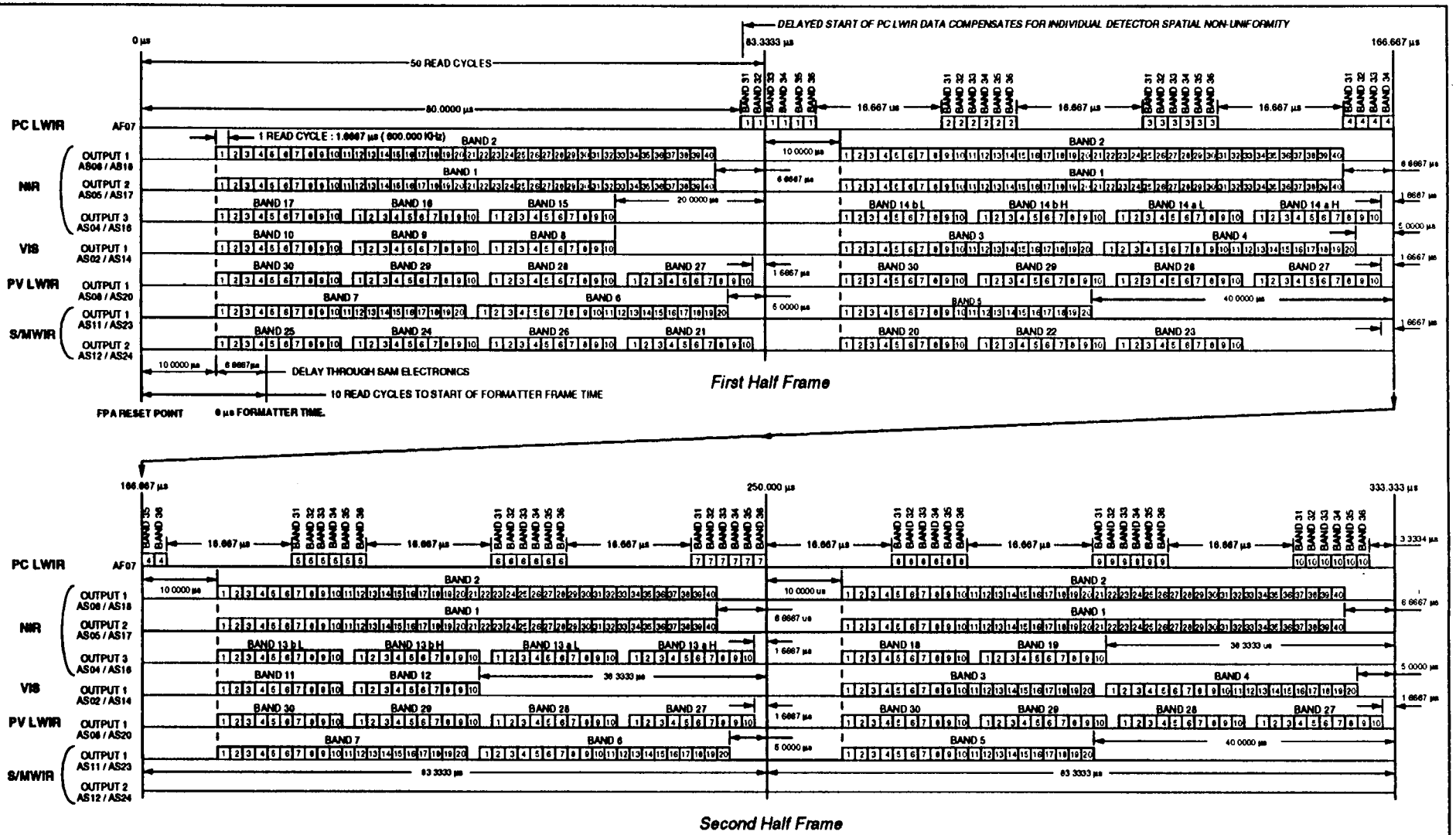


Notes:

1. Band single detector locations are shown in terms of 1 km IFOV offsets from Band 30, which is first band to see a scene. FPA optical center is at IFOV 15.
2. Ground scan direction of projected pattern is to the right (west to east). FPA's have false vertical separation to clarify individual FPA extent.
3. During one 1km sample, 250 m Bands 1 & 2 produce 16 samples/each and 500 m Bands 3-7 produce 4 samples/each.
4. The formatter assembles a science packet with bands aligned by the depicted offsets to view a common ground sample. This requires the collection of 30 frames of data before all bands have observed the same ground sample.
5. Science packet locations for TDI Bands 13, 13' and 14, 14' will be at first sample location of 13 and 14. High and low gain data is provided for Band 13 and Band14. Bands 27-30 are sampled 4X, but single sample is sent to ground.

3/96

Figure 30-3. FPA Band Offsets Relative to Band 30



- *FPA order is for reference information, for current details see ICD for VIS, NIR, SWIR/MWIR or LWIR FPA.*
- *Note FPA zero time and Formatter zero time in first half frame.*
- *Total data represents one unformatted Frame of Data (FD).*

Figure 30-4. FPA Readout Order and Timing

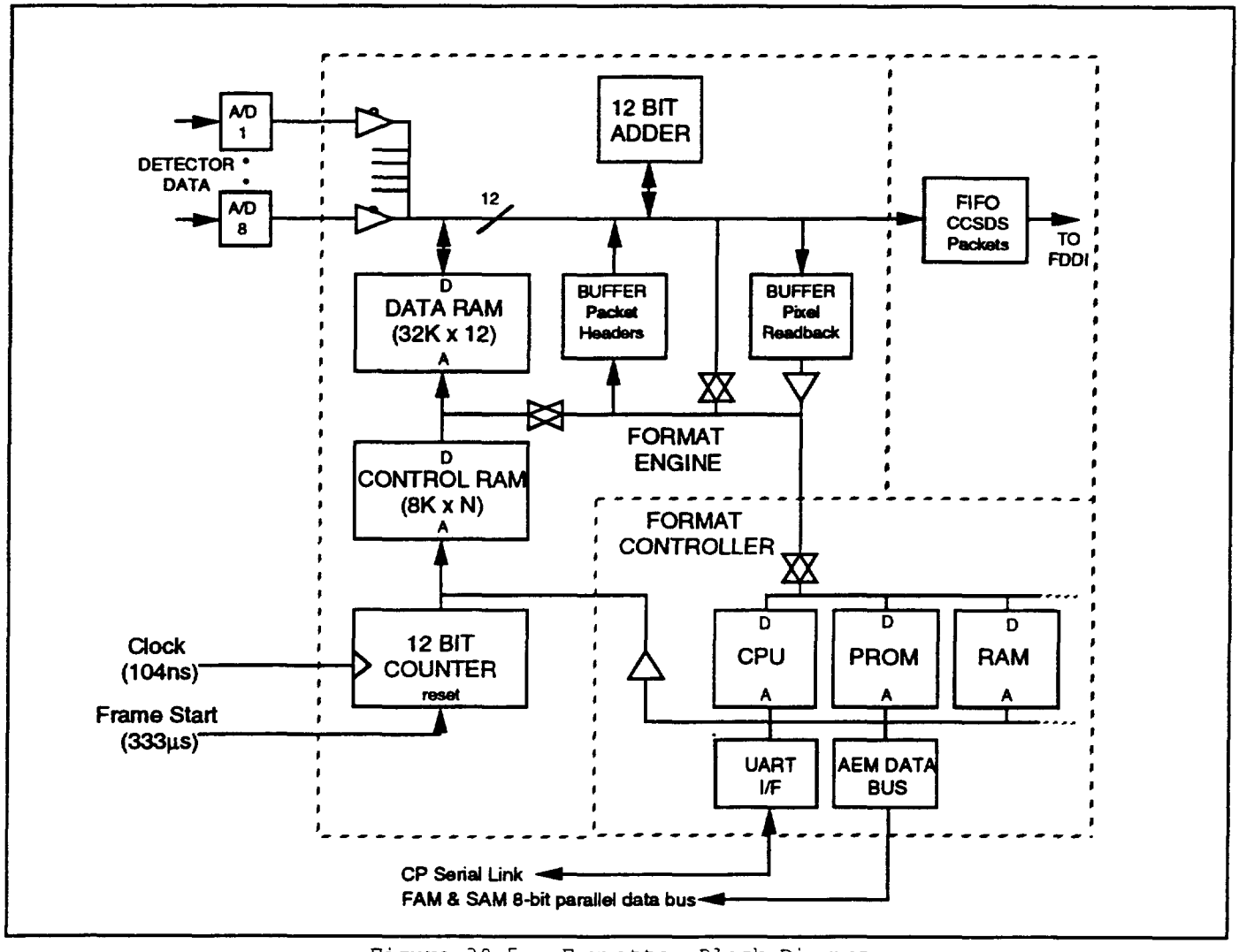


Figure 30-5. Formatter Block Diagram

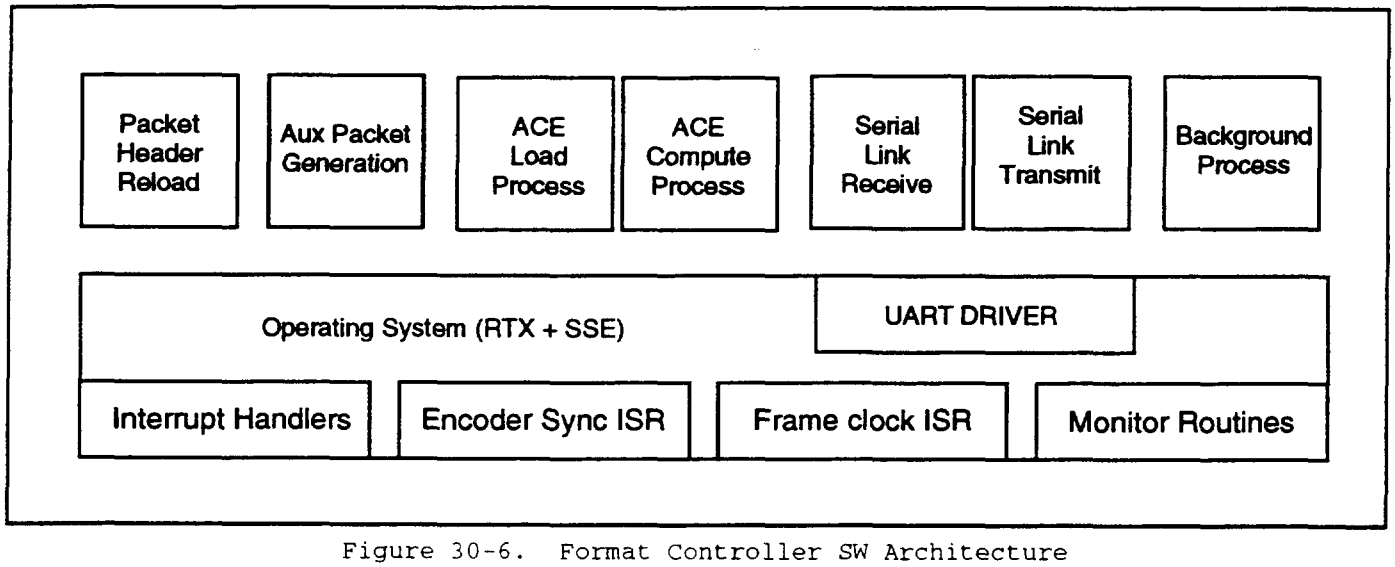


Figure 30-6. Format Controller SW Architecture

h. Monitor and periodically report the speed of the scan mirror during earth sector data collections. Calculate the mirror revolution period.

i. Compute DC offset restore parameters for each channel.

j. Provide offsets, PV gains, sample delays and PV FPA biases to the FAM and SAM over an 8-bit data bus.

k. Perform summation of collected TDI FPA samples, Bands 13 & 14, and oversampled Bands 27-30.

The Formatter block diagram is presented in Figure 30-5. The Formatter consists of a hardware Format Engine to rapidly process the large amount of FPA sensor data that has to be buffered and formatted each 1.477 sec scan cycle, and a Format Controller with a microprocessor for controlling the formatter functions listed above. The microprocessor is the same single board computer (SBC) used in the CP, except it doesn't have the related peripherals for overall instrument control.

The software (SW) architecture for the Format Controller is illustrated in Figure 30-6.

30.5.2 FIFO. The FIFO, which is implemented as a ping-pong RAM set (any 2 of 4 is needed), has the following features:

a. Buffer storage of 768K x 32 words between the formatter and the FDDI, implemented as 4 identical blocks of memory. Any 2 of the 4 blocks provides the required buffering, when operating in a ping-pong read-write manner.

b. The FIFO accepts formatter 16 bit words at 9.6 MHz, and sequentially stores them as 32 bit words at 4.8 MHz.

c. The FIFO may be sequentially read by the FDDI as 26 bit words at 2.2 MHz.

30.5.3 FDDI. The FDDI (Fiber Distributed Data Interface)* provides the high rate science link to the S/C and has the following features:

a. Encoding of the CCSDS science packet data into a FDDI (4B/5B) protocol per GSFC 420-03-02 GIIS, 6.4.

b. Transfer timing accomplished per the GIIS. The peak data rate shall not exceed 11.0 Mbps, and the average data rate over any two orbit period shall not exceed 6.2 MHz per GSFC 421-12-04-01 MODIS UIID, assuming a duty cycle of 40% Day rate and 60% Night rate.

c. MODIS data rates are: Day = 10.543 Mbps & Night = 3.150 Mbps (see Figure 30-1 for derivation).

* *This is a differential electrical coax interface with data formatted to the same protocol as data would be on a fiber optics interface.*

30.6 MODIS CSSDS SCIENCE PACKET GENERAL FORMAT

The formatter generates CCSDS science packets for the FDDI to send to the spacecraft over the high rate science link. The general definition and content of the MODIS CCSDS packets are shown in Figure 30-7. The first 120 bits contain the CCSDS Primary Header and Secondary Header, and the remaining is considered the Data Zone. The CCSDS Primary Header and Secondary Header have standard definitions for all EOS-AM instruments per the GIIS. MODIS has a deviation to permit using 7 of 8 Quick Look Flag bits for MODIS header data. The balance of the Data Zone is divided into particular MODIS fields consisting of a MODIS Header and Data Field. The MODIS Header is further divided into the indicated fields in Figure 30-7, which have details defined below. The MODIS Data Field contains different data that varies according to the type of packet (science long/short or engineering).

30.7 MODIS CSSDS SCIENCE PACKET DETAIL FORMAT

Figure 30-8 provides complete details for all fields of the CCSDS packet except for the Data Field, and includes alternate sub field detail. Details of the Data Field are presented later. The details in Figure 30-8 follow the requirements for the 48-bit Primary Header and 72-bit Secondary Header as defined in GIIS Change 4 Figure 6-6 except for the Quick Look Flag.

Paragraph titles within 30.7 below are followed by the Figure 30-8 titles (full word or abbreviation).

30.7.1 VERSION, TYPE & SECONDARY HEADER FLAG. The GIIS specifies the VERSION field to be set to zero, the TYPE field to be 0=Normal or 1=TEST, and the SECONDARY HEADER FLAG to be set to one.

30.7.2 Application Process ID. APID's are unique for each instrument, and for MODIS vary from decimal 064 through 127 per the MODIS UIID. APID's will be pre-assigned, but can be set by separate operational commands for science and engineering packets. See Table 10-25A for respective commands FR08 and FR11.

For MODIS Protoflight, APID 064 has been assigned to Science and Engineering Packets, and APID 127 assigned to the Test Packet. The APID field changes ID values to match the packet data contents.

For MODIS Flight 1, some MODIS APIDS are reserved for EOS PM spacecraft use. The forward link (commands) will use APID 110 for Instrument Command, APID 111 for Load Data and APID 112 for the Safe Mode Command. The return link (telemetry) will use APID 113 for Dump Data, APID 114 for Low Rate Engineering Data, APID 64 for Science/Engineering Data and APID 127 for the Test Packet.

30.7.3 PACKET SEQUENCE COUNT. The PKT SEQ CNT is the sequential count of packets associated with an APID. Individual matching, rotating Packet Counters must be used, if separate APIDs are assigned for different packet data. MODIS PF will initially use APIDs as defined in 30.7.2. The 14 bit counter will provide 0-16,383 count capability. In Figure 30-1 it will be noted that a single scan produces 1516 FDs (including engineering data). For Day mode, 2 packets per FD are required, which will result in 3032 packets/scan. So the 16,383 packet counter will roll over sometime during the sixth scan.

30.7.4 PACKET LENGTH. The PKT LENGTH field indicates the length of the data in the Data Zone (defined above) as the number of octets in binary count. For MODIS, this will normally be N1 = [(5136-48)/8]-1 = 635 octets or N2 = [(2208-48)/8]-1 = 269 octets dependent upon packet type.

30.7.5 TIME TAG. The TIME TAG field is inserted into the packet data in CCSDS day segmented time code. The details of day count, coarse time and fine time are contained in the lower left side of Figure 30-8. For MODIS, the current time tag is only applied to the packet containing the first frame of data (FD) for any view. Time for the balance of the view packets is related by the FD count that appears in the Source Identification field. An FD is 333.333 μs. The engineering packet time code takes on the same value as the first earth frame of data. Thus, true time for the first engineering packet has an offset of 1354 FDs x 333.333μs (0.4513328s).

30.7.6 QUICK LOOK. The QUICK LOOK flag is a single bit for MODIS, that can be set/reset by individual operational commands for the science and engineering packets. See Table 10-25A for respective commands FR09/FR10 and FR12/FR13.

As noted in 30.6, the MODIS definition deviates slightly from the GIIS in the Quick Look Flag field of the Data Zone, and only uses 1 of 8 bits for the Quick Look Flag.

30.7.7 PACKET TYPE. The PKT TYPE field varies according to the type of packets being sent to the S/C. See The center left of Figure 30-8 for legend details of 5 types.

30.7.8 SCAN COUNT. The SCAN COUNT field contains a small, near term count that can link accumulated packets to a particular scan. One scan mirror revolution produces two scans, one from Side 1 and one from Side 2.

30.7.9 MIRROR SIDE. The MIR SIDE field identifies which side of the mirror is the source for the 1.477 sec scan data.

30.7.10 SOURCE IDENTIFICATION/TYPE FLAG. The SOURCE IDENTIFICATION field has two forms with a TYPE FLAG single bit to identify which form describes the sensor data view source. One form provides the frames of data (FD) count collected over the earth view. The second form provides calibration view information. For this calibration data, the field is further subdivided to provide the calibration details indicated in the lower middle of Figure 30-8. The Source ID field has no meaning for engineering packets, and will be set to all zeroes (0's).

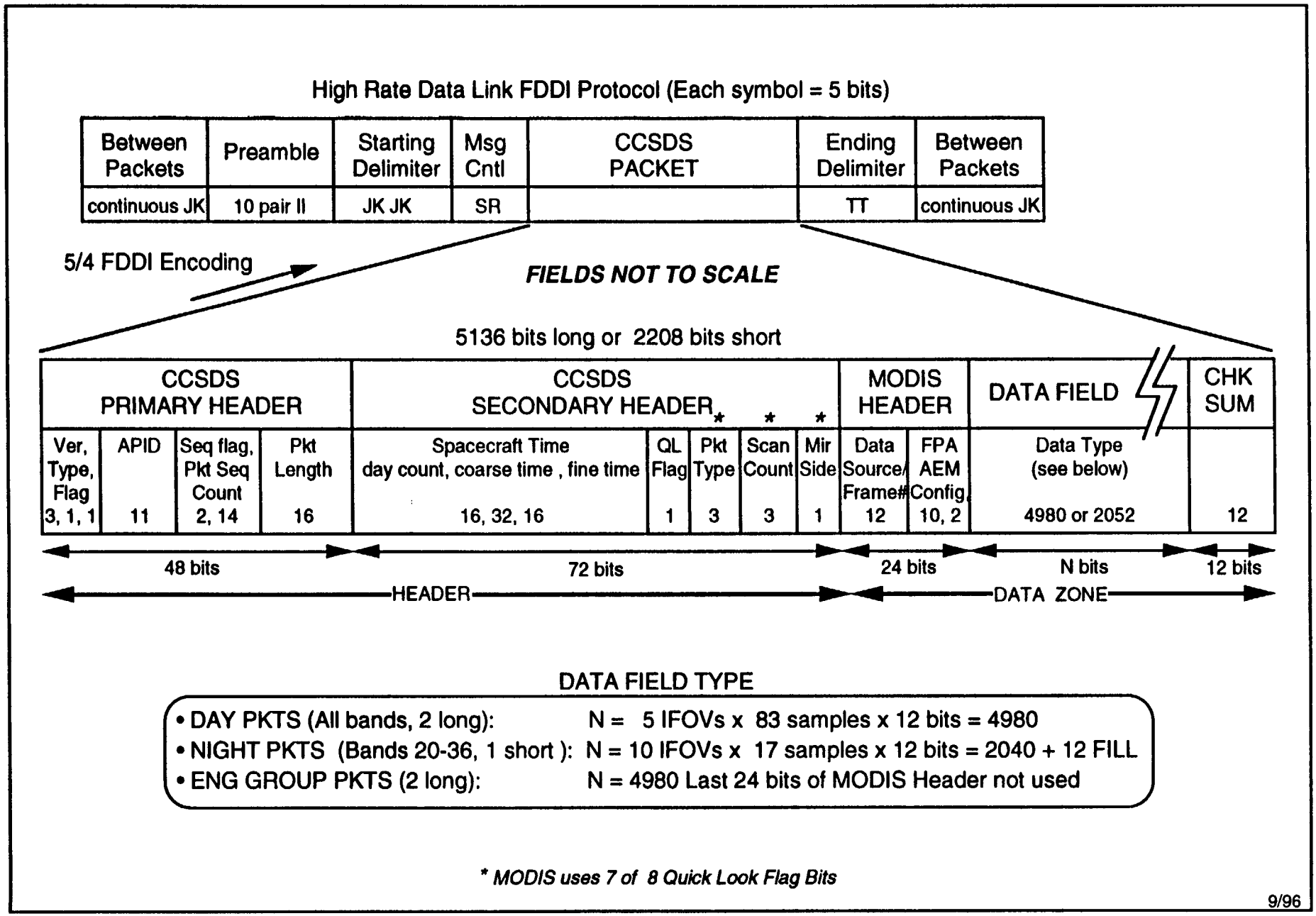
30.7.11 FPA/AEM CONFIGURATION. The FPA/AEM CONFIGURATION field provides the configuration status details of the four FPA's, which are controlled by the SAM and FAM AEM's. The PV FPA ROIC (readout integrated circuit) A/B selection follows the SAM A/B selection. Configuration details are indicated by the legend in the lower right side of Figure 30-8.

30.7.12 SCI STATE/SCI ABNORM. The SCI STATE and SCI ABNORM fields provide similar information. SCI STATE indicates the bottom line status of several subsystems, which have Normal/Test configuration options rolled into a single indicator. The single indicator is a software echo of Table 20-2A telemetry word CS_FR_SCI_NORMAL. Table 20-2B lists 18 items that are polled to obtain the rolled up status for CS_FR_SCI_NORMAL. (In some cases, the command state versus the telemetry state is polled, but the effect is the same for the summary status.) Roughly half of Table 20-2B relates to ground-test items, and the other half to on-orbit test items. However, all items are available as commands in Table 10-25A, if some on-orbit use can be devised for them.

SCI ABNORM is a ground-set flag that indicates prior knowledge of potentially abnormal science data due to things other than MODIS, such as, maneuvers, data link, etc. The flag is set/reset by command FR16: SET MOD FR_SCIABNORM TO ABNORM/NORM. The related 1553 bus telemetry word is SS_FR_SCIABNORM with ABNORM/NORM response.

30.7.13 DATA FIELD. The DATA FIELD is defined in detail below for each particular type of packet. In general, any type of packet has to contain an integer number of 12-bit items in order to pass the 12-bit Check Sum operation of the next field. In addition, the sum of the Data Field plus the 12-bit Check Sum field must be divisible by 24 in order for the FDDI Encoder protocol to operate correctly. This means that 12 fill bits have to be added to the night sensor 2040 bits to produce a 2052 bit Night Packet.

30.7.14 CHECK SUM. The CHECK SUM field contains the results of a formatter exclusive-or 12-bit check sum on the Data Field.



DATA FIELD TYPE

- DAY PKTS (All bands, 2 long): N = 5 IFOVs x 83 samples x 12 bits = 4980
- NIGHT PKTS (Bands 20-36, 1 short): N = 10 IFOVs x 17 samples x 12 bits = 2040 + 12 FILL
- ENG GROUP PKTS (2 long): N = 4980 Last 24 bits of MODIS Header not used

** MODIS uses 7 of 8 Quick Look Flag Bits*

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Figure 30-7. MODIS CCSDS Science Packet General Format

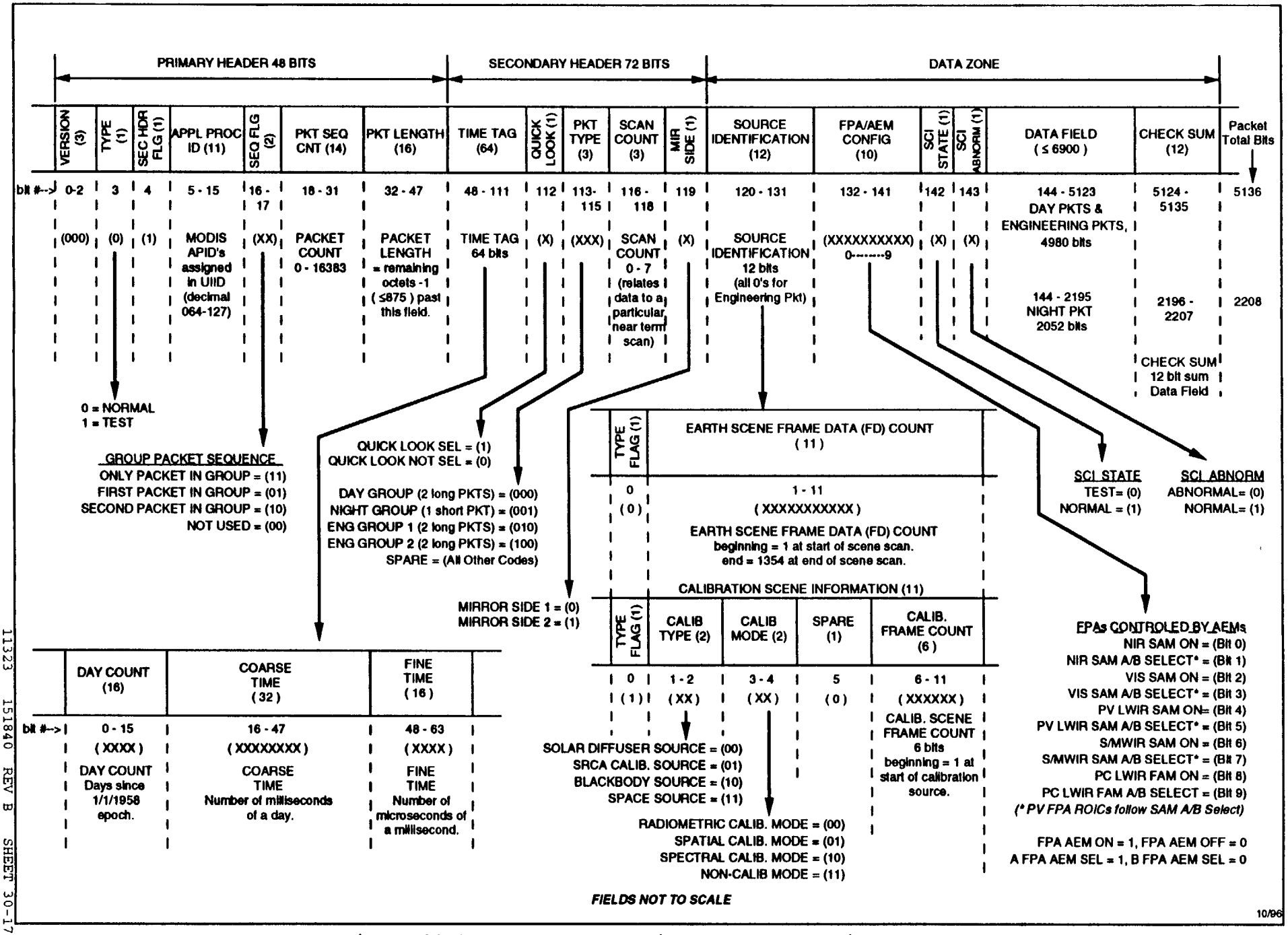


Figure 30-8. MODIS CCSDS Science Packet Detail Format

30.8 SCIENCE PACKET DATA FIELD DESCRIPTION

Beginning in September 1996, packet "segment" terminology was dropped, and "group" packet terminology was used. This results in packet data defined in terms of Science Day Group Packet 1 and Packet 2, Science Night Group Packet, Engineering Group 1 Packet 1 and Packet 2, and Engineering Group 2 Packet 1 and Packet 2. The Test Packet is a special case of any of the foregoing packets. Prior basic organizational details are essentially the same, except as noted in 30.9 and 30.10, where some engineering packet data fields have been relocated (see Figures 30-10 and 30-11 for layout overview).

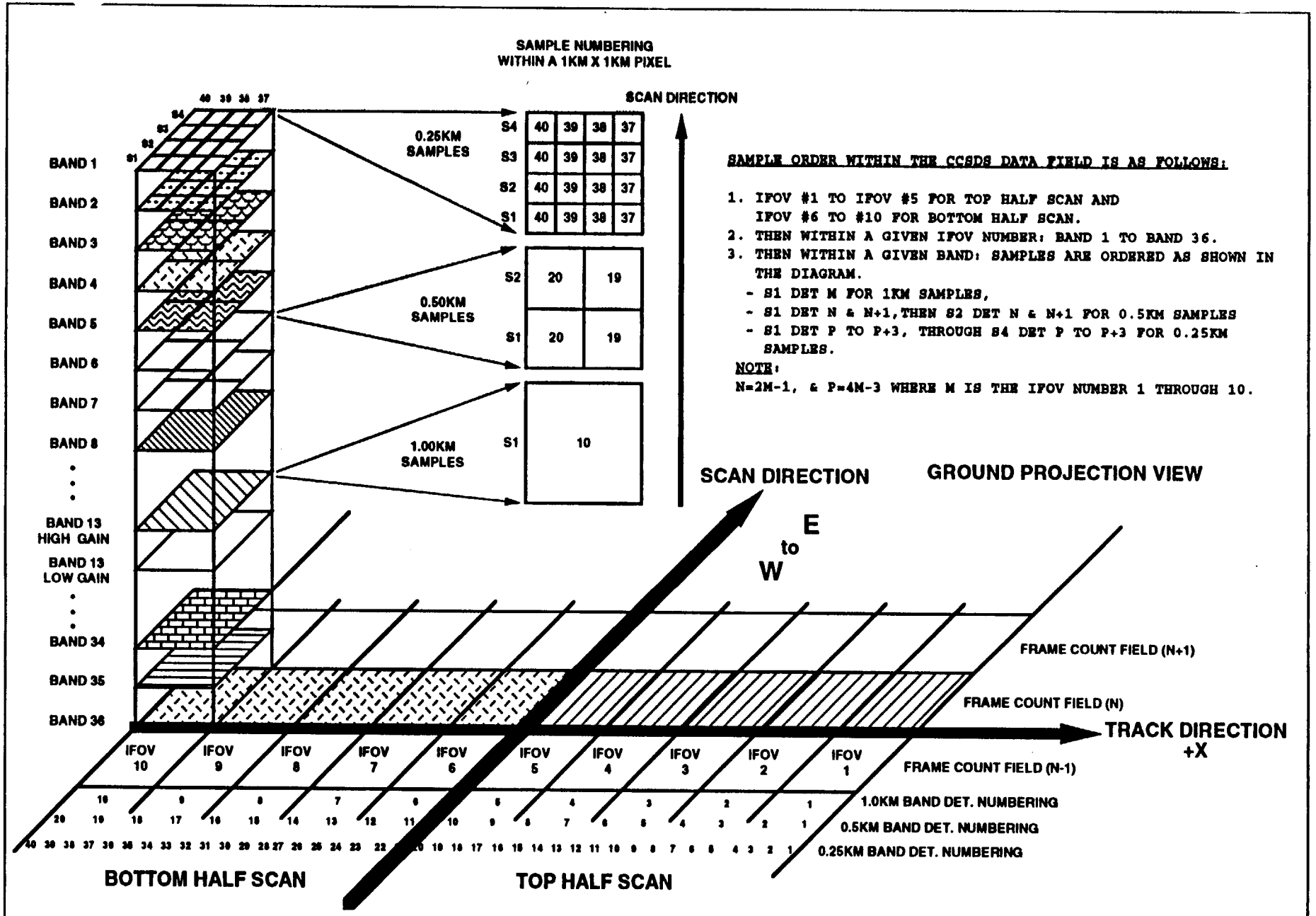
These descriptions only address the packet Data Field, and not the headers. The formatted Science sensor Frame of Data (FD) is organized and sequenced as shown by Figure 30-9, which because of its formatting relates similar ground IFOV's between the bands. This data is assembled into Day Group or Night Group science packets for transmission over the high rate science link. Day Group packets (long relative to night) contain 4980 bits. Night Group packets (short relative to day) contain 2052 bits (including 12 fill bits). Day Group data requires two packets, Packet 1 (IFOV 1-5) and Packet 2 (IFOV 6-10), to send all the day data. The Night Group data can be sent in a single Packet with all IFOVs 1-10. IFOV's are in terms of 1km IFOV's as is generally used throughout this document. Bands 1 & 2 have 250 m IFOV's and Bands 3-7 have 500 m IFOV's, both of which have a proportional increase in detector samples relative to the number of 1km IFOV samples.

30.8.1 Science Day Group Packet 1 Sensors IFOV 1-5. Table 30-1 provides the detailed bit locations for Science Day Group Packet 1 with Sensors IFOV 1-5. Column 1 contains the cumulative bit count within the packet for listed bands and detectors, including multiple samples where they exist. Table notes relate the exact Data Field start and end bit locations, which are the same as cited in Figure 30-8.

30.8.2 Science Day Group Packet 2 Sensors IFOV 6-10. Table 30-2 provides the detailed bit locations for Science Day Group Packet 2 with Sensors IFOV 6-10. As in Table 30-1, Column 1 contains the cumulative bit count within the packet for listed bands and detectors, including multiple samples where they exist. Table notes relate the exact Data Field start and end bit locations, which are the same as cited in Figure 30-8.

30.8.3 Science Night Group Packet Sensors IFOV 1-10. Table 30-3 provides the detailed bit locations for Science Night Group Packet with Sensors IFOV 1-10. As in Tables 30-1 & 30-2, Column 1 contains the cumulative bit count within the packet for listed bands and detectors. The night bands are inherently single sample detectors. Table notes relate the exact Data Field start and end bit locations, which are the same as cited in Figure 30-8. There are 12 fill bits added to the end of the night sensor data to produce a night field total bit count (2052) divisible by 24 for proper FDDI encoding.

30.8.4 Science/Engineering Scale Factors. DN scale factors are not provided in Tables 30-1, 2, 3, 4 and 7 for science data, DCR offsets and gains because of their interdependence and variation with test setups. Final calibration data will be contained in CDRL 222 Specification Compliance and Calibration Data Books.



Detail listings of sensor formatted Frame of Data (FD) appear in Tables 30-1, 30-2 & 30-3.

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Figure 30-9. MODIS FPA Sensors Formatted Frame of Data Structure

30.9 ENGINEERING GROUP 1 PACKET DATA FIELD DESCRIPTION

Engineering Group 1 Packets contains a variety of data that is generated or processed from several types of sources, and consists of two packets. Figure 30-10a provides a summary layout of Packet 1, and Figure 30-10b provides a summary layout of Packet 2.

The number of bits and the starting/ending packet bit locations for each data field, is blocked out in the figures. Details for each data field appear in the indicated table. Fill bits are used as needed to provided a group block divisible by 12 to facilitate FIFO/FDDI hardware transfers, and at the end to provide a packet data field that contains 4980 bits.

As indicated in 30.7, some MODIS header fields have no meaning for Engineering Group 1 Packets, and are set to zero.

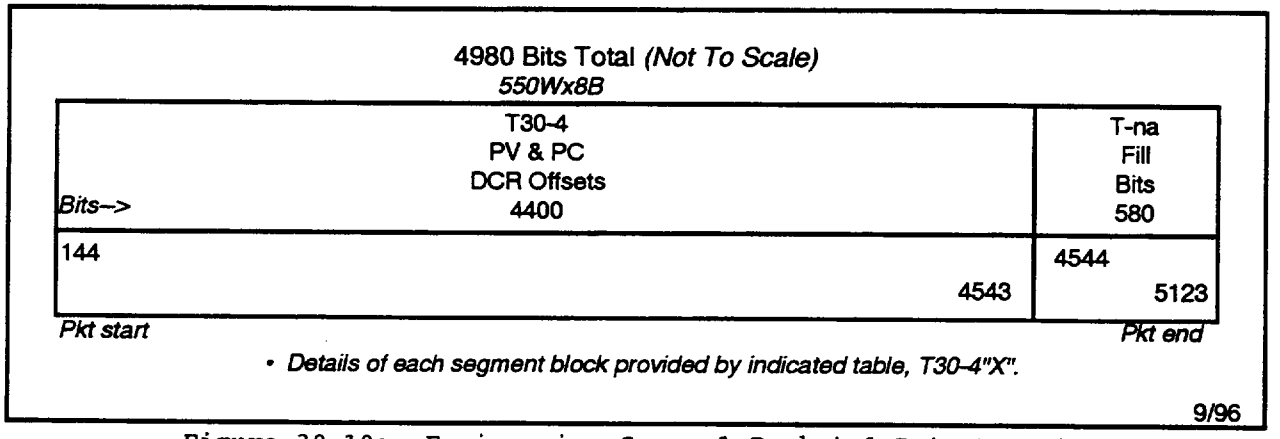

Figure 30-10a. Engineering Group 1 Packet 1 Data Layout

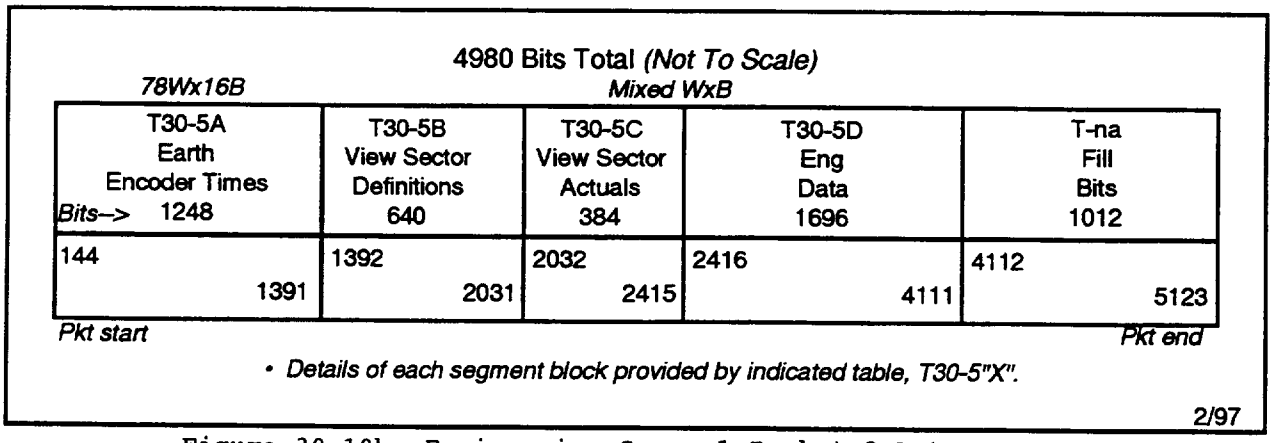

Figure 30-10b. Engineering Group 1 Packet 2 Data Layout

30.10 ENGINEERING GROUP 2 PACKET DATA FIELD DESCRIPTION

Engineering Group 2 Packet consists of two packets of 4980 bits each, and contains additional engineering data. Figure 30-11a provides a summary layout of Packet 1. Figure 30-11b provides the summary layout of Packet 2.

Details for each data field appear in the indicated table. Fill bits are used as needed to provided a group block divisible by 12 to facilitate FIFO/FDDI hardware transfers, and at the end to provide a packet data field that contains 4980 bits.

As indicated in 30.7, some MODIS header fields have no meaning for Engineering 2 Packets, and are set to zero.

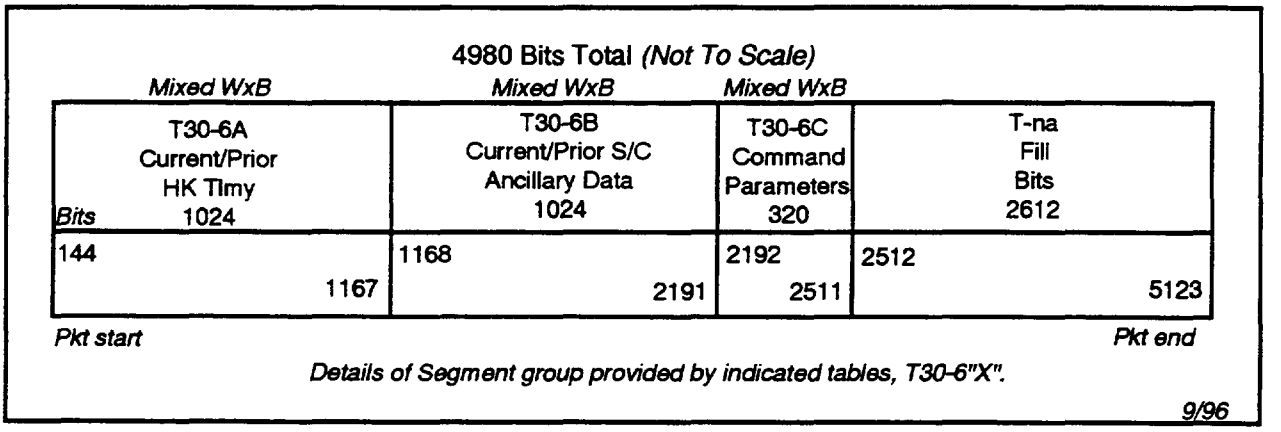

Figure 30-11a. Engineering Group 2 Packet 1 Data Layout

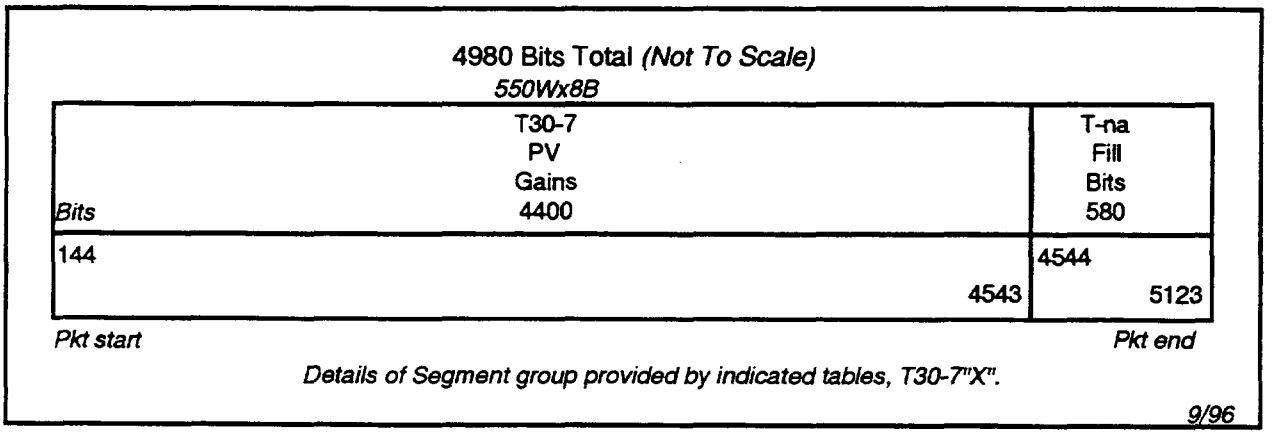

Figure 30-11b. Engineering Group 2 Packet 1 Data Layout

30.11 TEST PACKET DATA DESCRIPTION

As listed in Table 10-25A, MODIS command FR26 SET_FR_PKT_TYPE to NORMAL/TEST can toggle a MODIS test packet on and off. When set to TEST, the MODIS packet headers will contain the normal changing header data except APID 127 will replace normal APID 064. Also, the header Packet Sequence Count will change to count the number of Test Packets. When commanded to Test, MODIS continues to issue test packets until commanded back to Normal.

The headers and packets will reflect the prior MODIS configuration. That is, if in Day Rate, two Day Group packets will be issued in the Earth Sector. If in Night Rate, a single Night Group packet will be sent. For engineering Groups, two packets will be sent. The Data Field of the Test Packets will have fixed, non changing data that represents an increasing decimal count to a maximum of 415.

Tables 30-8A and 30-8B list the fixed data field information respectively for Test Day Packets 1 and 2.

Table 30-8C lists the fixed data for the Test Night Packet. Its values are the same as the same Band/Detector values listed in the Test Day Packets.

Engineering Group Packets do not have a tabular listing because they are the same as Test Day Packets 1 and 2.

The header Packet Type Field will change to provide the proper corresponding code for each of the above Day/Night/Engineering packets even though some of the data fields have the same fixed values.

When sending a Test Packet over the high rate science link, the FDDI Message Control Protocol changes from an SR symbol to an RR symbol.

TABLE 30-1. MODIS SCIENCE DAY GROUP PACKET 1 DATA FIELD

415Wx12B ***Day Packet 1 contains IFOV 1-5 data (4980 bits). See Figure 30-9 for interband relationship with ground pattern.***

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IFOV 1 (1km)				IFOV 2 (1km)				IFOV 3 (1km)				IFOV 4 (1km)				IFOV 5 (1km)			
Pkt Start Bit	Band	Det	Sample	Pkt Start Bit	Band	Det	Sample	Pkt Start Bit	Band	Det	Sample	Pkt Start Bit	Band	Det	Sample	Pkt Start Bit	Band	Det	Sample
144	1	1	1	1140	1	5	1	2136	1	9	1	3132	1	13	1	4128	1	17	1
156	1	2	1	1152	1	6	1	2148	1	10	1	3144	1	14	1	4140	1	18	1
168	1	3	1	1164	1	7	1	2160	1	11	1	3156	1	15	1	4152	1	19	1
180	1	4	1	1176	1	8	1	2172	1	12	1	3168	1	16	1	4164	1	20	1
192	1	1	2	1188	1	5	2	2184	1	9	2	3180	1	13	2	4176	1	17	2
204	1	2	2	1200	1	6	2	2196	1	10	2	3192	1	14	2	4188	1	18	2
216	1	3	2	1212	1	7	2	2208	1	11	2	3204	1	15	2	4200	1	19	2
228	1	4	2	1224	1	8	2	2220	1	12	2	3216	1	16	2	4212	1	20	2
240	1	1	3	1236	1	5	3	2232	1	9	3	3228	1	13	3	4224	1	17	3
252	1	2	3	1248	1	6	3	2244	1	10	3	3240	1	14	3	4236	1	18	3
264	1	3	3	1260	1	7	3	2256	1	11	3	3252	1	15	3	4248	1	19	3
276	1	4	3	1272	1	8	3	2268	1	12	3	3264	1	16	3	4260	1	20	3
288	1	1	4	1284	1	5	4	2280	1	9	4	3276	1	13	4	4272	1	17	4
300	1	2	4	1296	1	6	4	2292	1	10	4	3288	1	14	4	4284	1	18	4
312	1	3	4	1308	1	7	4	2304	1	11	4	3300	1	15	4	4296	1	19	4
324	1	4	4	1320	1	8	4	2316	1	12	4	3312	1	16	4	4308	1	20	4
336	2	1	1	1332	2	5	1	2328	2	9	1	3324	2	13	1	4320	2	17	1
348	2	2	1	1344	2	6	1	2340	2	10	1	3336	2	14	1	4332	2	18	1
360	2	3	1	1356	2	7	1	2352	2	11	1	3348	2	15	1	4344	2	19	1
372	2	4	1	1368	2	8	1	2364	2	12	1	3360	2	16	1	4356	2	20	1
384	2	1	2	1380	2	5	2	2376	2	9	2	3372	2	13	2	4368	2	17	2
396	2	2	2	1392	2	6	2	2388	2	10	2	3384	2	14	2	4380	2	18	2
408	2	3	2	1404	2	7	2	2400	2	11	2	3396	2	15	2	4392	2	19	2
420	2	4	2	1416	2	8	2	2412	2	12	2	3408	2	16	2	4404	2	20	2
432	2	1	3	1428	2	5	3	2424	2	9	3	3420	2	13	3	4416	2	17	3
444	2	2	3	1440	2	6	3	2436	2	10	3	3432	2	14	3	4428	2	18	3
456	2	3	3	1452	2	7	3	2448	2	11	3	3444	2	15	3	4440	2	19	3
468	2	4	3	1464	2	8	3	2460	2	12	3	3456	2	16	3	4452	2	20	3
480	2	1	4	1476	2	5	4	2472	2	9	4	3468	2	13	4	4464	2	17	4
492	2	2	4	1488	2	6	4	2484	2	10	4	3480	2	14	4	4476	2	18	4
504	2	3	4	1500	2	7	4	2496	2	11	4	3492	2	15	4	4488	2	19	4
516	2	4	4	1512	2	8	4	2508	2	12	4	3504	2	16	4	4500	2	20	4
528	3	1	1	1524	3	3	1	2520	3	5	1	3516	3	7	1	4512	3	9	1
540	3	2	1	1536	3	4	1	2532	3	6	1	3528	3	8	1	4524	3	10	1
552	3	1	2	1548	3	3	2	2544	3	5	2	3540	3	7	2	4536	3	9	2
564	3	2	2	1560	3	4	2	2556	3	6	2	3552	3	8	2	4548	3	10	2
576	4	1	1	1572	4	3	1	2568	4	5	1	3564	4	7	1	4560	4	9	1
588	4	2	1	1584	4	4	1	2580	4	6	1	3576	4	8	1	4572	4	10	1
600	4	1	2	1596	4	3	2	2592	4	5	2	3588	4	7	2	4584	4	9	2
612	4	2	2	1608	4	4	2	2604	4	6	2	3600	4	8	2	4596	4	10	2
624	5	1	1	1620	5	3	1	2616	5	5	1	3612	5	7	1	4608	5	9	1
636	5	2	1	1632	5	4	1	2628	5	6	1	3624	5	8	1	4620	5	10	1

⇓ continued next page

TABLE 30-1. MODIS SCIENCE DAY GROUP PACKET 1 DATA FIELD

415Wx12B ***Day Packet 1 contains IFOV 1-5 data (4980 bits). See Figure 30-9 for interband relationship with ground pattern.***

IFOV 1 (1km)

Pkt Start Bit	Band	Det	Sample
648	5	1	2
660	5	2	2
672	6	1	1
684	6	2	1
696	6	1	2
708	6	2	2
720	7	1	1
732	7	2	1
744	7	1	2
756	7	2	2
768	8	1	1
780	9	1	1
792	10	1	1
804	11	1	1
816	12	1	1
828	13L	1	1
840	13H	1	1
852	14L	1	1
864	14H	1	1
876	15	1	1
888	16	1	1
900	17	1	1
912	18	1	1
924	19	1	1
936	20	1	1
948	21	1	1
960	22	1	1
972	23	1	1
984	24	1	1
996	25	1	1
1008	26	1	1
1020	27	1	1
1032	28	1	1
1044	29	1	1
1056	30	1	1
1068	31	1	1
1080	32	1	1
1092	33	1	1
1104	34	1	1
1116	35	1	1
1128	36	1	1

IFOV 2 (1km)

Pkt Start Bit	Band	Det	Sample
1644	5	3	2
1656	5	4	2
1668	6	3	1
1680	6	4	1
1692	6	3	2
1704	6	4	2
1716	7	3	1
1728	7	4	1
1740	7	3	2
1752	7	4	2
1764	8	2	1
1776	9	2	1
1788	10	2	1
1800	11	2	1
1812	12	2	1
1824	13L	2	1
1836	13H	2	1
1848	14L	2	1
1860	14H	2	1
1872	15	2	1
1884	16	2	1
1896	17	2	1
1908	18	2	1
1920	19	2	1
1932	20	2	1
1944	21	2	1
1956	22	2	1
1968	23	2	1
1980	24	2	1
1992	25	2	1
2004	26	2	1
2016	27	2	1
2028	28	2	1
2040	29	2	1
2052	30	2	1
2064	31	2	1
2076	32	2	1
2088	33	2	1
2100	34	2	1
2112	35	2	1
2124	36	2	1

IFOV 3 (1km)

Pkt Start Bit	Band	Det	Sample
2640	5	5	2
2652	5	6	2
2664	6	5	1
2676	6	6	1
2688	6	5	2
2700	6	6	2
2712	7	5	1
2724	7	6	1
2736	7	5	2
2748	7	6	2
2760	8	3	1
2772	9	3	1
2784	10	3	1
2796	11	3	1
2808	12	3	1
2820	13L	3	1
2832	13H	3	1
2844	14L	3	1
2856	14H	3	1
2868	15	3	1
2880	16	3	1
2892	17	3	1
2904	18	3	1
2916	19	3	1
2928	20	3	1
2940	21	3	1
2952	22	3	1
2964	23	3	1
2976	24	3	1
2988	25	3	1
3000	26	3	1
3012	27	3	1
3024	28	3	1
3036	29	3	1
3048	30	3	1
3060	31	3	1
3072	32	3	1
3084	33	3	1
3096	34	3	1
3108	35	3	1
3120	36	3	1

IFOV 4 (1km)

Pkt Start Bit	Band	Det	Sample
3636	5	7	2
3648	5	8	2
3660	6	7	1
3672	6	8	1
3684	6	7	2
3696	6	8	2
3708	7	7	1
3720	7	8	1
3732	7	7	2
3744	7	8	2
3756	8	4	1
3768	9	4	1
3780	10	4	1
3792	11	4	1
3804	12	4	1
3816	13L	4	1
3828	13H	4	1
3840	14L	4	1
3852	14H	4	1
3864	15	4	1
3876	16	4	1
3888	17	4	1
3900	18	4	1
3912	19	4	1
3924	20	4	1
3936	21	4	1
3948	22	4	1
3960	23	4	1
3972	24	4	1
3984	25	4	1
3996	26	4	1
4008	27	4	1
4020	28	4	1
4032	29	4	1
4044	30	4	1
4056	31	4	1
4068	32	4	1
4080	33	4	1
4092	34	4	1
4104	35	4	1
4116	36	4	1

IFOV 5 (1km) *5/97*

Pkt Start Bit	Band	Det	Sample
4632	5	9	2
4644	5	10	2
4656	6	9	1
4668	6	10	1
4680	6	9	2
4692	6	10	2
4704	7	9	1
4716	7	10	1
4728	7	9	2
4740	7	10	2
4752	8	5	1
4764	9	5	1
4776	10	5	1
4788	11	5	1
4800	12	5	1
4812	13L	5	1
4824	13H	5	1
4836	14L	5	1
4848	14H	5	1
4860	15	5	1
4872	16	5	1
4884	17	5	1
4896	18	5	1
4908	19	5	1
4920	20	5	1
4932	21	5	1
4944	22	5	1
4956	23	5	1
4968	24	5	1
4980	25	5	1
4992	26	5	1
5004	27	5	1
5016	28	5	1
5028	29	5	1
5040	30	5	1
5052	31	5	1
5064	32	5	1
5076	33	5	1
5088	34	5	1
5100	35	5	1
5112	36	5	1

• 1st column is packet start bit for entry **• All items have 12 bits** **• Total Field = 4980 bits** **• Last Field bit in Pkt-> 5123**

TABLE 30-1. MODIS SCIENCE DAY GROUP PACKET 1 DATA FIELD

415Wx12B ***Day Packet 1 contains IFOV 1-5 data (4980 bits). See Figure 30-9 for interband relationship with ground pattern.***

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IFOV 1 (1km)				IFOV 2 (1km)				IFOV 3 (1km)				IFOV 4 (1km)				IFOV 5 (1km)			
Pkt Start Bit	Band	Det	Sample	Pkt Start Bit	Band	Det	Sample	Pkt Start Bit	Band	Det	Sample	Pkt Start Bit	Band	Det	Sample	Pkt Start Bit	Band	Det	Sample

T30-1. Change History

1. 9/17/96 Change title to Group vs Segment terminology.

TABLE 30-2. MODIS SCIENCE DAY GROUP PACKET 2 DATA FIELD

415Wx12B ***Day Packet 2 contains IFOV 6-10 data (4980 bits). See Figure 30-9 for interband relationship with ground pattern.***

IFOV 6 (1km)

Pkt Start Bit	Band	Det	Sample
144	1	21	1
156	1	22	1
168	1	23	1
180	1	24	1
192	1	21	2
204	1	22	2
216	1	23	2
228	1	24	2
240	1	21	3
252	1	22	3
264	1	24	3
276	1	23	3
288	1	21	4
300	1	22	4
312	1	23	4
324	1	24	4
336	2	21	1
348	2	22	1
360	2	23	1
372	2	24	1
384	2	21	2
396	2	22	2
408	2	23	2
420	2	24	2
432	2	21	3
444	2	22	3
456	2	24	3
468	2	23	3
480	2	21	4
492	2	22	4
504	2	23	4
516	2	24	4
528	3	11	1
540	3	12	1
552	3	11	2
564	3	12	2
576	4	11	1
588	4	12	1
600	4	11	2
612	4	12	2
624	5	11	1
636	5	12	1

continued next page ⇓

IFOV 7 (1km)

Pkt Start Bit	Band	Det	Sample
1140	1	25	1
1152	1	26	1
1164	1	27	1
1176	1	28	1
1188	1	25	2
1200	1	26	2
1212	1	27	2
1224	1	28	2
1236	1	25	3
1248	1	26	3
1260	1	27	3
1272	1	28	3
1284	1	25	4
1296	1	26	4
1308	1	27	4
1320	1	28	4
1332	2	25	1
1344	2	26	1
1356	2	27	1
1368	2	28	1
1380	2	25	2
1392	2	26	2
1404	2	27	2
1416	2	28	2
1428	2	25	3
1440	2	26	3
1452	2	27	3
1464	2	28	3
1476	2	25	4
1488	2	26	4
1500	2	27	4
1512	2	28	4
1524	3	13	1
1536	3	14	1
1548	3	13	2
1560	3	14	2
1572	4	13	1
1584	4	14	1
1596	4	13	2
1608	4	14	2
1620	5	13	1
1632	5	14	1

continued next page ⇓

IFOV 8 (1km)

Pkt Start Bit	Band	Det	Sample
2136	1	29	1
2148	1	30	1
2160	1	31	1
2172	1	32	1
2184	1	29	2
2196	1	30	2
2208	1	31	2
2220	1	32	2
2232	1	29	3
2244	1	30	3
2256	1	31	3
2268	1	32	3
2280	1	29	4
2292	1	30	4
2304	1	31	4
2316	1	32	4
2328	2	29	1
2340	2	30	1
2352	2	31	1
2364	2	32	1
2376	2	29	2
2388	2	30	2
2400	2	31	2
2412	2	32	2
2424	2	29	3
2436	2	30	3
2448	2	31	3
2460	2	32	3
2472	2	29	4
2484	2	30	4
2496	2	31	4
2508	2	32	4
2520	3	15	1
2532	3	16	1
2544	3	15	2
2556	3	16	2
2568	4	15	1
2580	4	16	1
2592	4	15	2
2604	4	16	2
2616	5	15	1
2628	5	16	1

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IFOV 9 (1km)

Pkt Start Bit	Band	Det	Sample
3132	1	33	1
3144	1	34	1
3156	1	35	1
3168	1	36	1
3180	1	33	2
3192	1	34	2
3204	1	35	2
3216	1	36	2
3228	1	33	3
3240	1	34	3
3252	1	35	3
3264	1	36	3
3276	1	33	4
3288	1	34	4
3300	1	35	4
3312	1	36	4
3324	2	33	1
3336	2	34	1
3348	2	35	1
3360	2	36	1
3372	2	33	2
3384	2	34	2
3396	2	35	2
3408	2	36	2
3420	2	33	3
3432	2	34	3
3444	2	35	3
3456	2	36	3
3468	2	33	4
3480	2	34	4
3492	2	35	4
3504	2	36	4
3516	3	7	1
3528	3	8	1
3540	3	7	2
3552	3	8	2
3564	4	17	1
3576	4	18	1
3588	4	17	2
3600	4	18	2
3612	5	17	1
3624	5	18	1

continued next page ⇓

IFOV 10 (1km) 5/97

Pkt Start Bit	Band	Det	Sample
4128	1	37	1
4140	1	38	1
4152	1	39	1
4164	1	40	1
4176	1	37	2
4188	1	38	2
4200	1	39	2
4212	1	40	2
4224	1	37	3
4236	1	38	3
4248	1	39	3
4260	1	40	3
4272	1	37	4
4284	1	38	4
4296	1	39	4
4308	1	40	4
4320	2	37	1
4332	2	38	1
4344	2	39	1
4356	2	40	1
4368	2	37	2
4380	2	38	2
4392	2	39	2
4404	2	40	2
4416	2	37	3
4428	2	38	3
4440	2	39	3
4452	2	40	3
4464	2	37	4
4476	2	38	4
4488	2	39	4
4500	2	40	4
4512	3	19	1
4524	3	20	1
4536	3	19	2
4548	3	20	2
4560	4	19	1
4572	4	20	1
4584	4	19	2
4596	4	20	2
4608	5	19	1
4620	5	20	1

TABLE 30-2. MODIS SCIENCE DAY GROUP PACKET 2 DATA FIELD

415Wx12B ***Day Packet 2 contains IFOV 6-10 data (4980 bits). See Figure 30-9 for interband relationship with ground pattern.***

IFOV 6 (1km)

Pkt Start Bit	Band	Det	Sample
648	5	11	2
660	5	12	2
672	6	11	1
684	6	12	1
696	6	11	2
708	6	12	2
720	7	11	1
732	7	12	1
744	7	11	2
756	7	12	2
768	8	6	1
780	9	6	1
792	10	6	1
804	11	6	1
816	12	6	1
828	13L	6	1
840	13H	6	1
852	14L	6	1
864	14H	6	1
876	15	6	1
888	16	6	1
900	17	6	1
912	18	6	1
924	19	6	1
936	20	6	1
948	21	6	1
960	22	6	1
972	23	6	1
984	24	6	1
996	25	6	1
1008	26	6	1
1020	27	6	1
1032	28	6	1
1044	29	6	1
1056	30	6	1
1068	31	6	1
1080	32	6	1
1092	33	6	1
1104	34	6	1
1116	35	6	1
1128	36	6	1

IFOV 7 (1km)

Pkt Start Bit	Band	Det	Sample
1644	5	13	2
1656	5	14	2
1668	6	13	1
1680	6	14	1
1692	6	13	2
1704	6	14	2
1716	7	13	1
1728	7	14	1
1740	7	13	2
1752	7	14	2
1764	8	7	1
1776	9	7	1
1788	10	7	1
1800	11	7	1
1812	12	7	1
1824	13L	7	1
1836	13H	7	1
1848	14L	7	1
1860	14H	7	1
1872	15	7	1
1884	16	7	1
1896	17	7	1
1908	18	7	1
1920	19	7	1
1932	20	7	1
1944	21	7	1
1956	22	7	1
1968	23	7	1
1980	24	7	1
1992	25	7	1
2004	26	7	1
2016	27	7	1
2028	28	7	1
2040	29	7	1
2052	30	7	1
2064	31	7	1
2076	32	7	1
2088	33	7	1
2100	34	7	1
2112	35	7	1
2124	36	7	1

IFOV 8 (1km)

Pkt Start Bit	Band	Det	Sample
2640	5	15	2
2652	5	16	2
2664	6	15	1
2676	6	16	1
2688	6	15	2
2700	6	16	2
2712	7	15	1
2724	7	16	1
2736	7	15	2
2748	7	16	2
2760	8	8	1
2772	9	8	1
2784	10	8	1
2796	11	8	1
2808	12	8	1
2820	13L	8	1
2832	13H	8	1
2844	14L	8	1
2856	14H	8	1
2868	15	8	1
2880	16	8	1
2892	17	8	1
2904	18	8	1
2916	19	8	1
2928	20	8	1
2940	21	8	1
2952	22	8	1
2964	23	8	1
2976	24	8	1
2988	25	8	1
3000	26	8	1
3012	27	8	1
3024	28	8	1
3036	29	8	1
3048	30	8	1
3060	31	8	1
3072	32	8	1
3084	33	8	1
3096	34	8	1
3108	35	8	1
3120	36	8	1

IFOV 9 (1km)

Pkt Start Bit	Band	Det	Sample
3636	5	17	2
3648	5	18	2
3660	6	17	1
3672	6	18	1
3684	6	17	2
3696	6	18	2
3708	7	17	1
3720	7	18	1
3732	7	17	2
3744	7	18	2
3756	8	9	1
3768	9	9	1
3780	10	9	1
3792	11	9	1
3804	12	9	1
3816	13L	9	1
3828	13H	9	1
3840	14L	9	1
3852	14H	9	1
3864	15	9	1
3876	16	9	1
3888	17	9	1
3900	18	9	1
3912	19	9	1
3924	20	9	1
3936	21	9	1
3948	22	9	1
3960	23	9	1
3972	24	9	1
3984	25	9	1
3996	26	9	1
4008	27	9	1
4020	28	9	1
4032	29	9	1
4044	30	9	1
4056	31	9	1
4068	32	9	1
4080	33	9	1
4092	34	9	1
4104	35	9	1
4116	36	9	1

IFOV 10 (1km) *5/97*

Pkt Start Bit	Band	Det	Sample
4632	5	19	2
4644	5	20	2
4656	6	19	1
4668	6	20	1
4680	6	19	2
4692	6	20	2
4704	7	19	1
4716	7	20	1
4728	7	19	2
4740	7	20	2
4752	8	10	1
4764	9	10	1
4776	10	10	1
4788	11	10	1
4800	12	10	1
4812	13L	10	1
4824	13H	10	1
4836	14L	10	1
4848	14H	10	1
4860	15	10	1
4872	16	10	1
4884	17	10	1
4896	18	10	1
4908	19	10	1
4920	20	10	1
4932	21	10	1
4944	22	10	1
4956	23	10	1
4968	24	10	1
4980	25	10	1
4992	26	10	1
5004	27	10	1
5016	28	10	1
5028	29	10	1
5040	30	10	1
5052	31	10	1
5064	32	10	1
5076	33	10	1
5088	34	10	1
5100	35	10	1
5112	36	10	1

• 1st column is packet start bit for entry **• All items have 12 bits** **• Total Field = 4980 bits** **• Last Field bit in Pkt-> 5123**

TABLE 30-2. MODIS SCIENCE DAY GROUP PACKET 2 DATA FIELD

415Wx12B ***Day Packet 2 contains IFOV 6-10 data (4980 bits). See Figure 30-9 for interband relationship with ground pattern.***

IFOV 6 (1km)

Pkt Start Bit	Band	Det	Sample

IFOV 7 (1km)

Pkt Start Bit	Band	Det	Sample

IFOV 8 (1km)

Pkt Start Bit	Band	Det	Sample

IFOV 9 (1km)

Pkt Start Bit	Band	Det	Sample

IFOV 10 (1km) *5/97*

Pkt Start Bit	Band	Det	Sample

T30-2 Change History

1. 9/17/96 Change title to Group vs Segment terminology.

TABLE 30-3. MODIS SCIENCE NIGHT GROUP PACKET DATA FIELD

171Wx12B=2052 bits

See Figure 30-9 for interband relationship with ground pattern.

IFOV#1 (1km)

Pkt Start Bit	Band	Det	Sample
144	20	1	1
156	21	1	1
168	22	1	1
180	23	1	1
192	24	1	1
204	25	1	1
216	26	1	1
228	27	1	1
240	28	1	1
252	29	1	1
264	30	1	1
276	31	1	1
288	32	1	1
300	33	1	1
312	34	1	1
324	35	1	1
336	36	1	1

IFOV#2 (1km)

Pkt Start Bit	Band	Det	Sample
348	20	2	1
360	21	2	1
372	22	2	1
384	23	2	1
396	24	2	1
408	25	2	1
420	26	2	1
432	27	2	1
444	28	2	1
456	29	2	1
468	30	2	1
480	31	2	1
492	32	2	1
504	33	2	1
516	34	2	1
528	35	2	1
540	36	2	1

IFOV#3 (1km)

Pkt Start Bit	Band	Det	Sample
552	20	3	1
564	21	3	1
576	22	3	1
588	23	3	1
600	24	3	1
612	25	3	1
624	26	3	1
636	27	3	1
648	28	3	1
660	29	3	1
672	30	3	1
684	31	3	1
696	32	3	1
708	33	3	1
720	34	3	1
732	35	3	1
744	36	3	1

IFOV#4 (1km)

Pkt Start Bit	Band	Det	Sample
756	20	4	1
768	21	4	1
780	22	4	1
792	23	4	1
804	24	4	1
816	25	4	1
828	26	4	1
840	27	4	1
852	28	4	1
864	29	4	1
876	30	4	1
888	31	4	1
900	32	4	1
912	33	4	1
924	34	4	1
936	35	4	1
948	36	4	1

IFOV#5 (1km) *5/97*

Pkt Start Bit	Band	Det	Sample
960	20	5	1
972	21	5	1
984	22	5	1
996	23	5	1
1008	24	5	1
1020	25	5	1
1032	26	5	1
1044	27	5	1
1056	28	5	1
1068	29	5	1
1080	30	5	1
1092	31	5	1
1104	32	5	1
1116	33	5	1
1128	34	5	1
1140	35	5	1
1152	36	5	1

IFOV#6 (1km)

Pkt Start Bit	Band	Det	Sample
1164	20	6	1
1176	21	6	1
1188	22	6	1
1200	23	6	1
1212	24	6	1
1224	25	6	1
1236	26	6	1
1248	27	6	1
1260	28	6	1
1272	29	6	1
1284	30	6	1
1296	31	6	1
1308	32	6	1
1320	33	6	1
1332	34	6	1
1344	35	6	1
1356	36	6	1

IFOV#7 (1km)

Pkt Start Bit	Band	Det	Sample
1368	20	7	1
1380	21	7	1
1392	22	7	1
1404	23	7	1
1416	24	7	1
1428	25	7	1
1440	26	7	1
1452	27	7	1
1464	28	7	1
1476	29	7	1
1488	30	7	1
1500	31	7	1
1512	32	7	1
1524	33	7	1
1536	34	7	1
1548	35	7	1
1560	36	7	1

IFOV#8 (1km)

Pkt Start Bit	Band	Det	Sample
1572	20	8	1
1584	21	8	1
1596	22	8	1
1608	23	8	1
1620	24	8	1
1632	25	8	1
1644	26	8	1
1656	27	8	1
1668	28	8	1
1680	29	8	1
1692	30	8	1
1704	31	8	1
1716	32	8	1
1728	33	8	1
1740	34	8	1
1752	35	8	1
1764	36	8	1

IFOV#9 (1km)

Pkt Start Bit	Band	Det	Sample
1776	20	9	1
1788	21	9	1
1800	22	9	1
1812	23	9	1
1824	24	9	1
1836	25	9	1
1848	26	9	1
1860	27	9	1
1872	28	9	1
1884	29	9	1
1896	30	9	1
1908	31	9	1
1920	32	9	1
1932	33	9	1
1944	34	9	1
1956	35	9	1
1968	36	9	1

IFOV#10 (1km)

Pkt Start Bit	Band	Det	Sample
1980	20	10	1
1992	21	10	1
2004	22	10	1
2016	23	10	1
2028	24	10	1
2040	25	10	1
2052	26	10	1
2064	27	10	1
2076	28	10	1
2088	29	10	1
2100	30	10	1
2112	31	10	1
2124	32	10	1
2136	33	10	1
2148	34	10	1
2160	35	10	1
2172	36	10	1

• 1st column is packet start bit for entry

• All items have 12 bits

• Total Field = 2052 bits with 12 fill bits

• 2195 <--Last Field bit in Pkt with added 12 fill bits

T30-3 Change History

1. 9/17/96 Change title to Group vs Segment terminology.

TABLE 30-4. MODIS ENGINEERING GROUP 1 PACKET 1 DATA FIELD
FPA DCR Offsets (4400 bits)

Sort by Pkt Start Bit — 550 words x 8 bits

Pkt Start Bit	Memory Table Word Offset	Band	Det	DCR Offset, Hex	PC Comments
144	0	1	1	XX	
152	1	1	2	XX	
160	2	1	3	XX	
168	3	1	4	XX	
176	4	2	1	XX	
184	5	2	2	XX	
192	6	2	3	XX	
200	7	2	4	XX	
208	8	3	1	XX	
216	9	3	2	XX	
224	10	4	1	XX	
232	11	4	2	XX	
240	12	5	1	XX	
248	13	5	2	XX	
256	14	6	1	XX	
264	15	6	2	XX	
272	16	7	1	XX	
280	17	7	2	XX	
288	18	8	1	XX	
296	19	9	1	XX	
304	20	10	1	XX	
312	21	11	1	XX	
320	22	12	1	XX	
328	23	13L	1	XX	
336	24	13H	1	XX	
344	25	14L	1	XX	
352	26	14H	1	XX	
360	27	15	1	XX	
368	28	16	1	XX	
376	29	17	1	XX	
384	30	18	1	XX	
392	31	19	1	XX	
400	32	20	1	XX	
408	33	21	1	XX	
416	34	22	1	XX	
424	35	23	1	XX	
432	36	24	1	XX	
440	37	25	1	XX	
448	38	26	1	XX	
456	39	27	1	XX	
464	40	28	1	XX	
472	41	29	1	XX	
480	42	30	1	XX	
488	43	31	1	XX	postamp
496	44	31	1	XX	preamp
504	45	32	1	XX	postamp
512	46	32	1	XX	preamp
520	47	33	1	XX	postamp
528	48	33	1	XX	preamp
536	49	34	1	XX	postamp
544	50	34	1	XX	preamp
552	51	35	1	XX	postamp
560	52	35	1	XX	preamp
568	53	36	1	XX	postamp
576	54	36	1	XX	preamp
584	55	1	5	XX	
592	56	1	6	XX	

Reference Sort by Band/Det — 5/97

Pkt Start Bit	Memory Table Word Offset	Band	Det	PC Comments
144	0	1	1	
152	1	1	2	
160	2	1	3	
168	3	1	4	
584	55	1	5	
592	56	1	6	
600	57	1	7	
608	58	1	8	
1024	110	1	9	
1032	111	1	10	
1040	112	1	11	
1048	113	1	12	
1464	165	1	13	
1472	166	1	14	
1480	167	1	15	
1488	168	1	16	
1904	220	1	17	
1912	221	1	18	
1920	222	1	19	
1928	223	1	20	
2344	275	1	21	
2352	276	1	22	
2360	277	1	23	
2368	278	1	24	
2784	330	1	25	
2792	331	1	26	
2800	332	1	27	
2808	333	1	28	
3224	385	1	29	
3232	386	1	30	
3240	387	1	31	
3248	388	1	32	
3664	440	1	33	
3672	441	1	34	
3680	442	1	35	
3688	443	1	36	
4104	495	1	37	
4112	496	1	38	
4120	497	1	39	
4128	498	1	40	
176	4	2	1	
184	5	2	2	
192	6	2	3	
200	7	2	4	
616	59	2	5	
624	60	2	6	
632	61	2	7	
640	62	2	8	
1056	114	2	9	
1064	115	2	10	
1072	116	2	11	
1080	117	2	12	
1496	169	2	13	
1504	170	2	14	
1512	171	2	15	
1520	172	2	16	
1936	224	2	17	

TABLE 30-4. MODIS ENGINEERING GROUP 1 PACKET 1 DATA FIELD
FPA DCR Offsets (4400 bits)

Sort by Pkt Start Bit — 550 words x 8 bits

Pkt Start Bit	Memory Table Word Offset	Band	Det	DCR Offset, Hex	PC Comments
600	57	1	7	XX	
608	58	1	8	XX	
616	59	2	5	XX	
624	60	2	6	XX	
632	61	2	7	XX	
640	62	2	8	XX	
648	63	3	3	XX	
656	64	3	4	XX	
664	65	4	3	XX	
672	66	4	4	XX	
680	67	5	3	XX	
688	68	5	4	XX	
696	69	6	3	XX	
704	70	6	4	XX	
712	71	7	3	XX	
720	72	7	4	XX	
728	73	8	2	XX	
736	74	9	2	XX	
744	75	10	2	XX	
752	76	11	2	XX	
760	77	12	2	XX	
768	78	13L	2	XX	
776	79	13H	2	XX	
784	80	14L	2	XX	
792	81	14H	2	XX	
800	82	15	2	XX	
808	83	16	2	XX	
816	84	17	2	XX	
824	85	18	2	XX	
832	86	19	2	XX	
840	87	20	2	XX	
848	88	21	2	XX	
856	89	22	2	XX	
864	90	23	2	XX	
872	91	24	2	XX	
880	92	25	2	XX	
888	93	26	2	XX	
896	94	27	2	XX	
904	95	28	2	XX	
912	96	29	2	XX	
920	97	30	2	XX	
928	98	31	2	XX	postamp
936	99	31	2	XX	preamp
944	100	32	2	XX	postamp
952	101	32	2	XX	preamp
960	102	33	2	XX	postamp
968	103	33	2	XX	preamp
976	104	34	2	XX	postamp
984	105	34	2	XX	preamp
992	106	35	2	XX	postamp
1000	107	35	2	XX	preamp
1008	108	36	2	XX	postamp
1016	109	36	2	XX	preamp
1024	110	1	9	XX	
1032	111	1	10	XX	
1040	112	1	11	XX	
1048	113	1	12	XX	

Reference Sort by Band/Det — 5/97

Pkt Start Bit	Memory Table Word Offset	Band	Det	PC Comments
1944	225	2	18	
1952	226	2	19	
1960	227	2	20	
2376	279	2	21	
2384	280	2	22	
2392	281	2	23	
2400	282	2	24	
2816	334	2	25	
2824	335	2	26	
2832	336	2	27	
2840	337	2	28	
3256	389	2	29	
3264	390	2	30	
3272	391	2	31	
3280	392	2	32	
3696	444	2	33	
3704	445	2	34	
3712	446	2	35	
3720	447	2	36	
4136	499	2	37	
4144	500	2	38	
4152	501	2	39	
4160	502	2	40	
208	8	3	1	
216	9	3	2	
648	63	3	3	
656	64	3	4	
1088	118	3	5	
1096	119	3	6	
1528	173	3	7	
1536	174	3	8	
1968	228	3	9	
1976	229	3	10	
2408	283	3	11	
2416	284	3	12	
2848	338	3	13	
2856	339	3	14	
3288	393	3	15	
3296	394	3	16	
3728	448	3	17	
3736	449	3	18	
4168	503	3	19	
4176	504	3	20	
224	10	4	1	
232	11	4	2	
664	65	4	3	
672	66	4	4	
1104	120	4	5	
1112	121	4	6	
1544	175	4	7	
1552	176	4	8	
1984	230	4	9	
1992	231	4	10	
2424	285	4	11	
2432	286	4	12	
2864	340	4	13	
2872	341	4	14	

TABLE 30-4. MODIS ENGINEERING GROUP 1 PACKET 1 DATA FIELD
FPA DCR Offsets (4400 bits)

Sort by Pkt Start Bit — 550 words x 8 bits

Pkt Start Bit	Memory Table Word Offset	Band	Det	DCR Offset, Hex	PC Comments
1056	114	2	9	XX	
1064	115	2	10	XX	
1072	116	2	11	XX	
1080	117	2	12	XX	
1088	118	3	5	XX	
1096	119	3	6	XX	
1104	120	4	5	XX	
1112	121	4	6	XX	
1120	122	5	5	XX	
1128	123	5	6	XX	
1136	124	6	5	XX	
1144	125	6	6	XX	
1152	126	7	5	XX	
1160	127	7	6	XX	
1168	128	8	3	XX	
1176	129	9	3	XX	
1184	130	10	3	XX	
1192	131	11	3	XX	
1200	132	12	3	XX	
1208	133	13L	3	XX	
1216	134	13H	3	XX	
1224	135	14L	3	XX	
1232	136	14H	3	XX	
1240	137	15	3	XX	
1248	138	16	3	XX	
1256	139	17	3	XX	
1264	140	18	3	XX	
1272	141	19	3	XX	
1280	142	20	3	XX	
1288	143	21	3	XX	
1296	144	22	3	XX	
1304	145	23	3	XX	
1312	146	24	3	XX	
1320	147	25	3	XX	
1328	148	26	3	XX	
1336	149	27	3	XX	
1344	150	28	3	XX	
1352	151	29	3	XX	
1360	152	30	3	XX	
1368	153	31	3	XX	postamp
1376	154	31	3	XX	preamp
1384	155	32	3	XX	postamp
1392	156	32	3	XX	preamp
1400	157	33	3	XX	postamp
1408	158	33	3	XX	preamp
1416	159	34	3	XX	postamp
1424	160	34	3	XX	preamp
1432	161	35	3	XX	postamp
1440	162	35	3	XX	preamp
1448	163	36	3	XX	postamp
1456	164	36	3	XX	preamp
1464	165	1	13	XX	
1472	166	1	14	XX	
1480	167	1	15	XX	
1488	168	1	16	XX	
1496	169	2	13	XX	
1504	170	2	14	XX	

Reference Sort by Band/Det — 5/97

Pkt Start Bit	Memory Table Word Offset	Band	Det	PC Comments
3304	395	4	15	
3312	396	4	16	
3744	450	4	17	
3752	451	4	18	
4184	505	4	19	
4192	506	4	20	
240	12	5	1	
248	13	5	2	
680	67	5	3	
688	68	5	4	
1120	122	5	5	
1128	123	5	6	
1560	177	5	7	
1568	178	5	8	
2000	232	5	9	
2008	233	5	10	
2440	287	5	11	
2448	288	5	12	
2880	342	5	13	
2888	343	5	14	
3320	397	5	15	
3328	398	5	16	
3760	452	5	17	
3768	453	5	18	
4200	507	5	19	
4208	508	5	20	
256	14	6	1	
264	15	6	2	
696	69	6	3	
704	70	6	4	
1136	124	6	5	
1144	125	6	6	
1576	179	6	7	
1584	180	6	8	
2016	234	6	9	
2024	235	6	10	
2456	289	6	11	
2464	290	6	12	
2896	344	6	13	
2904	345	6	14	
3336	399	6	15	
3344	400	6	16	
3776	454	6	17	
3784	455	6	18	
4216	509	6	19	
4224	510	6	20	
272	16	7	1	
280	17	7	2	
712	71	7	3	
720	72	7	4	
1152	126	7	5	
1160	127	7	6	
1592	181	7	7	
1600	182	7	8	
2032	236	7	9	
2040	237	7	10	
2472	291	7	11	

TABLE 30-4. MODIS ENGINEERING GROUP 1 PACKET 1 DATA FIELD

FPA DCR Offsets (4400 bits)

Sort by Pkt Start Bit — 550 words x 8 bits

Pkt Start Bit	Memory Table Word Offset	Band	Det	DCR Offset, Hex	PC Comments
1512	171	2	15	XX	
1520	172	2	16	XX	
1528	173	3	7	XX	
1536	174	3	8	XX	
1544	175	4	7	XX	
1552	176	4	8	XX	
1560	177	5	7	XX	
1568	178	5	8	XX	
1576	179	6	7	XX	
1584	180	6	8	XX	
1592	181	7	7	XX	
1600	182	7	8	XX	
1608	183	8	4	XX	
1616	184	9	4	XX	
1624	185	10	4	XX	
1632	186	11	4	XX	
1640	187	12	4	XX	
1648	188	13L	4	XX	
1656	189	13H	4	XX	
1664	190	14L	4	XX	
1672	191	14H	4	XX	
1680	192	15	4	XX	
1688	193	16	4	XX	
1696	194	17	4	XX	
1704	195	18	4	XX	
1712	196	19	4	XX	
1720	197	20	4	XX	
1728	198	21	4	XX	
1736	199	22	4	XX	
1744	200	23	4	XX	
1752	201	24	4	XX	
1760	202	25	4	XX	
1768	203	26	4	XX	
1776	204	27	4	XX	
1784	205	28	4	XX	
1792	206	29	4	XX	
1800	207	30	4	XX	
1808	208	31	4	XX	postamp
1816	209	31	4	XX	preamp
1824	210	32	4	XX	postamp
1832	211	32	4	XX	preamp
1840	212	33	4	XX	postamp
1848	213	33	4	XX	preamp
1856	214	34	4	XX	postamp
1864	215	34	4	XX	preamp
1872	216	35	4	XX	postamp
1880	217	35	4	XX	preamp
1888	218	36	4	XX	postamp
1896	219	36	4	XX	preamp
1904	220	1	17	XX	
1912	221	1	18	XX	
1920	222	1	19	XX	
1928	223	1	20	XX	
1936	224	2	17	XX	
1944	225	2	18	XX	
1952	226	2	19	XX	
1960	227	2	20	XX	

Reference Sort by Band/Det — 5/97

Pkt Start Bit	Memory Table Word Offset	Band	Det	PC Comments
2480	292	7	12	
2912	346	7	13	
2920	347	7	14	
3352	401	7	15	
3360	402	7	16	
3792	456	7	17	
3800	457	7	18	
4232	511	7	19	
4240	512	7	20	
288	18	8	1	
728	73	8	2	
1168	128	8	3	
1608	183	8	4	
2048	238	8	5	
2488	293	8	6	
2928	348	8	7	
3368	403	8	8	
3808	458	8	9	
4248	513	8	10	
296	19	9	1	
736	74	9	2	
1176	129	9	3	
1616	184	9	4	
2056	239	9	5	
2496	294	9	6	
2936	349	9	7	
3376	404	9	8	
3816	459	9	9	
4256	514	9	10	
304	20	10	1	
744	75	10	2	
1184	130	10	3	
1624	185	10	4	
2064	240	10	5	
2504	295	10	6	
2944	350	10	7	
3384	405	10	8	
3824	460	10	9	
4264	515	10	10	
312	21	11	1	
752	76	11	2	
1192	131	11	3	
1632	186	11	4	
2072	241	11	5	
2512	296	11	6	
2952	351	11	7	
3392	406	11	8	
3832	461	11	9	
4272	516	11	10	
320	22	12	1	
760	77	12	2	
1200	132	12	3	
1640	187	12	4	
2080	242	12	5	
2520	297	12	6	
2960	352	12	7	
3400	407	12	8	

TABLE 30-4. MODIS ENGINEERING GROUP 1 PACKET 1 DATA FIELD

FPA DCR Offsets (4400 bits)

Sort by Pkt Start Bit — 550 words x 8 bits

Pkt Start Bit	Memory Table Word Offset	Band	Det	DCR Offset, Hex	PC Comments
1968	228	3	9	XX	
1976	229	3	10	XX	
1984	230	4	9	XX	
1992	231	4	10	XX	
2000	232	5	9	XX	
2008	233	5	10	XX	
2016	234	6	9	XX	
2024	235	6	10	XX	
2032	236	7	9	XX	
2040	237	7	10	XX	
2048	238	8	5	XX	
2056	239	9	5	XX	
2064	240	10	5	XX	
2072	241	11	5	XX	
2080	242	12	5	XX	
2088	243	13L	5	XX	
2096	244	13H	5	XX	
2104	245	14L	5	XX	
2112	246	14H	5	XX	
2120	247	15	5	XX	
2128	248	16	5	XX	
2136	249	17	5	XX	
2144	250	18	5	XX	
2152	251	19	5	XX	
2160	252	20	5	XX	
2168	253	21	5	XX	
2176	254	22	5	XX	
2184	255	23	5	XX	
2192	256	24	5	XX	
2200	257	25	5	XX	
2208	258	26	5	XX	
2216	259	27	5	XX	
2224	260	28	5	XX	
2232	261	29	5	XX	
2240	262	30	5	XX	
2248	263	31	5	XX	postamp
2256	264	31	5	XX	preamp
2264	265	32	5	XX	postamp
2272	266	32	5	XX	preamp
2280	267	33	5	XX	postamp
2288	268	33	5	XX	preamp
2296	269	34	5	XX	postamp
2304	270	34	5	XX	preamp
2312	271	35	5	XX	postamp
2320	272	35	5	XX	preamp
2328	273	36	5	XX	postamp
2336	274	36	5	XX	preamp
2344	275	1	21	XX	
2352	276	1	22	XX	
2360	277	1	23	XX	
2368	278	1	24	XX	
2376	279	2	21	XX	
2384	280	2	22	XX	
2392	281	2	23	XX	
2400	282	2	24	XX	
2408	283	3	11	XX	
2416	284	3	12	XX	

Reference Sort by Band/Det — 5/97

Pkt Start Bit	Memory Table Word Offset	Band	Det	PC Comments
3840	462	12	9	
4280	517	12	10	
360	27	15	1	
800	82	15	2	
1240	137	15	3	
1680	192	15	4	
2120	247	15	5	
2560	302	15	6	
3000	357	15	7	
3440	412	15	8	
3880	467	15	9	
4320	522	15	10	
368	28	16	1	
808	83	16	2	
1248	138	16	3	
1688	193	16	4	
2128	248	16	5	
2568	303	16	6	
3008	358	16	7	
3448	413	16	8	
3888	468	16	9	
4328	523	16	10	
376	29	17	1	
816	84	17	2	
1256	139	17	3	
1696	194	17	4	
2136	249	17	5	
2576	304	17	6	
3016	359	17	7	
3456	414	17	8	
3896	469	17	9	
4336	524	17	10	
384	30	18	1	
824	85	18	2	
1264	140	18	3	
1704	195	18	4	
2144	250	18	5	
2584	305	18	6	
3024	360	18	7	
3464	415	18	8	
3904	470	18	9	
4344	525	18	10	
392	31	19	1	
832	86	19	2	
1272	141	19	3	
1712	196	19	4	
2152	251	19	5	
2592	306	19	6	
3032	361	19	7	
3472	416	19	8	
3912	471	19	9	
4352	526	19	10	
400	32	20	1	
840	87	20	2	
1280	142	20	3	
1720	197	20	4	
2160	252	20	5	

TABLE 30-4. MODIS ENGINEERING GROUP 1 PACKET 1 DATA FIELD

FPA DCR Offsets (4400 bits)

Sort by Pkt Start Bit — 550 words x 8 bits

Pkt Start Bit	Memory Table Word Offset	Band	Det	DCR Offset, Hex	PC Comments
2424	285	4	11	XX	
2432	286	4	12	XX	
2440	287	5	11	XX	
2448	288	5	12	XX	
2456	289	6	11	XX	
2464	290	6	12	XX	
2472	291	7	11	XX	
2480	292	7	12	XX	
2488	293	8	6	XX	
2496	294	9	6	XX	
2504	295	10	6	XX	
2512	296	11	6	XX	
2520	297	12	6	XX	
2528	298	13L	6	XX	
2536	299	13H	6	XX	
2544	300	14L	6	XX	
2552	301	14H	6	XX	
2560	302	15	6	XX	
2568	303	16	6	XX	
2576	304	17	6	XX	
2584	305	18	6	XX	
2592	306	19	6	XX	
2600	307	20	6	XX	
2608	308	21	6	XX	
2616	309	22	6	XX	
2624	310	23	6	XX	
2632	311	24	6	XX	
2640	312	25	6	XX	
2648	313	26	6	XX	
2656	314	27	6	XX	
2664	315	28	6	XX	
2672	316	29	6	XX	
2680	317	30	6	XX	
2688	318	31	6	XX	postamp
2696	319	31	6	XX	preamp
2704	320	32	6	XX	postamp
2712	321	32	6	XX	preamp
2720	322	33	6	XX	postamp
2728	323	33	6	XX	preamp
2736	324	34	6	XX	postamp
2744	325	34	6	XX	preamp
2752	326	35	6	XX	postamp
2760	327	35	6	XX	preamp
2768	328	36	6	XX	postamp
2776	329	36	6	XX	preamp
2784	330	1	25	XX	
2792	331	1	26	XX	
2800	332	1	27	XX	
2808	333	1	28	XX	
2816	334	2	25	XX	
2824	335	2	26	XX	
2832	336	2	27	XX	
2840	337	2	28	XX	
2848	338	3	13	XX	
2856	339	3	14	XX	
2864	340	4	13	XX	
2872	341	4	14	XX	

Reference Sort by Band/Det — 5/97

Pkt Start Bit	Memory Table Word Offset	Band	Det	PC Comments
2600	307	20	6	
3040	362	20	7	
3480	417	20	8	
3920	472	20	9	
4360	527	20	10	
408	33	21	1	
848	88	21	2	
1288	143	21	3	
1728	198	21	4	
2168	253	21	5	
2608	308	21	6	
3048	363	21	7	
3488	418	21	8	
3928	473	21	9	
4368	528	21	10	
416	34	22	1	
856	89	22	2	
1296	144	22	3	
1736	199	22	4	
2176	254	22	5	
2616	309	22	6	
3056	364	22	7	
3496	419	22	8	
3936	474	22	9	
4376	529	22	10	
424	35	23	1	
864	90	23	2	
1304	145	23	3	
1744	200	23	4	
2184	255	23	5	
2624	310	23	6	
3064	365	23	7	
3504	420	23	8	
3944	475	23	9	
4384	530	23	10	
432	36	24	1	
872	91	24	2	
1312	146	24	3	
1752	201	24	4	
2192	256	24	5	
2632	311	24	6	
3072	366	24	7	
3512	421	24	8	
3952	476	24	9	
4392	531	24	10	
440	37	25	1	
880	92	25	2	
1320	147	25	3	
1760	202	25	4	
2200	257	25	5	
2640	312	25	6	
3080	367	25	7	
3520	422	25	8	
3960	477	25	9	
4400	532	25	10	
448	38	26	1	
888	93	26	2	

TABLE 30-4. MODIS ENGINEERING GROUP 1 PACKET 1 DATA FIELD
FPA DCR Offsets (4400 bits)

Sort by Pkt Start Bit — 550 words x 8 bits

Pkt Start Bit	Memory Table Word Offset	Band	Det	DCR Offset, Hex	PC Comments
2880	342	5	13	XX	
2888	343	5	14	XX	
2896	344	6	13	XX	
2904	345	6	14	XX	
2912	346	7	13	XX	
2920	347	7	14	XX	
2928	348	8	7	XX	
2936	349	9	7	XX	
2944	350	10	7	XX	
2952	351	11	7	XX	
2960	352	12	7	XX	
2968	353	13L	7	XX	
2976	354	13H	7	XX	
2984	355	14L	7	XX	
2992	356	14H	7	XX	
3000	357	15	7	XX	
3008	358	16	7	XX	
3016	359	17	7	XX	
3024	360	18	7	XX	
3032	361	19	7	XX	
3040	362	20	7	XX	
3048	363	21	7	XX	
3056	364	22	7	XX	
3064	365	23	7	XX	
3072	366	24	7	XX	
3080	367	25	7	XX	
3088	368	26	7	XX	
3096	369	27	7	XX	
3104	370	28	7	XX	
3112	371	29	7	XX	
3120	372	30	7	XX	
3128	373	31	7	XX	postamp
3136	374	31	7	XX	preamp
3144	375	32	7	XX	postamp
3152	376	32	7	XX	preamp
3160	377	33	7	XX	postamp
3168	378	33	7	XX	preamp
3176	379	34	7	XX	postamp
3184	380	34	7	XX	preamp
3192	381	35	7	XX	postamp
3200	382	35	7	XX	preamp
3208	383	36	7	XX	postamp
3216	384	36	7	XX	preamp
3224	385	1	29	XX	
3232	386	1	30	XX	
3240	387	1	31	XX	
3248	388	1	32	XX	
3256	389	2	29	XX	
3264	390	2	30	XX	
3272	391	2	31	XX	
3280	392	2	32	XX	
3288	393	3	15	XX	
3296	394	3	16	XX	
3304	395	4	15	XX	
3312	396	4	16	XX	
3320	397	5	15	XX	
3328	398	5	16	XX	

Reference Sort by Band/Det — 5/97

Pkt Start Bit	Memory Table Word Offset	Band	Det	PC Comments
1328	148	26	3	
1768	203	26	4	
2208	258	26	5	
2648	313	26	6	
3088	368	26	7	
3528	423	26	8	
3968	478	26	9	
4408	533	26	10	
456	39	27	1	
896	94	27	2	
1336	149	27	3	
1776	204	27	4	
2216	259	27	5	
2656	314	27	6	
3096	369	27	7	
3536	424	27	8	
3976	479	27	9	
4416	534	27	10	
464	40	28	1	
904	95	28	2	
1344	150	28	3	
1784	205	28	4	
2224	260	28	5	
2664	315	28	6	
3104	370	28	7	
3544	425	28	8	
3984	480	28	9	
4424	535	28	10	
472	41	29	1	
912	96	29	2	
1352	151	29	3	
1792	206	29	4	
2232	261	29	5	
2672	316	29	6	
3112	371	29	7	
3552	426	29	8	
3992	481	29	9	
4432	536	29	10	
480	42	30	1	
920	97	30	2	
1360	152	30	3	
1800	207	30	4	
2240	262	30	5	
2680	317	30	6	
3120	372	30	7	
3560	427	30	8	
4000	482	30	9	
4440	537	30	10	
488	43	31	1	postamp
496	44	31	1	preamp
928	98	31	2	postamp
936	99	31	2	preamp
1368	153	31	3	postamp
1376	154	31	3	preamp
1808	208	31	4	postamp
1816	209	31	4	preamp
2248	263	31	5	postamp

TABLE 30-4. MODIS ENGINEERING GROUP 1 PACKET 1 DATA FIELD
FPA DCR Offsets (4400 bits)

Sort by Pkt Start Bit — 550 words x 8 bits

Pkt Start Bit	Memory Table Word Offset	Band	Det	DCR Offset, Hex	PC Comments
3336	399	6	15	XX	
3344	400	6	16	XX	
3352	401	7	15	XX	
3360	402	7	16	XX	
3368	403	8	8	XX	
3376	404	9	8	XX	
3384	405	10	8	XX	
3392	406	11	8	XX	
3400	407	12	8	XX	
3408	408	13L	8	XX	
3416	409	13H	8	XX	
3424	410	14L	8	XX	
3432	411	14H	8	XX	
3440	412	15	8	XX	
3448	413	16	8	XX	
3456	414	17	8	XX	
3464	415	18	8	XX	
3472	416	19	8	XX	
3480	417	20	8	XX	
3488	418	21	8	XX	
3496	419	22	8	XX	
3504	420	23	8	XX	
3512	421	24	8	XX	
3520	422	25	8	XX	
3528	423	26	8	XX	
3536	424	27	8	XX	
3544	425	28	8	XX	
3552	426	29	8	XX	
3560	427	30	8	XX	
3568	428	31	8	XX	postamp
3576	429	31	8	XX	preamp
3584	430	32	8	XX	postamp
3592	431	32	8	XX	preamp
3600	432	33	8	XX	postamp
3608	433	33	8	XX	preamp
3616	434	34	8	XX	postamp
3624	435	34	8	XX	preamp
3632	436	35	8	XX	postamp
3640	437	35	8	XX	preamp
3648	438	36	8	XX	postamp
3656	439	36	8	XX	preamp
3664	440	1	33	XX	
3672	441	1	34	XX	
3680	442	1	35	XX	
3688	443	1	36	XX	
3696	444	2	33	XX	
3704	445	2	34	XX	
3712	446	2	35	XX	
3720	447	2	36	XX	
3728	448	3	17	XX	
3736	449	3	18	XX	
3744	450	4	17	XX	
3752	451	4	18	XX	
3760	452	5	17	XX	
3768	453	5	18	XX	
3776	454	6	17	XX	
3784	455	6	18	XX	

Reference Sort by Band/Det — 5/97

Pkt Start Bit	Memory Table Word Offset	Band	Det	PC Comments
2256	264	31	5	preamp
2688	318	31	6	postamp
2696	319	31	6	preamp
3128	373	31	7	postamp
3136	374	31	7	preamp
3568	428	31	8	postamp
3576	429	31	8	preamp
4008	483	31	9	postamp
4016	484	31	9	preamp
4448	538	31	10	postamp
4456	539	31	10	preamp
504	45	32	1	postamp
512	46	32	1	preamp
944	100	32	2	postamp
952	101	32	2	preamp
1384	155	32	3	postamp
1392	156	32	3	preamp
1824	210	32	4	postamp
1832	211	32	4	preamp
2264	265	32	5	postamp
2272	266	32	5	preamp
2704	320	32	6	postamp
2712	321	32	6	preamp
3144	375	32	7	postamp
3152	376	32	7	preamp
3584	430	32	8	postamp
3592	431	32	8	preamp
4024	485	32	9	postamp
4032	486	32	9	preamp
4464	540	32	10	postamp
4472	541	32	10	preamp
520	47	33	1	postamp
528	48	33	1	preamp
960	102	33	2	postamp
968	103	33	2	preamp
1400	157	33	3	postamp
1408	158	33	3	preamp
1840	212	33	4	postamp
1848	213	33	4	preamp
2280	267	33	5	postamp
2288	268	33	5	preamp
2720	322	33	6	postamp
2728	323	33	6	preamp
3160	377	33	7	postamp
3168	378	33	7	preamp
3600	432	33	8	postamp
3608	433	33	8	preamp
4040	487	33	9	postamp
4048	488	33	9	preamp
4480	542	33	10	postamp
4488	543	33	10	preamp
536	49	34	1	postamp
544	50	34	1	preamp
976	104	34	2	postamp
984	105	34	2	preamp
1416	159	34	3	postamp
1424	160	34	3	preamp

TABLE 30-4. MODIS ENGINEERING GROUP 1 PACKET 1 DATA FIELD
FPA DCR Offsets (4400 bits)

Sort by Pkt Start Bit — 550 words x 8 bits

Pkt Start Bit	Memory Table Word Offset	Band	Det	DCR Offset, Hex	PC Comments
3792	456	7	17	XX	
3800	457	7	18	XX	
3808	458	8	9	XX	
3816	459	9	9	XX	
3824	460	10	9	XX	
3832	461	11	9	XX	
3840	462	12	9	XX	
3848	463	13L	9	XX	
3856	464	13H	9	XX	
3864	465	14L	9	XX	
3872	466	14H	9	XX	
3880	467	15	9	XX	
3888	468	16	9	XX	
3896	469	17	9	XX	
3904	470	18	9	XX	
3912	471	19	9	XX	
3920	472	20	9	XX	
3928	473	21	9	XX	
3936	474	22	9	XX	
3944	475	23	9	XX	
3952	476	24	9	XX	
3960	477	25	9	XX	
3968	478	26	9	XX	
3976	479	27	9	XX	
3984	480	28	9	XX	
3992	481	29	9	XX	
4000	482	30	9	XX	
4008	483	31	9	XX	postamp
4016	484	31	9	XX	preamp
4024	485	32	9	XX	postamp
4032	486	32	9	XX	preamp
4040	487	33	9	XX	postamp
4048	488	33	9	XX	preamp
4056	489	34	9	XX	postamp
4064	490	34	9	XX	preamp
4072	491	35	9	XX	postamp
4080	492	35	9	XX	preamp
4088	493	36	9	XX	postamp
4096	494	36	9	XX	preamp
4104	495	1	37	XX	
4112	496	1	38	XX	
4120	497	1	39	XX	
4128	498	1	40	XX	
4136	499	2	37	XX	
4144	500	2	38	XX	
4152	501	2	39	XX	
4160	502	2	40	XX	
4168	503	3	19	XX	
4176	504	3	20	XX	
4184	505	4	19	XX	
4192	506	4	20	XX	
4200	507	5	19	XX	
4208	508	5	20	XX	
4216	509	6	19	XX	
4224	510	6	20	XX	
4232	511	7	19	XX	
4240	512	7	20	XX	

Reference Sort by Band/Det — 5/97

Pkt Start Bit	Memory Table Word Offset	Band	Det	PC Comments
1856	214	34	4	postamp
1864	215	34	4	preamp
2296	269	34	5	postamp
2304	270	34	5	preamp
2736	324	34	6	postamp
2744	325	34	6	preamp
3176	379	34	7	postamp
3184	380	34	7	preamp
3616	434	34	8	postamp
3624	435	34	8	preamp
4056	489	34	9	postamp
4064	490	34	9	preamp
4496	544	34	10	postamp
4504	545	34	10	preamp
552	51	35	1	postamp
560	52	35	1	preamp
992	106	35	2	postamp
1000	107	35	2	preamp
1432	161	35	3	postamp
1440	162	35	3	preamp
1872	216	35	4	postamp
1880	217	35	4	preamp
2312	271	35	5	postamp
2320	272	35	5	preamp
2752	326	35	6	postamp
2760	327	35	6	preamp
3192	381	35	7	postamp
3200	382	35	7	preamp
3632	436	35	8	postamp
3640	437	35	8	preamp
4072	491	35	9	postamp
4080	492	35	9	preamp
4512	546	35	10	postamp
4520	547	35	10	preamp
568	53	36	1	postamp
576	54	36	1	preamp
1008	108	36	2	postamp
1016	109	36	2	preamp
1448	163	36	3	postamp
1456	164	36	3	preamp
1888	218	36	4	postamp
1896	219	36	4	preamp
2328	273	36	5	postamp
2336	274	36	5	preamp
2768	328	36	6	postamp
2776	329	36	6	preamp
3208	383	36	7	postamp
3216	384	36	7	preamp
3648	438	36	8	postamp
3656	439	36	8	preamp
4088	493	36	9	postamp
4096	494	36	9	preamp
4528	548	36	10	postamp
4536	549	36	10	preamp
336	24	13H	1	
776	79	13H	2	
1216	134	13H	3	

TABLE 30-4. MODIS ENGINEERING GROUP 1 PACKET 1 DATA FIELD

FPA DCR Offsets (4400 bits)

Sort by Pkt Start Bit — 550 words x 8 bits

Pkt Start Bit	Memory Table Word Offset	Band	Det	DCR Offset, Hex	PC Comments
4248	513	8	10	XX	
4256	514	9	10	XX	
4264	515	10	10	XX	
4272	516	11	10	XX	
4280	517	12	10	XX	
4288	518	13L	10	XX	
4296	519	13H	10	XX	
4304	520	14L	10	XX	
4312	521	14H	10	XX	
4320	522	15	10	XX	
4328	523	16	10	XX	
4336	524	17	10	XX	
4344	525	18	10	XX	
4352	526	19	10	XX	
4360	527	20	10	XX	
4368	528	21	10	XX	
4376	529	22	10	XX	
4384	530	23	10	XX	
4392	531	24	10	XX	
4400	532	25	10	XX	
4408	533	26	10	XX	
4416	534	27	10	XX	
4424	535	28	10	XX	
4432	536	29	10	XX	
4440	537	30	10	XX	
4448	538	31	10	XX	postamp
4456	539	31	10	XX	preamp
4464	540	32	10	XX	postamp
4472	541	32	10	XX	preamp
4480	542	33	10	XX	postamp
4488	543	33	10	XX	preamp
4496	544	34	10	XX	postamp
4504	545	34	10	XX	preamp
4512	546	35	10	XX	postamp
4520	547	35	10	XX	preamp
4528	548	36	10	XX	postamp
4536	549	36	10	XX	preamp

• Pkt end bit = 4543. Subtract 144 to obtain local field bit.

Reference Sort by Band/Det — 5/97

Pkt Start Bit	Memory Table Word Offset	Band	Det	PC Comments
1656	189	13H	4	
2096	244	13H	5	
2536	299	13H	6	
2976	354	13H	7	
3416	409	13H	8	
3856	464	13H	9	
4296	519	13H	10	
328	23	13L	1	
768	78	13L	2	
1208	133	13L	3	
1648	188	13L	4	
2088	243	13L	5	
2528	298	13L	6	
2968	353	13L	7	
3408	408	13L	8	
3848	463	13L	9	
4288	518	13L	10	
352	26	14H	1	
792	81	14H	2	
1232	136	14H	3	
1672	191	14H	4	
2112	246	14H	5	
2552	301	14H	6	
2992	356	14H	7	
3432	411	14H	8	
3872	466	14H	9	
4312	521	14H	10	
344	25	14L	1	
784	80	14L	2	
1224	135	14L	3	
1664	190	14L	4	
2104	245	14L	5	
2544	300	14L	6	
2984	355	14L	7	
3424	410	14L	8	
3864	465	14L	9	
4304	520	14L	10	

Notes: *(This table also relates to 1553 bus memory locations, see Note 3)*

1. Table indicates DCR offset values for the FR to download to the FAM and SAM calculated on a per scan basis. Calculations compare FPA sensor data of BB view with ideal BB radiation for particular temperature and band. If the PC or PV DCR process has been commanded Off, the last processed values will continue to be downloaded each scan.

2. Field contains 550 x 8 bits = 4400 bits total, and includes DCR offsets for all detectors (all 1km IFOV's, including 13Hi/13Lo and 14Hi/13Lo, multiple detectors related to the 250m and 500m IFOV's, and separate preamp and postamp DCR values for PC Bands 31-36).

3. In Table 10-24, Memory Table 1 Offset locations are shown in Column 2 as Word-Offsets from zero location for use in 1553 Bus upload or download (16 bit memory words). Memory Table 4 for PV Gains is organized in the same relation with blanks where fixed gain PC data would appear.

TABLE 30-4. MODIS ENGINEERING GROUP 1 PACKET 1 DATA FIELD

FPA DCR Offsets (4400 bits)

Sort by Pkt Start Bit — 550 words x 8 bits

Pkt Start Bit	Memory Table Word Offset	Band	Det	DCR Offset, Hex	PC Comments

Reference Sort by Band/Det — 5/97

Pkt Start Bit	Memory Table Word Offset	Band	Det	PC Comments

T30-4 Change History

1. 9/17/96 Change title to Group vs Segment terminology.

TABLE 30-5A. MODIS ENGINEERING GROUP 1 PACKET 2 DATA FIELD

EARTH ENCODER TIME DATA (1248 bits)

• 78 words x 16 bits (24 data words + 54 fill words with 0 value). 5/97

• Time between every 100th mirror encoder pulse over earth view.

Pkt Start Bit	Time Count Hex, 16 bits
144	XXXX
160	XXXX
176	XXXX
192	XXXX
208	XXXX
224	XXXX
240	XXXX
256	XXXX
272	XXXX
288	XXXX
304	XXXX
320	XXXX
336	XXXX
352	XXXX
368	XXXX
384	XXXX
400	XXXX
416	XXXX
432	XXXX
448	XXXX
464	XXXX
480	XXXX
496	XXXX
512	0000
528	0000
544	0000
560	0000
576	0000
•	•
•	•
•	•
•	•
1344	0000
1360	0000
1376	0000

Pkt end bit = 1391. Subtract 144 to obtain local field bit.

Notes:

1. Nominal period of encoder counts is 180.32 μs.
2. Nominal 100 count interval = 18,032 μs.
3. 16 bits used to facilitate flight SW implementation.
4. Some powers of 2: 2^14 = 16384, 2^15 = 32,768, 2^16 = 65,536.
5. See Pkt bit 119 for mirror side ID (0=side 1, 1=side 2).
6. Count begins 2 FD times (333.333 μs) before earth FD collects begin. The first 100-group report occurs about 19 FD times after first formated FD is complete. Which takes 30 collect FDs to assemble

T30-5A Change History

1. 9/17/96 Change title to Group vs Segment terminology.

TABLE 30-5B. MODIS ENGINEERING GROUP 1 PACKET 2 DATA FIELD

VIEW SECTOR DEFINTIONS DATA (640 bits)

40 words x 16 bits 5/97

Pkt Enc Start Bit	View Sector	Mirror Side	SMA Enc A/B	Hex Count 16 bits	Decimal Count	Enc/Vern Data
1392	SD	1	A	36AC	13996	Enc
1408	SD	1	A	0	0	Vern
1424	SD	1	B	36B7	14007	Enc
1440	SD	1	B	17	23	Vern
1456	SD	2	A	16AC	5804	Enc
1472	SD	2	A	0	0	Vern
1488	SD	2	B	16B7	5815	Enc
1504	SD	2	B	17	23	Vern
1520	SRCA	1	A	38EB	14571	Enc
1536	SRCA	1	A	1A	26	Vern
1552	SRCA	1	B	38F7	14583	Enc
1568	SRCA	1	B	16	22	Vern
1584	SRCA	2	A	18EB	6379	Enc
1600	SRCA	2	A	1A	26	Vern
1616	SRCA	2	B	18F7	6391	Enc
1632	SRCA	2	B	16	22	Vern
1648	BB	1	A	3AEC	15084	Enc
1664	BB	1	A	10	16	Vern
1680	BB	1	B	3AF8	15096	Enc
1696	BB	1	B	C	12	Vern
1712	BB	2	A	1AEC	6892	Enc
1728	BB	2	A	10	16	Vern
1744	BB	2	B	1AF8	6904	Enc
1760	BB	2	B	C	12	Vern
1776	Space	1	A	3D9C	15772	Enc
1792	Space	1	A	14	20	Vern
1808	Space	1	B	3DA8	15784	Enc
1824	Space	1	B	F	15	Vern
1840	Space	2	A	1D9C	7580	Enc
1856	Space	2	A	14	20	Vern
1872	Space	2	B	1DA8	7592	Enc
1888	Space	2	B	F	15	Vern
1904	Earth	1	A	1A6	422	Enc
1920	Earth	1	A	7	7	Vern
1936	Earth	1	B	1B2	434	Enc
1952	Earth	1	B	2	2	Vern
1968	Earth	2	A	21A6	8614	Enc
1984	Earth	2	A	7	7	Vern
2000	Earth	2	B	21B2	8626	Enc
2016	Earth	2	B	2	2	Vern

• Pkt end bit = 2031. Subtract 1392 to obtain local field bit.

Notes:

1. Encoder & vernier counts are 16-bit words each, or 640 bits total.
2. As listed, Pkt bit locations increment, alternating between Enc Start Bit and Vrn Start Bit.
3. Encoder counts are interger number of 180.32 μs encoder pulses from mirror Index.
4. Vernier counts are integer number of 6.66 μs (0.02 IFOV@1km) vernier pulses.
5. Sum of encoder and vernier counts define start of view sector. Once synced, there are three FD reset sample settling times before collects start.
6. Figure 30-1 indicates how many 333.333μs FD are collected across each view.

T30-5B Change History

1. 9/17/96 Revise title to Group vs Segment terminology & mesh encoder/vernier cols.
2. 4/97 EO1122D incorporations for Rev B to SD, SRCA & BB encoder view starts.
3. 4/97 Direct Rev B change to decrease Space View start by 30 encoder counts .

TABLE 30-5C. MODIS ENGINEERING GROUP 1 PACKET 2 DATA FIELD
VIEW SECTOR ACTUALS (384 bits)

40 words x 16 bits 5/97

Pkt Enc Start Bit	View Sector Parameter	Hex Value
2032	SD Encoder	XXXX
2048	SD Vernier	XXXX
2064	SRCA Encoder	XXXX
2080	SRCA Vernier	XXXX
2096	BB Encoder	XXXX
2112	BB Vernier	XXXX
2128	Space Encoder	XXXX
2144	Space Vernier	XXXX
2160	Earth Encoder	XXXX
2176	Earth Vernier	XXXX
2192	Mirror Side [2]	X
2196	SM Elec Side [3]	X
2200	216 Fill Bits [4]	na

• Pkt end bit = 2415. Subtract 2032 to obtain local field bit.

Notes:

1. This table reflects the actual in-use subset of Table 30-5B. It includes any test delta encoder or vernier counts. Values rotate scan by scan.

[2] Mirror side: 0=side 1, 1=side 2.

[3] SM Elec side: 0=side A, 1=side B.

[4] Fill bits assure the next field start (Eng Data) is the same as for the EM.

T30-5C Change History

1. 9/17/96 New table.

TABLE 30-5D. MODIS ENGINEERING GROUP 1 PACKET 2 DATA FIELD

ENGINEERING DATA (1792 bits) - BB, FAM, SAM, SDSM & SRCA Data

User interest may be limited to Columns 1, 2 & 7 - - See Notes at table bottom for description of columns. *5/97*

pf chgs	1 Subsystem	2 Mnemonic Name	3 # of Bits	4 Pkt#2 Start Bit	5 Approx Tlmy Range	6 Scale & Limit	7 Remarks	8 Tlmy Type	9 Analog Mux	10 HW Addr/Read	11 HW Data	12 Design Unique ID
	BB	IR_BB_HTRA_CURR	8	2416	0 to 1.25A	T20-5	BB Htr A current (bang-bang SW controller); SW echo in HK T20-2	A	A	C0003/C0004	5572	MM09A01T
	BB	IR_BB_HTRB_CURR	8	2424	0 to 1.25A	T20-5	BB Htr B current (bang-bang SW controller); SW echo in HK T20-2	A	A	C0003/C0004	5773	MM09A19T
	BB	TP_BB_TEMP01	12	2432	270K to 320K	T20-6	Obc BB temp; SW echo in HK T20-2	P	PB	C0003/C0004	X00B	CE01A01T
	BB	TP_BB_TEMP02	12	2444	270K to 320K	T20-6	Obc BB temp; SW echo in HK T20-2	P	PB	C0003/C0004	X08B	CE01A02T
	BB	TP_BB_TEMP03	12	2456	270K to 320K	T20-6	Obc BB temp; SW echo in HK T20-2	P	PB	C0003/C0004	X10B	CE01A03T
	BB	TP_BB_TEMP04	12	2468	270K to 320K	T20-6	Obc BB temp; SW echo in HK T20-2	P	PB	C0003/C0004	X18B	CE01A04T
	BB	TP_BB_TEMP05	12	2480	270K to 320K	T20-6	Obc BB temp; SW echo in HK T20-2	P	PB	C0003/C0004	X20B	CE01A05T
	BB	TP_BB_TEMP06	12	2492	270K to 320K	T20-6	Obc BB temp; SW echo in HK T20-2	P	PB	C0003/C0004	X28B	CE01A06T
	BB	TP_BB_TEMP07	12	2504	270K to 320K	T20-6	Obc BB temp; SW echo in HK T20-2	P	PB	C0003/C0004	X30B	CE01A07T
	BB	TP_BB_TEMP08	12	2516	270K to 320K	T20-6	Obc BB temp; SW echo in HK T20-2	P	PB	C0003/C0004	X38B	CE01A08T
	BB	TP_BB_TEMP09	12	2528	270K to 320K	T20-6	Obc BB temp; SW echo in HK T20-2	P	PB	C0003/C0004	X40B	CE01A09T
	BB	TP_BB_TEMP10	12	2540	270K to 320K	T20-6	Obc BB temp; SW echo in HK T20-2	P	PB	C0003/C0004	X48B	CE01A10T
	BB	TP_BB_TEMP11	12	2552	270K to 320K	T20-6	Obc BB temp; SW echo in HK T20-2	P	PB	C0003/C0004	X50B	CE01A11T
	BB	TP_BB_TEMP12	12	2564	270K to 320K	T20-6	Obc BB temp; SW echo in HK T20-2	P	PB	C0003/C0004	X58B	CE01A12T
	BB	TP_BB_TEMP_AVG	12	2576	270K to 320K	na	Obc BB avg temp used by Flt SW for DCR algorithmn	SW	na	na	na	na
	CP	SS_CP_VALENG_FMT	1	2588	na	na	CP valid format for eng data to go over CP-FR link, Valid=1	SW	na	na	na	na
15	PC	VR_PC_B31C10_DCR	8	2589	-2.5 TO 2.5V	T20-5	FAM AF01mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	0070	AF01A01T
15	PC	VR_PC_B31C09_DCR	8	2597	-2.5 TO 2.5V	T20-5	FAM AF01mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	0070	AF01A01T
15	PC	VR_PC_B31C08_DCR	8	2605	-2.5 TO 2.5V	T20-5	FAM AF01mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	0070	AF01A01T
15	PC	VR_PC_B31C07_DCR	8	2613	-2.5 TO 2.5V	T20-5	FAM AF01mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	0070	AF01A01T
15	PC	VR_PC_B31C06_DCR	8	2621	-2.5 TO 2.5V	T20-5	FAM AF01mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	0070	AF01A01T
15	PC	VR_PC_B31C05_DCR	8	2629	-2.5 TO 2.5V	T20-5	FAM AF01mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	0070	AF01A01T
15	PC	VR_PC_B31C04_DCR	8	2637	-2.5 TO 2.5V	T20-5	FAM AF01mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	0070	AF01A01T
15	PC	VR_PC_B31C03_DCR	8	2645	-2.5 TO 2.5V	T20-5	FAM AF01mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	0070	AF01A01T
15	PC	VR_PC_B31C02_DCR	8	2653	-2.5 TO 2.5V	T20-5	FAM AF01mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	0070	AF01A01T
15	PC	VR_PC_B31C01_DCR	8	2661	-2.5 TO 2.5V	T20-5	FAM AF01mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	0070	AF01A01T
15	PC	VR_PC_B32C10_DCR	8	2669	-2.5 TO 2.5V	T20-5	FAM AF02 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	00F0	AF02A01T
15	PC	VR_PC_B32C09_DCR	8	2677	-2.5 TO 2.5V	T20-5	FAM AF02 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	00F0	AF02A01T
15	PC	VR_PC_B32C08_DCR	8	2685	-2.5 TO 2.5V	T20-5	FAM AF02 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	00F0	AF02A01T
15	PC	VR_PC_B32C07_DCR	8	2693	-2.5 TO 2.5V	T20-5	FAM AF02 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	00F0	AF02A01T
15	PC	VR_PC_B32C06_DCR	8	2701	-2.5 TO 2.5V	T20-5	FAM AF02 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	00F0	AF02A01T
15	PC	VR_PC_B32C05_DCR	8	2709	-2.5 TO 2.5V	T20-5	FAM AF02 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	00F0	AF02A01T
15	PC	VR_PC_B32C04_DCR	8	2717	-2.5 TO 2.5V	T20-5	FAM AF02 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	00F0	AF02A01T
15	PC	VR_PC_B32C03_DCR	8	2725	-2.5 TO 2.5V	T20-5	FAM AF02 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	00F0	AF02A01T
15	PC	VR_PC_B32C02_DCR	8	2733	-2.5 TO 2.5V	T20-5	FAM AF02 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	00F0	AF02A01T
7,15	PC	VR_PC_B32C01_DCR	8	2741	-2.5 TO 2.5V	T20-5	FAM AF02 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	00F0	AF02A01T
7,15	PC	VR_PC_B33C10_DCR	8	2749	-2.5 TO 2.5V	T20-5	FAM AF02 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	00F0	AF02A01T
7,15	PC	VR_PC_B33C09_DCR	8	2757	-2.5 TO 2.5V	T20-5	FAM AF03 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	0170	AF03A01T
7,15	PC	VR_PC_B33C08_DCR	8	2765	-2.5 TO 2.5V	T20-5	FAM AF03 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	0170	AF03A01T

TABLE 30-5D. MODIS ENGINEERING GROUP 1 PACKET 2 DATA FIELD

ENGINEERING DATA (1792 bits) - BB, FAM, SAM, SDSM & SRCA Data

User interest may be limited to Columns 1, 2 & 7 - - See Notes at table bottom for description of columns.

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pf chgs	1 Subsystem	2 Mnemonic Name	3 # of Bits	4 Pkt#2 Start Bit	5 Approx Tlmy Range	6 Scale & Limit	7 Remarks	8 Tlmy Type	9 Analog Mux	10 HW Addr/Read	11 HW Data	12 Design Unique ID
7,15	PC	VR_PC_B33C07_DCR	8	2773	-2.5 TO 2.5V	T20-5	FAM AF03 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	0170	AF03A01T
7,15	PC	VR_PC_B33C06_DCR	8	2781	-2.5 TO 2.5V	T20-5	FAM AF03 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	0170	AF03A01T
7,15	PC	VR_PC_B33C05_DCR	8	2789	-2.5 TO 2.5V	T20-5	FAM AF03 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	0170	AF03A01T
7,15	PC	VR_PC_B33C04_DCR	8	2797	-2.5 TO 2.5V	T20-5	FAM AF03 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	0170	AF03A01T
7,15	PC	VR_PC_B33C03_DCR	8	2805	-2.5 TO 2.5V	T20-5	FAM AF03 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	0170	AF03A01T
7,15	PC	VR_PC_B33C02_DCR	8	2813	-2.5 TO 2.5V	T20-5	FAM AF03 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	0170	AF03A01T
7,15	PC	VR_PC_B33C01_DCR	8	2821	-2.5 TO 2.5V	T20-5	FAM AF03 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	0170	AF03A01T
15	PC	VR_PC_B34C10_DCR	8	2829	-2.5 TO 2.5V	T20-5	FAM AF04 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	01F0	AF04A01T
15	PC	VR_PC_B34C09_DCR	8	2837	-2.5 TO 2.5V	T20-5	FAM AF04 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	01F0	AF04A01T
15	PC	VR_PC_B34C08_DCR	8	2845	-2.5 TO 2.5V	T20-5	FAM AF04 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	01F0	AF04A01T
15	PC	VR_PC_B34C07_DCR	8	2853	-2.5 TO 2.5V	T20-5	FAM AF04 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	01F0	AF04A01T
15	PC	VR_PC_B34C06_DCR	8	2861	-2.5 TO 2.5V	T20-5	FAM AF04 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	01F0	AF04A01T
15	PC	VR_PC_B34C05_DCR	8	2869	-2.5 TO 2.5V	T20-5	FAM AF04 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	01F0	AF04A01T
15	PC	VR_PC_B34C04_DCR	8	2877	-2.5 TO 2.5V	T20-5	FAM AF04 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	01F0	AF04A01T
15	PC	VR_PC_B34C03_DCR	8	2885	-2.5 TO 2.5V	T20-5	FAM AF04 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	01F0	AF04A01T
15	PC	VR_PC_B34C02_DCR	8	2893	-2.5 TO 2.5V	T20-5	FAM AF04 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	01F0	AF04A01T
15	PC	VR_PC_B34C01_DCR	8	2901	-2.5 TO 2.5V	T20-5	FAM AF04 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	01F0	AF04A01T
15	PC	VR_PC_B35C10_DCR	8	2909	-2.5 TO 2.5V	T20-5	FAM AF05 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	0270	AF05A01T
15	PC	VR_PC_B35C09_DCR	8	2917	-2.5 TO 2.5V	T20-5	FAM AF05 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	0270	AF05A01T
15	PC	VR_PC_B35C08_DCR	8	2925	-2.5 TO 2.5V	T20-5	FAM AF05 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	0270	AF05A01T
15	PC	VR_PC_B35C07_DCR	8	2933	-2.5 TO 2.5V	T20-5	FAM AF05 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	0270	AF05A01T
15	PC	VR_PC_B35C06_DCR	8	2941	-2.5 TO 2.5V	T20-5	FAM AF05 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	0270	AF05A01T
15	PC	VR_PC_B35C05_DCR	8	2949	-2.5 TO 2.5V	T20-5	FAM AF05 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	0270	AF05A01T
15	PC	VR_PC_B35C04_DCR	8	2957	-2.5 TO 2.5V	T20-5	FAM AF05 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	0270	AF05A01T
15	PC	VR_PC_B35C03_DCR	8	2965	-2.5 TO 2.5V	T20-5	FAM AF05 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	0270	AF05A01T
15	PC	VR_PC_B35C02_DCR	8	2973	-2.5 TO 2.5V	T20-5	FAM AF05 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	0270	AF05A01T
15	PC	VR_PC_B35C01_DCR	8	2981	-2.5 TO 2.5V	T20-5	FAM AF05 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	0270	AF05A01T
15	PC	VR_PC_B36C10_DCR	8	2989	-2.5 TO 2.5V	T20-5	FAM AF06 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	02F0	AF06A01T
15	PC	VR_PC_B36C09_DCR	8	2997	-2.5 TO 2.5V	T20-5	FAM AF06 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	02F0	AF06A01T
15	PC	VR_PC_B36C08_DCR	8	3005	-2.5 TO 2.5V	T20-5	FAM AF06 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	02F0	AF06A01T
15	PC	VR_PC_B36C07_DCR	8	3013	-2.5 TO 2.5V	T20-5	FAM AF06 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	02F0	AF06A01T
15	PC	VR_PC_B36C06_DCR	8	3021	-2.5 TO 2.5V	T20-5	FAM AF06 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	02F0	AF06A01T
15	PC	VR_PC_B36C05_DCR	8	3029	-2.5 TO 2.5V	T20-5	FAM AF06 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	02F0	AF06A01T
15	PC	VR_PC_B36C04_DCR	8	3037	-2.5 TO 2.5V	T20-5	FAM AF06 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	02F0	AF06A01T
15	PC	VR_PC_B36C03_DCR	8	3045	-2.5 TO 2.5V	T20-5	FAM AF06 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	02F0	AF06A01T
15	PC	VR_PC_B36C02_DCR	8	3053	-2.5 TO 2.5V	T20-5	FAM AF06 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	02F0	AF06A01T
15	PC	VR_PC_B36C01_DCR	8	3061	-2.5 TO 2.5V	T20-5	FAM AF06 mux; tlmy result of FR data bus postamp DCR	APC	A	C0003/C0004	02F0	AF06A01T
1	PV	CR_PVLW_S_DELAY	8	3069	0-50 units	T20-5	PV LWIR registration delay of A_4 or B_10 C&B-ACE pwb, D#0-50 max, 1=3.33µs; SW echo in HK T20-2	APV	A	C0003/C0004	0371	AS10A02T

TABLE 30-5D. MODIS ENGINEERING GROUP 1 PACKET 2 DATA FIELD

ENGINEERING DATA (1792 bits) - BB, FAM, SAM, SDSM & SRCA Data

User interest may be limited to Columns 1, 2 & 7 - - See Notes at table bottom for description of columns. *5/97*

pf chge	1 Subsystem	2 Mnemonic Name	3 # of Bits	4 Pkt#2 Start Bit	5 Approx Tlmy Range	6 Scale & Limit	7 Remarks	8 Tlmy Type	9 Analog Mux	10 HW Addr/Read	11 HW Data	12 Design Unique ID
1	PV	CR_PVNIR_S_DELAY	8	3077	0-50 units	T20-5	PV NIR registration sample delay of A_2 or B_8 C&B-ACE pwb, D#0-50 max, 1=3.33μs; SW echo in HK T20-2	APV	A	C0003/C0004	0371	AS10A02T
1	PV	CR_PVSM_S_DELAY	8	3085	0-50 units	T20-5	PV SMIR registration sample delay of A_5 or B_11 C&B pwb, D#0-50 max, 1=3.33μs; SW echo in HK T20-2	APV	A	C0003/C0004	0371	AS10A02T
1	PV	CR_PVVIS_S_DELAY	8	3093	0-50 units	T20-5	PV VIS registration sample delay of A_1 or B_7 C&B-ACE pwb, D#0-50 max, 1=3.33μs; SW echo in HK T20-2	APV	A	C0003/C0004	0371	AS10A02T
	PV	VR_PVLW_ITWKA	8	3101	-4.1 to +4.1V	T20-5	PV LWIR SCA ITWKA bias of A_4 or B_10 C&B-ACE pwb; in param T30-5E	APV	A	C0003/C0004	0371	AS10A02T
	PV	VR_PVLW_VCAL	8	3109	-10 to +10V	T20-5	PV LWIR SCA VCAL(ECAL) bias of A_4 or B_10 C&B-ACE pwb; SW echo in HK T20-2; in param T30-5E	APV	A	C0003/C0004	0371	AS10A02T
	PV	VR_PVLW_VDDA	8	3117	-10 to +10V	T20-5	PV LWIR SCA VDDA bias of A_4 or B_10 C&B-ACE pwb	APV	A	C0003/C0004	0371	AS10A02T
	PV	VR_PVLW_VDDD	8	3125	-10 to +10V	T20-5	PV LWIR SCA VDDD bias of A_4 or B_10 C&B-ACE pwb	APV	A	C0003/C0004	0371	AS10A02T
	PV	VR_PVLW_VDDOUT	8	3133	-10 to +10V	T20-5	PV LWIR SCA VDDOUT bias of A_4 or B_10 C&B-ACE pwb	APV	A	C0003/C0004	0371	AS10A02T
	PV	VR_PVLW_VDET	8	3141	-25.2 to +25.2V	T20-5	PV LWIR SCA VDET bias of A_4 or B_10 C&B-ACE pwb	APV	A	C0003/C0004	0371	AS10A02T
	PV	VR_PVLW_VPWELL	8	3149	-10 to +10V	T20-5	PV LWIR SCA VPWELL bias of A_4 or B_10 C&B-ACE pwb	APV	A	C0003/C0004	0371	AS10A02T
	PV	VR_PVNIR_ITWKA	8	3157	-4.1 to +4.1V	T20-5	PV NIR SCA ITWKA bias of A_2 or B_8 C&B-ACE pwb; in param T30-5E	APV	A	C0003/C0004	0371	AS10A02T
	PV	VR_PVNIR_VCAL	8	3165	-10 to +10V	T20-5	PV NIR SCA VCAL(ECAL) bias of A_2 or B_8 C&B-ACE pwb; SW echo in HK T20-2; in param T30-5E	APV	A	C0003/C0004	0371	AS10A02T
	PV	VR_PVNIR_VD1	8	3173	-25.2 to +25.2V	T20-5	PV NIR SCA VD1 bias of A_2 or B_8 C&B-ACE pwb	APV	A	C0003/C0004	0371	AS10A02T
	PV	VR_PVNIR_VDDA	8	3181	-10 to +10V	T20-5	PV NIR SCA VDDA bias of A_2 or B_8 C&B-ACE pwb	APV	A	C0003/C0004	0371	AS10A02T
	PV	VR_PVNIR_VDDD	8	3189	-10 to +10V	T20-5	PV NIR SCA VDDD bias of A_2 or B_8 C&B-ACE pwb	APV	A	C0003/C0004	0371	AS10A02T
	PV	VR_PVNIR_VDDOUT	8	3197	-10 to +10V	T20-5	PV NIR SCA VDDOUT bias of A_2 or B_8 C&B-ACE pwb	APV	A	C0003/C0004	0371	AS10A02T
	PV	VR_PVNIR_VDET	8	3205	-25.2 to +25.2V	T20-5	PV NIR SCA VDET bias of A_2 or B_8 C&B-ACE pwb	APV	A	C0003/C0004	0371	AS10A02T
	PV	VR_PVNIR_VGUARD	8	3213	-2.5 to +2.5V	T20-5	PV NIR SCA VGUARD bias of A_2 or B_8 C&B-ACE pwb	APV	A	C0003/C0004	0371	AS10A02T
	PV	VR_PVNIR_VPWELL	8	3221	-10 to +10V	T20-5	PV NIR SCA VPWELL bias of A_2 or B_8 C&B-ACE pwb	APV	A	C0003/C0004	0371	AS10A02T
	PV	VR_PVSM_ITWKA	8	3229	-4.1 to +4.1V	T20-5	PV SMIR ITWKA bias of A_5 or B_11 C&B pwb; in param T30-5E	APV	A	C0003/C0004	0371	AS10A02T
	PV	VR_PVSM_VCAL	8	3237	-10 to +10V	T20-5	PV SMIR SCA VCAL bias of A_5 or B_11 C&B pwb; in HK T20-2; in param T30-5E	APV	A	C0003/C0004	0371	AS10A02T
	PV	VR_PVSM_VDDA	8	3245	-10 to +10V	T20-5	PV SMIR SCA VDDA bias of A_5 or B_11 C&B pwb	APV	A	C0003/C0004	0371	AS10A02T
	PV	VR_PVSM_VDDD	8	3253	-10 to +10V	T20-5	PV SMIR SCA VDDD bias of A_5 or B_11 C&B pwb	APV	A	C0003/C0004	0371	AS10A02T
	PV	VR_PVSM_VDDOUT	8	3261	-10 to +10V	T20-5	PV SMIR SCA VDDOUT bias of A_5 or B_11 C&B pwb	APV	A	C0003/C0004	0371	AS10A02T
	PV	VR_PVSM_VDET	8	3269	-25.2 to +25.2V	T20-5	PV SMIR SCA VDET bias of A_5 or B_11 C&B pwb	APV	A	C0003/C0004	0371	AS10A02T
	PV	VR_PVSM_VPWELL	8	3277	-10 to +10V	T20-5	PV SMIR SCA VPWELL bias of A_5 or B_11 C&B pwb	APV	A	C0003/C0004	0371	AS10A02T
	PV	VR_PVVIS_ITWKA	8	3285	-4.1 to +4.1V	T20-5	PV VIS ITWKA bias of A_1 or B_7 C&B-ACE pwb; in param T30-5E	APV	A	C0003/C0004	0371	AS10A02T
	PV	VR_PVVIS_VCAL	8	3293	-10 to +10V	T20-5	PV VIS SCA VCAL(ECAL) bias of A_1 or B_7 C&B-ACE pwb; SW echo in HK T20-2; in param T30-5E	APV	A	C0003/C0004	0371	AS10A02T
	PV	VR_PVVIS_VD1	8	3301	-25.2 to +25.2V	T20-5	PV VIS SCA VD1 bias of A_1 or B_7 C&B-ACE pwb	APV	A	C0003/C0004	0371	AS10A02T
	PV	VR_PVVIS_VDDA	8	3309	-10 to +10V	T20-5	PV VIS SCA VDDA bias of A_1 or B_7 C&B-ACE pwb	APV	A	C0003/C0004	0371	AS10A02T
	PV	VR_PVVIS_VDDD	8	3317	-10 to +10V	T20-5	PV VIS SCA VDDD bias of A_1 or B_7 C&B-ACE pwb	APV	A	C0003/C0004	0371	AS10A02T
	PV	VR_PVVIS_VDDOUT	8	3325	-10 to +10V	T20-5	PV VIS SCA VDDOUT bias of A_1 or B_7 C&B-ACE pwb	APV	A	C0003/C0004	0371	AS10A02T
	PV	VR_PVVIS_VDET	8	3333	-25.2 to +25.2V	T20-5	PV VIS SCA VDET bias of A_1 or B_7 C&B-ACE pwb	APV	A	C0003/C0004	0371	AS10A02T
	PV	VR_PVVIS_VGUARD	8	3341	-2.5 to +2.5V	T20-5	PV VIS SCA VGUARD bias of A_1 or B_7 C&B-ACE pwb	APV	A	C0003/C0004	0371	AS10A02T

TABLE 30-5D. MODIS ENGINEERING GROUP 1 PACKET 2 DATA FIELD

ENGINEERING DATA (1792 bits) - BB, FAM, SAM, SDSM & SRCA Data

User interest may be limited to Columns 1, 2 & 7 - - See Notes at table bottom for description of columns. *5/97*

pf chgs	1 Subsystem	2 Mnemonic Name	3 # of Bits	4 Pkt#2 Start Bit	5 Approx Tlmy Range	6 Scale & Limit	7 Remarks	8 Tlmy Type	9 Analog Mux	10 HW Addr/Read	11 HW Data	12 Design Unique ID
	PV	VR_PVVIS_VPWELL	8	3349	-10 to +10V	T20-5	PV VIS SCA VPWELL bias of A_1 or B_7 C&B-ACE pwb	APV	A	C0003/C0004	0371	AS10A02T
3	SM	SS_SM_VIEW_SMPL1	2	3357	na	Col 7	00=invalid, 01=SD, 10=DCR, 11=SUN; similar step pt in HK T20-2	SW	na	na	na	na
3	SM	SS_SM_VIEW_SMPL2	2	3359	na	Col 7	00=invalid, 01=SD, 10=DCR, 11=SUN; similar step pt in HK T20-2	SW	na	na	na	na
3	SM	SS_SM_VIEW_SMPL3	2	3361	na	Col 7	00=invalid, 01=SD, 10=DCR, 11=SUN; similar step pt in HK T20-2	SW	na	na	na	na
9,14	SM	VR_SM01_SMPL1	12	3363	T20-5	T20-5	SDSM 413nm Si det (Band 8); see T20-5 for scale factor eq	A	A	C0003/C0004	0D7C	CE04A01T
9,14	SM	VR_SM01_SMPL2	12	3375	T20-5	T20-5	SDSM 413nm Si det (Band 8); see T20-5 for scale factor eq	A	A	C0003/C0004	0D7C	CE04A01T
9,14	SM	VR_SM01_SMPL3	12	3387	T20-5	T20-5	SDSM 413nm Si det (Band 8); see T20-5 for scale factor eq	A	A	C0003/C0004	0D7C	CE04A01T
14	SM	VR_SM02_SMPL1	12	3399	T20-5	T20-5	SDSM 469nm Si det (Band 3); see T20-5 for scale factor eq	A	A	C0003/C0004	0CFB	CE04A02T
14	SM	VR_SM02_SMPL2	12	3411	T20-5	T20-5	SDSM 469nm Si det (Band 3); see T20-5 for scale factor eq	A	A	C0003/C0004	0CFB	CE04A02T
14	SM	VR_SM02_SMPL3	12	3423	T20-5	T20-5	SDSM 469nm Si det (Band 3); see T20-5 for scale factor eq	A	A	C0003/C0004	0CFB	CE04A02T
9,14	SM	VR_SM03_SMPL1	12	3435	T20-5	T20-5	SDSM 534nm Si det (Band 11); see T20-5 for scale factor eq	A	A	C0003/C0004	0C7A	CE04A03T
9,14	SM	VR_SM03_SMPL2	12	3447	T20-5	T20-5	SDSM 534nm Si det (Band 11); see T20-5 for scale factor eq	A	A	C0003/C0004	0C7A	CE04A03T
9,14	SM	VR_SM03_SMPL3	12	3459	T20-5	T20-5	SDSM 534nm Si det (Band 11); see T20-5 for scale factor eq	A	A	C0003/C0004	0C7A	CE04A03T
9,14	SM	VR_SM04_SMPL1	12	3471	T20-5	T20-5	SDSM 558nm Si det (Band 4); see T20-5 for scale factor eq	A	A	C0003/C0004	0BF9	CE04A04T
9,14	SM	VR_SM04_SMPL2	12	3483	T20-5	T20-5	SDSM 558nm Si det (Band 4); see T20-5 for scale factor eq	A	A	C0003/C0004	0BF9	CE04A04T
9,14	SM	VR_SM04_SMPL3	12	3495	T20-5	T20-5	SDSM 558nm Si det (Band 4); see T20-5 for scale factor eq	A	A	C0003/C0004	0BF9	CE04A04T
9,14	SM	VR_SM05_SMPL1	12	3507	T20-5	T20-5	SDSM 644nm Si det (Band 1); see T20-5 for scale factor eq	A	A	C0003/C0004	0B78	CE04A05T
9,14	SM	VR_SM05_SMPL2	12	3519	T20-5	T20-5	SDSM 644nm Si det (Band 1); see T20-5 for scale factor eq	A	A	C0003/C0004	0B78	CE04A05T
9,14	SM	VR_SM05_SMPL3	12	3531	T20-5	T20-5	SDSM 644nm Si det (Band 1); see T20-5 for scale factor eq	A	A	C0003/C0004	0B78	CE04A05T
9,14	SM	VR_SM06_SMPL1	12	3543	T20-5	T20-5	SDSM 749nm Si det (Band 15); see T20-5 for scale factor eq	A	A	C0003/C0004	0AF7	CE04A06T
9,14	SM	VR_SM06_SMPL2	12	3555	T20-5	T20-5	SDSM 749nm Si det (Band 15); see T20-5 for scale factor eq	A	A	C0003/C0004	0AF7	CE04A06T
9,14	SM	VR_SM06_SMPL3	12	3567	T20-5	T20-5	SDSM 749nm Si det (Band 15); see T20-5 for scale factor eq	A	A	C0003/C0004	0AF7	CE04A06T
9,14	SM	VR_SM07_SMPL1	12	3579	T20-5	T20-5	SDSM 861nm Si det (Band 2); see T20-5 for scale factor eq	A	A	C0003/C0004	0A76	CE04A07T
9,14	SM	VR_SM07_SMPL2	12	3591	T20-5	T20-5	SDSM 861nm Si det (Band 2); see T20-5 for scale factor eq	A	A	C0003/C0004	0A76	CE04A07T
9,14	SM	VR_SM07_SMPL3	12	3603	T20-5	T20-5	SDSM 861nm Si det (Band 2); see T20-5 for scale factor eq	A	A	C0003/C0004	0A76	CE04A07T
14	SM	VR_SM08_SMPL1	12	3615	T20-5	T20-5	SDSM 905nm Si det (Band 17); see T20-5 for scale factor eq	A	A	C0003/C0004	09F5	CE04A08T
14	SM	VR_SM08_SMPL2	12	3627	T20-5	T20-5	SDSM 905nm Si det (Band 17); see T20-5 for scale factor eq	A	A	C0003/C0004	09F5	CE04A08T
14	SM	VR_SM08_SMPL3	12	3639	T20-5	T20-5	SDSM 905nm Si det (Band 17); see T20-5 for scale factor eq	A	A	C0003/C0004	09F5	CE04A08T
8,14	SM	VR_SM09_SMPL1	12	3651	T20-5	T20-5	SDSM 939nm Si det (19); see T20-5 for scale factor eq	A	A	C0003/C0004	0974	CE04A09T
8,14	SM	VR_SM09_SMPL2	12	3663	T20-5	T20-5	SDSM 939nm Si det (19); see T20-5 for scale factor eq	A	A	C0003/C0004	0974	CE04A09T
8,14	SM	VR_SM09_SMPL3	12	3675	T20-5	T20-5	SDSM 939nm Si det (19); see T20-5 for scale factor eq	A	A	C0003/C0004	0974	CE04A09T
13,15	SR	CS_SR_LAMP_USE	3	3687	na	Col 7	SR lamp On combination: B#000=not On; 001=1X10W; 010=2X10W; 011= 3X10W; 100=1X1W; other codes=invalid. Rdt to later CS_SR_LAMPSE from 1553	SW	na	na	na	na
15	SR	IR_SR_10WLA_CURR	12	3690	T20-5	T20-5	SRCA 10W Lamp Current_A=B#; SW echo in HK T20-2	A	A	C0003/C0004	58F3	MM10A02T
15	SR	IR_SR_10WLB_CURR	12	3702	T20-5	T20-5	SRCA 10W Lamp Current_B=B#; SW echo in HK T20-2	A	A	C0003/C0004	5A73	MM10A05T
15	SR	IR_SR_1WLA_CURR	12	3714	T20-5	T20-5	SRCA 1W Lamp Current_A=B#; SW echo in HK T20-2	A	A	C0003/C0004	5873	MM10A01T
15	SR	IR_SR_1WLB_CURR	12	3726	T20-5	T20-5	SRCA 1W Lamp Current_B=B#; SW echo in HK T20-2	A	A	C0003/C0004	59F3	MM10A04T
15	SR	VR_SR_LAMPS	12	3738	T20-5	T20-5	Common voltage across all lamps; SW echo in HK T20-2	A	A	C0003/C0004	5B74	MM10A22T
15	SR	VR_SR_SELF_CAL1	12	3750	T20-5	T20-5	SRCA Didymium spectral self cal det sample 1	A	A	C0003/C0004	0872	CE03A20T

TABLE 30-5D. MODIS ENGINEERING GROUP 1 PACKET 2 DATA FIELD

ENGINEERING DATA (1792 bits) - BB, FAM, SAM, SDSM & SRCA Data

User interest may be limited to Columns 1, 2 & 7 - - See Notes at table bottom for description of columns.

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pf chgs	1 Subsystem	2 Mnemonic Name	3 # of Bits	4 Pkt#2 Start Bit	5 Approx Tlmy Range	6 Scale & Limit	7 Remarks	8 Tlmy Type	9 Analog Mux	10 HW Addr/Read	11 HW Data	12 Design Unique ID
15	SR	VR_SR_SELF_CAL2	12	3762	T20-5	T20-5	SRCA Didymium spectral self cal det sample 2	A	A	C0003/C0004	0872	CE03A20T
15	SR	VR_SR_SELF_CAL3	12	3774	T20-5	T20-5	SRCA Didymium spectral self cal det sample 3	A	A	C0003/C0004	0872	CE03A20T
15	SR	VR_SR_SPCT_NORM1	12	3786	T20-5	T20-5	SRCA Collimator ref det for normaliztion sample 1	A	A	C0003/C0004	08F3	CE03A21T
15	SR	VR_SR_SPCT_NORM2	12	3798	T20-5	T20-5	SRCA Collimator ref det for normaliztion sample 2	A	A	C0003/C0004	08F3	CE03A21T
15	SR	VR_SR_SPCT_NORM3	12	3810	T20-5	T20-5	SRCA Collimator ref det for normaliztion sample 3	A	A	C0003/C0004	08F3	CE03A21T
15	SR	VR_SR_SRC_A_RAD	12	3822	T20-5	T20-5	Output of temp stabilized Silicon photodiode A for SIS rad FB control; SW echo in HK T20-2	A	A	C0003/C0004	5973	MM10A03T
15	SR	VR_SR_SRC_B_RAD	12	3834	T20-5	T20-5	Output of temp stabilized Silicon photodiode B for SIS rad FB control; SW echo in HK T20-2	A	A	C0003/C0004	5AF3	MM10A06T
6,15	SR	CR_SR_A_ONE	1	3846	na	na	SRCA AON_BOFF=1, AOFF=0 by R cmd	D	na	40005	A	MM09D22T
6,15	SR	CR_SR_B_ONE	1	3847	na	na	SRCA BON_AOFF=1, BOFF=0 by R cmd	D	na	40005	B	MM09D23T
6,15	SR	CR_SR_GRAT_CH_AE	1	3848	na	na	SRCA Grating/Mirror Coarse Home A=0/Not=1 (see Note 12 &10.8.9.c)	DCE	na	C0001	8	na
6,15	SR	CR_SR_GRAT_CH_BE	1	3849	na	na	SRCA Grating/Mirror Coarse Home B=0/Not=1 (see Note 12 &10.8.9.c)	DCE	na	C0001	C	na
6,15	SR	CR_SR_GRAT_FH_AE	1	3850	na	na	SRCA Grating/Mirror Fine Home A=0/Not=1(see Note 12 & 10.8.9.c)	DCE	na	C0001	9	na
6,15	SR	CR_SR_GRAT_FH_BE	1	3851	na	na	SRCA Grating/Mirror Fine Home B=0/Not=1 (see Note 12 & 10.8.9.c)	DCE	na	C0001	D	na
6,15	SR	CR_SR_IR_SRCOFFE	1	3852	na	na	SRCA IR Source ON/OFF = 0/1 , (see Note 12)	DCE	na	C0001	1	na
6,15	SR	CR_SR_LAMPS_LOWE	1	3853	na	na	SRCA Lamp Level Low/High =0/1, Low is normal BOL	SW	na	na	na	na
6,15	SR	CR_SR_LSHDN_ENAE	1	3854	na	na	SRCA SIS LAMP overvoltage Enabled/Disabled=0/11 (see Note 12)	DCE	na	C0001	4	na
6,15	SR	CR_SR_SISFB_RADE	1	3855	na	na	SRCA SIS feedback control to Rad/Current=0/1 (see Note 12)	DCE	na	C0001	3	na
6,15	SR	CR_SR_SISHTROFFE	1	3856	na	na	SRCA SIS det Htr ON/OFF=0/1 (see Note 12)	DCE	na	C0001	2	na
6,15	SR	CR_SR_SLIT_HOMAE	1	3857	na	na	SRCA Slit Home A=0/Not Home=1 (see Note 12)	DCE	na	C0001	A	na
6,15	SR	CR_SR_SLIT_HOMBE	1	3858	na	na	SRCA Slit Home B=0/Not Home=1 (see Note 12)	DCE	na	C0001	E	na
6,15	SR	CR_SR_WHL_HOMEAE	1	3859	na	na	SRCA Source Wheel Home A=0/Not Home=1 (see Note 12)	DCE	na	C0001	B	na
6,15	SR	CR_SR_WHL_HOMEBE	1	3860	na	na	SRCA Source Wheel Home B=0/Not Home=1 (see Note 12)	DCE	na	C0001	F	na
6,15	SR	CS_SR_GRAT_STEPE	16	3861	D# 0-61199 steps	Col 7	Grating/Mirror mtr absolute step count=D#(16bits), max=61199; (~0.006°/step); Home=Mirror=0 step; can rotate 360°	SW	na	na	na	na
6,15	SR	CS_SR_LAMPSE	3	3877	1W/10W/ 20W	col 7	OFF/WATT_ONE/WATT10/WATT20/WATT30 = 000/001/010 /011/100	SW	na	na	na	na
6,15	SR	CS_SR_SLIT_STEPE	6	3880	D# 0 - 48 steps	Col 7	Slit mtr absolute step=D#(6 bits), max=48; (3.75°/step); 0 step=Slit Reticle, 24 steps=Along Scan Reticle (tlmy Home), 48 steps=Along Track Reticle; hard stops just beyond 0 & 48 steps	SW	na	na	na	na
6,15	SR	CS_SR_SRCWH_STPE	7	3886	D# 0 - 119 steps	Col 7	Filter Wheel mtr absolute step=D#(7 bits), max=100; (3°/step); 0 step=ND Filter, 20 steps=Open (tlmy Home), 40 steps=Order Filt#1, 60 steps=Order Flt#2, 80 steps=Order Filr#3, 100 steps=Beam combiner; rel steps can rotate 360°	SW	na	na	na	na
6,15	SR	CS_SR_USEL10WX1E	4	3893	1 of 4	Col 7	SRCA 10WX1 lamp use with B#1/0 for ea bit for lamps 1,2,3,4	SW	na	na	na	na
6,15	SR	CS_SR_USEL10WX2E	4	3897	2 of 4	Col 7	SRCA 10WX2 lamp use with B#1/0 for ea bit for lamps 1,2,3,4	SW	na	na	na	na
6,15	SR	CS_SR_USEL10WX3E	4	3901	3 of 4	Col 7	SRCA 10WX3 lamp use with B#1/0 for ea bit for lamps 1,2,3,4	SW	na	na	na	na
6,15	SR	CS_SR_USEL1WX1E	2	3905	1 of 2	Col 7	SRCA 1WX1 lamp with B#1/0 ea AB from lamps 5,6	SW	na	na	na	na
6,15	SR	TA_SR_IR_SRC_AE	12	3907	-55 to +200°C	T20-5	IR source A temp	A	U27	C0003/C0004	55F3	MM09A06T
6,15	SR	TA_SR_IR_SRC_BE	12	3919	-55 to +200°C	T20-5	IR source B temp	A	U26	C0003/C0004	4EF3	MM09A20T
6,15	SR	TA_SR_SRC_A_SPDE	12	3931	-43 to +85°C	T20-5	Temp of Silicon photodiode A for SIS rad FB control	A	U27	C0003/C0004	5673	MM09A07T

TABLE 30-5D. MODIS ENGINEERING GROUP 1 PACKET 2 DATA FIELD

ENGINEERING DATA (1792 bits) - BB, FAM, SAM, SDSM & SRCA Data

User interest may be limited to Columns 1, 2 & 7 - - See Notes at table bottom for description of columns. *5/97*

pf chgs	1 Subsystem	2 Mnemonic Name	3 # of Bits	4 Pkt#2 Start Bit	5 Approx Tlmy Range	6 Scale & Limit	7 Remarks	8 Tlmy Type	9 Analog Mux	10 HW Addr/Read	11 HW Data	12 Design Unique ID
6,15	SR	TA_SR_SRC_B_SPDE	12	3943	-43 to +85°C	T20-5	Temp of Silicon photodiode B for SIS rad FB control	A	U27	C0003/C0004	56F3	MM09A08T
6,15	SR	TP_SR_GRAT_ELEXE	9	3955	-43 to +85°C	T20-6	Grating motor drive board temp	P	U10	C0003/C0004	139B	CE03A05T
6,15	SR	TP_SR_GRAT_MTRE	9	3964	-43 to +85°C	T20-6	SRCA grating motor temp	P	U10	C0003/C0004	141B	CE03A06T
6,15	SR	TP_SR_LAMP_RINGE	9	3973	-43 to +85°C	T20-6	SIS lamp ring temp	P	U10	C0003/C0004	119B	CE03A01T
6,15	SR	TP_SR_MIR2_DETE	9	3982	-43 to +85°C	T20-6	Near secondary mirror diode temp	P	U10	C0003/C0004	131B	CE03A04T
6,15	SR	TP_SR_MONO_CHS1E	9	3991	-43 to +85°C	T20-6	Monochromator chassis1 temp	P	U10	C0003/C0004	149B	CE03A11T
6,15	SR	TP_SR_MONO_CHS2E	9	4000	-43 to +85°C	T20-6	Monochromator chassis2 temp	P	U10	C0003/C0004	129B	CE03A03T
6,15	SR	TP_SR_SNOUTE	9	4009	-43 to +85°C	T20-6	Output collimator of SRCA temp	P	U10	C0003/C0004	121B	CE03A02T
10,15	AO	TA_AO_NIR_FPAE	12	4018	-23 to +85°C	T20-6	NIR warm FPA temp	A	U28	C0003/C0004	5F75	MM11A27T
10,15	AO	TA_AO_VIS_FPAE	12	4030	-23 to +85°C	T20-6	VIS warm FPA temp	A	U28	C0003/C0004	5EF5	MM11A25T
10,15	RC	TA_RC_LWIR_CFPAE	12	4042	82K to 88K	T20-5	RC LWIR FPA temp; range shifts with set point	A	U28	C0003/C0004	5E75	MM11A23T
10,15	RC	TA_RC_SMIR_CFPAE	12	4054	60K to 100K	T20-5	RC SMIR FPA temp; fixed range temp	A	U28	C0003/C0004	5DF5	MM11A21T
10,15	MF	TP_MF_CALBHD_SRE	9	4066	-23 to +85°C	T20-6	MF inside temp: -X Cal blkhd below SRCA mnt; TV sys ref temp	P	U8	C0003/C0004	19AB	MF00A03T
10,15	SA	TP_SA_A_MTRE	9	4075	-23 to +85°C	T20-6	Scan mtr temp A (no B)	P	U11	C0003/C0004	345B	SA00A02T
10,15	SA	TP_SA_RCT1_MIRE	12	4084	-23 to +85°C	T20-6	Scan Assy mirror radiatively coupled temp 1 monitor	P	U11	C0003/C0004	365B	SA00A05T
10,15	SA	TP_SA_RCT2_MIRE	12	4096	-23 to +85°C	T20-6	Scan Assy mirror radiatively coupled temp 2 monitor	P	U11	C0003/C0004	375B	SA00A07T
10,15	XX	FILL BITS	4	4108	na	na	Fill bits to provide subfield divisible by 12 to facilitate HW xfers	na	na	na	na	na
10,15	***199***	***<--Col 1 & 3 Totals-->***	***1696***	***4111***		***<--Last Pkt bit, for local field bits subtrtact 2416.***						

15 "E" suffix in name differentiates Engineering Packet item from original same item in 1553 Housekeeping Telemetry.

TABLE 30-5D. MODIS ENGINEERING GROUP 1 PACKET 2 DATA FIELD

ENGINEERING DATA (1792 bits) - BB, FAM, SAM, SDSM & SRCA Data

User interest may be limited to Columns 1, 2 & 7 - - See Notes at table bottom for description of columns. *5/97*

pf chgs	1 Subsystem	2 Mnemonic Name	3 # of Bits	4 Pkt#2 Start Bit	5 Approx Tlmy Range	6 Scale & Limit	7 Remarks	8 Tlmy Type	9 Analog Mux	10 HW Addr/Read	11 HW Data	12 Design Unique ID

Notes: (Most entries are processed in similar manner as the Table 20-2A telemetry items.)

1. Column 1 is Subsystem 2-alpha code defined by 151840 Table 10 or Figure 11. All items are outputted each 1.477 sec scan cycle.

2. Column 2 Mnemonic Name is 2nd 16 character field of OASIS name. First 16 character field (not shown) contains External Element, which is MOD.
   Leading 2 characters indicate :
   1st character: C = configuration, I = current, S = status, T = temperature, V = voltage
   2nd character: A = active analog, D = pseudo or derived, R = real or raw data, S = flight software generated, P = passive analog.

3. Column 3 indicates the number of bits (status or digital value) for each item.

4. Column 4 indicates the starting bit location within Engineering 2 Packet Segment#2.

5. Column 5 provides nominal analog tlmy range.

6. Column 6 points toreference for analog scale factors and limits.

7. Column 7 provides remarks. Some items have SW echo in HK T20-2A, or a similar type pt.

8. Column 8 is a tlmy processing type code: A = active analog direct, APC = analog via 1 of 6 PC muxes (FAM), APV = active analog via 1 of 1 PV mux (SAM), SW = software.

9. Column 9 is analog mux processing group on the CP analog telemetry board.

10. Columns 10 & 11 provide analog/digital hardware hex data address & location. See Table 20-3 for PC & PV mux data locations.

11. Column 12 is a Unique ID for hardware related items.

TABLE 30-5D. MODIS ENGINEERING GROUP 1 PACKET 2 DATA FIELD

ENGINEERING DATA (1792 bits) - BB, FAM, SAM, SDSM & SRCA Data

User interest may be limited to Columns 1, 2 & 7 - - See Notes at table bottom for description of columns.

5/97

pf chge	1 Subsystem	2 Mnemonic Name	3 # of Bits	4 Pkt#2 Start Bit	5 Approx Tlmy Range	6 Scale & Limit	7 Remarks	8 Tlmy Type	9 Analog Mux	10 HW Addr/Read	11 HW Data	12 Design Unique ID

Table 30-5D Change History [X] = General table notes.

1. 11/24/95 Revised sample delay range on 4 PV FPAs, e.g., CR_PVVIS_S_DELAY to 0-50 from 0-63 units of 3.33µs.

[2] 11/24 Interchanged data in Columns 5 & 6 so the data is now in the same sequence as Table 20-2 Tlmy.

3. 1/5/96 Partition CS_SM_MIR_VIEW into 3pt (1/ea sample): SS_SM_VIEW_SMPL1, SS_SM_VIEW_SMPL2, SS_SM_VIEW_SMPL3. Chged Cum/Start bits.
4. 1/5/96 Update center wavelength values & show related MODIS band in Remarks col of all VR_SM0X_SMPL1,2,3.

[5] 5/4/96 Delete Col 3b Table CumBits & renumber Col 3a to 3.

6. 5/4/96 Add 34 SR items as SW echo from T20-2A. New items have slightly changed name ending in "E" to distinguish source of signals. Also turn double entry VR_PC_B33C10 into SS_PC_SPARE slot.

----------Split for chgs since 5/8/96 Initial Release----------

7. 8/12/96 Adjust starting bit locations at start bit 2741 to allow insertion of missing VR_PC_B32C01_DCR. This ripples signal start bits down to start bit 2821, which is now VR_PC_B33C01_DCR instead of being a Spare.
8. 8/12/96 Correct Col 11 HW Data location on six SM (SDSM) items begining at VR_SM09_SMPL1. (3pl OD7C from OD79 & 3pl OE7E from OE7D.)
9. 9/16/96 Col 7 Remarks minor chgs to 2 of 9 VR_SM0X_SMPLX detector filter center wavelengths based on measured filter data.
10. 9/16/96 Add 8 1553 bus temperature points at end out of subsytem sequence. Add suffix E to name to distinguish from HK tlmy.
11. 9/17/96 Chg table title from T30-5C to T30-5D, and use Group vs Segment packet terminology.

[12] 11/8/96 provide info for Columns 5 & 6.

13. 11/8/96 Update SR data for lamp use and mtr position defintions.
14. 12/2/96 Reverse the sequence of Col 11 addsresses on VR_SM01_SMPLX through VR_SM09_SMPLX.
15. 4/97 Multiple EO1122D incoporations for Rev B. See EO1122D (released 970305) for details (mostly spare deletions, which affected pkt start bit).

TABLE 30-6A. MODIS ENGINEERING GROUP 2 PACKET 1 DATA FIELD

CURRENT/PRIOR HOUSEKEEPING TELEMETRY DATA(512 BITS/EA)

Contains latest 2 rotating 512-bit telemetry fields.

Current 512 bits - with Major Cycle 1 as sample 5/97

Pkt Start Bit	Major Cycle 1 Word	# of bits	512 Field start-end	# of words	General Frame Structure Major Cycle Borders	
144	SS_CP1553_MAJCYC	6	000-005			↑
etc	*etc*		*etc*		***1 sec samples***	
				20W	20W x 16b/W = 320 bits	
429	FILL_BITS	35	285-319		repeats every major cycle	↓
464	TP_BB_TEMP09H	12	320-331			↑
etc	*etc*		*etc*		***8 sec samples***	
				8W	8W x 16b/W = 128 bits	
579	FILL_BITS	12	436-447		repeats every 8 major cycles	↓
592	TP_AO_VNDICH_HSG	12	448-459			↑
etc	*etc*		*etc*		***65 sec samples***	
				4W	4W x 16b/W = 64 bits	
655	FILL_BITS	1	511-511		unique each major cycle	↓

Prior 512 Bits - with Major Cycle 0 as sample

Pkt Start Bit	Major Cycle 0 Word	# of bits	512 Field start-end	# of words	General Frame Structure Major Cycle Borders	
656	SS_CP1553_MAJCYC	6	000-005			↑
etc	*etc*		*etc*		***1 sec samples***	
				20W	20W x 16b/W = 320 bits	
941	FILL_BITS	35	285-319		repeats every major cycle	↓
976	CR_BB_A_PWR_ON	1	320-320			↑
etc	*etc*		*etc*		***8 sec samples***	
				8W	8W x 16b/W = 128 bits	
1103	FILL_BITS	1	447-447		repeats every 8 major cycles	↓
1104	TP_AO_LWIR_LENS	12	448-457			↑
etc	*etc*		*etc*		***65 sec samples***	
				4W	4W x 16b/W = 64 bits	
1167	FILL_BITS	4	508-511		unique each major cycle	↓

Notes:

1. Samples are partial structures for 1553 Major Cycle 1 and Major Cycle 0.
2. Note the general frame structure as shown by right half of table.
3. Both Pkt start bit location and local 512-bit field start/end locations are listed.
4. To decode each 512 bit field, determine the major cycle (0-63) from the first word. Then from Table 20-4 HK Frame Definition determine unique structure for that Major Cycle.
5. See Table 20-2A for data on individual words.

TABLE 30-6B. MODIS ENGINEERING GROUP 2 PACKET 1 DATA FIELD
CURRENT/PRIOR S/C ANCILLARY DATA (512 BITS/EA)

CURRENT S/C ANCILLARY DATA (512 BITS) 10/96

Pkt Start Bit	# of Bits	Hex Value	Word Description	Units	Format	Scaling
1168	48		Packet Header	na	na	na
1216	1		Secondary Header ID Flag	na	na	na
1217	63		Time Stampe	microsec	CDS	na
1280	8		Flag Byte	na	na	na
1288	24		Time Conversion	microsec	2C	0
1312	32		S/C Position - X	meters	2C	-3
1344	32		S/C Position - Y	meters	2C	-3
1376	32		S/C Position - Z	meters	2C	-3
1408	32		S/C Veleocity - X	meters/sec	2C	-12
1440	32		S/C Veleocity - Y	meters/sec	2C	-12
1472	32		S/C Veleocity - Z	meters/sec	2C	-12
1504	4		Reserved	-	-	-
1508	12		Attitude Angle - Roll	arcsec	2C	0
1520	4		Reserved	-	-	-
1524	12		Attitude Angle - Pitch	arcsec	2C	0
1536	4		Reserved	-	-	-
1540	12		Attitude Angle - Yaw	arcsec	2C	0
1552	4		Reserved	-	-	-
1556	12		Attitude Rate - Roll	arcsec/sec	2C	0
1568	4		Reserved	-	-	-
1572	12		Attitude Rate - Pitch	arcsec/sec	2C	0
1584	4		Reserved	-	-	-
1588	12		Attitude Rate - Yaw	arcsec/sec	2C	-1
1600	8		Magnetic Coil Current - X	Amperes	2C	-6
1608	8		Magnetic Coil Current - Y	Amperes	2C	-6
1616	8		Magnetic Coil Current - Z	Amperes	2C	-6
1624	8		Solar Array Current	Amperes	US	0
1632	8		Solar Position - X	na	2C	-7
1640	8		Solar Position - Y	na	2C	-7
1648	8		Solar Position - Z	na	2C	-7
1656	8		Moon Position - X	na	2C	-7
1664	8		MoonPosition - Y	na	2C	-7
1672	8		Moon Position - Z	na	2C	-7
1679	<-End 1st 512 bit field		See GSFC 420-03-02 GIIS Tables 6-2 & 6-3 for details.			

TABLE 30-6B. MODIS ENGINEERING GROUP 2 PACKET 1 DATA FIELD
CURRENT/PRIOR S/C ANCILLARY DATA (512 BITS/EA)

PRIOR S/C ANCILLARY DATA (512 BITS) 5/97

Pkt Start Bit	# of Bits	V alue	Word Description	Units	Format	Scaling
1680	48		Packet Header	na	na	na
1728	1		Secondary Header ID Flag	na	na	na
1729	63		Time Stampe	microsec	CDS	na
1792	8		Flag Byte	na	na	na
1800	24		Time Conversion	microsec	2C	0
1824	32		S/C Position - X	meters	2C	-3
1856	32		S/C Position - Y	meters	2C	-3
1888	32		S/C Position - Z	meters	2C	-3
1920	32		S/C Veleocity - X	meters/sec	2C	-12
1952	32		S/C Veleocity - Y	meters/sec	2C	-12
1984	32		S/C Veleocity - Z	meters/sec	2C	-12
2016	4		Reserved	-	-	-
2020	12		Attitude Angle - Roll	arcsec	2C	0
2032	4		Reserved	-	-	-
2036	12		Attitude Angle - Pitch	arcsec	2C	0
2048	4		Reserved	-	-	-
2052	12		Attitude Angle - Yaw	arcsec	2C	0
2064	4		Reserved	-	-	-
2068	12		Attitude Rate - Roll	arcsec/sec	2C	0
2080	4		Reserved	-	-	-
2084	12		Attitude Rate - Pitch	arcsec/sec	2C	0
2096	4		Reserved	-	-	-
2100	12		Attitude Rate - Yaw	arcsec/sec	2C	-1
2112	8		Magnetic Coil Current - X	Amperes	2C	-6
2120	8		Magnetic Coil Current - Y	Amperes	2C	-6
2128	8		Magnetic Coil Current - Z	Amperes	2C	-6
2136	8		Solar Array Current	Amperes	US	0
2144	8		Solar Position - X	na	2C	-7
2152	8		Solar Position - Y	na	2C	-7
2160	8		Solar Position - Z	na	2C	-7
2168	8		Moon Position - X	na	2C	-7
2176	8		MoonPosition - Y	na	2C	-7
2184	8		Moon Position - Z	na	2C	-7
2191	<-End 2nd 512 bit field		See GSFC 420-03-02 GIIS Tables 6-2 & 6-3 for details.			

Table 30-6B Notes:

1. MODIS does not use any of this ancillary data in orbit. It comes from the S/C via 1553 Bus Subaddress 4, and is placed in the engineering packet for ground use.
2. To convert Current Data Pkt bits to local 512-bit field, subtract 1168.
3. To convert Prior Data Pkt bits to local 512-bit field, subtract 1680.
4. See GSFC 420-03-02 GIIS Tables 6-2 & 6-3 for further ancillary notes and details.

Table 30-6B Change History [x] = General Comment.

[1] 9/18/96 Redefine packet start location. Contents are the same.

[2] 10/22/96 Define explicit pkt bit table layout to facilitate IGSE TAC readout algorithm.

TABLE 30-6C. MODIS ENGINEERING GROUP 2 PACKET 1 DATA FIELD
COMMAND PARAMETER DATA (320 bits)

5/97

pf chgs	1 Subsys	2 Parameter (OASIS Command Name)	3 # of Bits	4 General Remarks	5 Prm ID#	6 Pkt Start Bit	7 Field 16-bit Word	8 Field Cum Bits
7	BB04	SET_BB_HTR_TEMP	12	Sets BB heater temp set point to D#XXXX	1	2192	0	12
	CP07	SET_CP_OPER_MODE	3	Set Oper Mode to: Survival, Safe, Standby, OG, Science, Test (Test=formatter test pattern for link check)	16	2204	0	15
	FR07	SET_FR_RATE	1	Sets FR rate to B#X=1/0: 1=DAY, 0=NIGHT	23	2207	0	16
	FR08	SET_FR _SCI_APID	11	Set Sci FPA APID D# 064-127 in science packet header	5	2208	1	27
7	SR07	SET_SR_L10WX1	4	Set initial 1x10W lamps to B#1/0 ea ABCD from lamps 1,2,3,4	20	2219	1	31
7	FR26	SET_FR_PKT_TYPE	1	Set FR Sci Pkt to Test=1,Normal=0; test creates fixed CCSDS pkt to check link	51	2223	1	32
1	PV05	SET_PVVIS_VCAL	8	Set PV VIS VCAL volts to -8V to +1V (spread over 8 binary bits)	35	2224	2	40
1	PV11	SET_PVNIR_VCAL	8	Set PV NIR VCAL volts to -8V to +1V (spread over 8 binary bits)	38	2232	2	48
1	PV17	SET_PVSM_VCAL	8	Set PV SMIR VCAL to -8V to +1V (spread over 8 binary bits)	41	2240	3	56
1	PV25	SET_PVLW_VCAL	8	Set PV LWIR VCAL to -8V to +1V (spread over 8 binary bits)	45	2248	3	64
7	PV06	SET_PVVIS_ITWK_V	8	Set PV VIS ITWK to -2.5V to -4.5V (spread over 8 binary bits)	36	2256	4	72
7	PV12	SET_PVNIR_ITWK_V	8	Set PV NIR ITWK to -2.5V to -4.5V (spread over 8 binary bits)	39	2264	4	80
7	PV19	SET_PVSM_ITWK_V	8	Set PV SMIR ITWK to -2.5V to -4.5V (spread over 8 binary bits)	42	2272	5	88
7	PV27	SET_PVLW_ITWK_V	8	Set PV LWIR ITWK to -2.5V to -4.5V (spread over 8 binary bits)	46	2280	5	96
	PV20	SET_PVSM_VDET_V	8	Set PV SMIR VDET to 0V to -8V (spread over 8 binary bits)	43	2288	6	104
	PV28	SET_PVLW_VDET_V	8	Set PV LWIR VDET to 0V to -8V (spread over 8 binary bits)	47	2296	6	112
	FR11	SET_FR_ENG_APID	11	Set Sci Eng APID D# 064-127 in engineering packet header	7	2304	7	123
7	SR06	SET_SR_L10WX2	4	Set initial 2x10W lamps to B#1/0 ea ABCD from lamps 1,2,3,4	19	2315	7	127
	CP04	ENABLE_CP_IMOK	1	Enable=1 (Disable=0) for CP 5 sec monitor of SCC IMOK/sec	17	2319	7	128
	CP05	DISABLE_CP_IMOK	1	Disable=0 (Enable=1) for CP 5 sec monitor of SCC IMOK/sec	17	2319	7	128
	FR32	SET_FR_BBRADTAB	1	FR BB radiation-vs-temp table to Normal/Test=1/0	60	2320	8	129
	FR33	SET_FR_OFFSETTAB	1	FR Offset table to Normal/Test=1/0	61	2321	8	130
	FR34	SET_FR_GAINTAB	1	FR gain table to Normal/Test=1/0	62	2322	8	131
	FR35	TEST_FR_BBRAD	12	Sets fixed BB radiation value=X#XXX; no HK tlmy	63	2323	8	143
	FR09	SET_FR_SCI_QLK	1	Sets FPA quick look flag to 1 in science packet header	6	2335	8	144
	FR10	RESET_FR_SCI_QLK	1	Resets FPA quick look flag to 0 in science packet header	6	2335	8	144
3	FR18	SET_FR_SR_DELAY	7	Set SRCA view FPA delay to D#XXX(0-50) 0.02IFOVs,1km	12	2336	9	151
3	FR19	SET_FR_BB_DELAY	7	Set BB view FPA delay to D#XXX(0-50) 0.02IFOVs,1km	13	2343	9	158
	CP06	SET_CP_TMF_BUS	1	Set CP TMF Bus to B#X=1/0: 1=B, 0=A	2	2350	9	159
	DR03	OPEN_DR_UL_LOCK	1	Allows activating any DR unlatch cmd if received just prior to it	29	2351	9	160
3	FR17	SET_FR_SD_DELAY	7	Set SD view FPA delay to D#XXX(0-50) 0.02IFOVs,1km	11	2352	10	167
3	FR20	SET_FR_SP_DELAY	7	Set Space view FPA delay to D#XXX(0-50) 0.02IFOVs,1km	14	2359	10	174
	PV31	SET_PV_MEM	1	Set PV active side MEM to ROM/RAM, B# 1=ROM, 0=RAM	50	2366	10	175
	FR12	SET_FR_ENG_QLK	1	Sets Sci Eng quick look flag to 1 in engineering packet header	8	2367	10	176

TABLE 30-6C. MODIS ENGINEERING GROUP 2 PACKET 1 DATA FIELD
COMMAND PARAMETER DATA (320 bits)

5/97

pf chgs	1 Subsys	2 Parameter (OASIS Command Name)	3 # of Bits	4 General Remarks	5 Prm ID#	6 Pkt Start Bit	7 Field 16-bit Word	8 Field Cum Bits
	FR13	RESET_FR_ENG_QLK	1	Resets Sci Eng quick look flag to 0 in engineering packet header	8	2367	10	176
5	CP21	CP_SPARE	12	Was SET_CP_PK_PWR	22	2368	11	188
	SR05	SET_SR_3L10W	4	Set initial 3x10W lamps to B#1/0 ea ABCD from lamps 1,2,3,4	18	2380	11	192
	FR31	SET_FR_ENC_DELTA	14	Delta rotates all view collects, D# to 14-bit X# by 2sC	59	2384	12	206
	PV16	SET_PVSMIR_ECAL	1	PV SMIR A or B elex calibration, B# 1=ON, 0=OFF	40	2398	12	207
	PV24	SET_PVLW_ECAL	1	PV LWIR A or B elex calibration, B# 1=ON, 0=OFF	44	2399	12	208
	FR37	TEST_FR_PCOFFSET	16	Sets fixed PC offset value=X#XXYY, where XX=preamp, YY=postamp	65	2400	13	224
	FR36	TEST_FR_PVOFFSET	8	Sets fixed PV offset value=X#XX	64	2416	14	232
	FR38	TEST_FR_PVGAIN	8	Sets fixed PV gain value=X#XX	66	2424	14	240
	PV32	SET_PVVIS_NSTEP	8	Sets VIS FPA step cycles of chrg injection, D#XX ≤ 40	67	2432	15	248
	PV33	SET_PVNIR_NSTEP	8	Sets NIR FPA step cycles of chrg injection, D#XX ≤ 40	68	2440	15	256
	PV34	SET_PVSM_NSTEP	8	Sets SM FPA step cycles of chrg injection, D#XX ≤ 40	69	2448	16	264
	PV35	SET_PVLW_NSTEP	8	Sets LW FPA step cycles of chrg injection, D#XX ≤ 10	70	2456	16	272
3	FR21	SET_FR_EA_DELAY	7	Set Earth view FPA delay to D#XXX(0-50) 0.02IFOVs,1km	15	2464	17	279
	PV18	SET_PVSMIR_CSUB	1	Test only, PV SMIR chrg subtraction active side to 1=ON, 0=OFF	48	2471	17	280
	PV26	SET_PVLW_CSUB	1	Test only-PV LWIR chrg subtraction, active side to 1=ON, 0=OFF	49	2472	17	281
7	DR04	SET_DR_SVD_UL	1	SVD unlatch paraffin htr: 0=ON, 1=OFF; Flt SW timer has 3 min OFF	30	2473	17	282
7	DR05	SET_DR_NAD_UL	1	NAD unlatch paraffin htr: 0=ON, 1=OFF; Flt SW timer has 3 min OFF	31	2474	17	283
7	DR06	SET_DR_SDD_UL	1	SDD unlatch paraffin htr: 0=ON, 1=OFF; Flt SW timer has 3 min OFF	32	2475	17	284
7	DR27	SET_DR_SDD_FS	1	4th & final FS step, SDD FS htr: 0=ON, 1=OFF; Flt SW timer has 3 min OFF	33	2476	17	285
	FR29	SET_FR_PV_DCRCMP	1	PV DCR Computation: 1=ON, 0=OFF	52	2477	17	286
	FR27	SET_FR_PC_DCRCMP	1	PC DCR Computation: 1=ON, 0=OFF	53	2478	17	287
6	FR45	FR_SPARE	1	Was SET_FR_PCDCRPRE	56	2479	17	288
5	FR43	FR_SPARE	1	Was SET_FR_PCDCRDBG	58	2480	18	289
	SR04	SET_SR_SIPD_HTR	1	Turns SRCA SIS RAD SIPD Htr ON/OFF = 1/0	71	2481	18	290
	SR09	SET_SR_SIS_FB	1	Set SRCA SIS Feedback control to Radiance/Current = 1/0	72	2482	18	291
	SR10	SET_SR_LOV_SHDN	1	Set SRCA Lamp OverVoltage Shutdown to Enable/Disable=0/1	73	2483	18	292
	SR11	SET_SR_LAMPLEVEL	1	Set SRCA Lamp Level to High/Low = 1/0, Low is normal BOL	74	2484	18	293
	SR12	SET_SR_LAMPS	3	Set SRCA lamps to OFF/W1/W10/W20/W30.	75	2485	18	296
	CP26	SET_CP_LOG_STATE	4	Sets OPERAND & INSTRUCTION class of loads (& dumps)	77	2488	18	300
	FR46	SET_FR_LOG_STATE	4	Sets OPERAND & INSTRUCTION class of loads (& dumps)	78	2492	18	304
	SR21	SET_SR_IR_SRC	1	Turns SRCA IR source ON/OFF = 1/0	76	2496	19	305
5	FR44	FR_SPARE	1	Was SET_FR_PCDCRPOST	57	2497	19	306
7	SR08	SET_SR_L1WX1	2	Set initial 1x1W lamps to B#1/0 ea AB from lamps 5,6	21	2498	19	308
	PV04	SET_PVVIS_ECAL	1	PV VIS A or B elex calibration, B# 1=ON, 0=OFF	34	2500	19	309
	PV10	SET_PVNIR_ECAL	1	PV NIR A or B elex calibration, B# 1=ON, 0=OFF	37	2501	19	310

TABLE 30-6C. MODIS ENGINEERING GROUP 2 PACKET 1 DATA FIELD
COMMAND PARAMETER DATA (320 bits)

5/97

pf chgs	1 Subsys	2 Parameter (OASIS Command Name)	3 # of Bits	4 General Remarks	5 Prm ID#	6 Pkt Start Bit	7 Field 16-bit Word	8 Field Cum Bits
8	FR16	SET_FR_SCIABNORM	1	0=ABNORM, 1=NORM for other than MODIS abnormal conditions	10	2502	19	311
	XXXX	FILL_BITS	9	Spare bits for software alignment	n/a	2503	19	320
	TG04	RESET_TG	na	Active TG Reset=0 (Flt SW steps 1, 0 for neg chg; no gnd SET cmd)	3	n/a	n/a	n/a
7	FR06	SPARE	na	Used to be SET_FR_FPA_DCR	4	n/a	n/a	n/a
7	FR14	SET_FR_MEM_APID	na	Set Sci Mem APID D# 064-127 in memory packet header	9	n/a	n/a	n/a
7	FR15	SET_FR_MEM_QLK	na	Sets MEM quick look flag to 1 in memory packet header	10	n/a	n/a	n/a
	FR04	TEST_FR_SELF	na	Active FR Test=0 (Flt SW steps 1, 0 for neg chg; no gnd RETEST cmd)	24	n/a	n/a	n/a
	FR05	RESET_FR_STD	na	Active FR Reset=0 (Flt SW steps 1, 0 for neg chg; no gnd SET cmd; called B0 on dwgs)	25	n/a	n/a	n/a
	FR22	RESET_FR_UPLD	na	Active FR Reset=0 (Flt SW steps 1, 0 for neg chg; no gnd SET cmd; called B1 on dwgs)	26	n/a	n/a	n/a
4	FO06	FO_SPARE	na	FO_SPARE (was RESET_FO; fast transient)	27	n/a	n/a	n/a
	FI04	RESET_FI	na	Active FI Reset=0 (Flt SW steps 1, 0 for neg chg; no gnd SET cmd)	28	n/a	n/a	n/a
2	FR30	FR_SPARE	na	na (was SET_FR_PV_DCR_TH)	54	n/a	n/a	n/a
2	FR28	FR_SPARE	na	na (was SET_FR_PC_DCR_TH)	55	n/a	n/a	n/a
			320	<-- tot bits (excludes double entry for Prm 6, 10 & 17)	Pkt end bit = 2511			

TABLE 30-6C. MODIS ENGINEERING GROUP 2 PACKET 1 DATA FIELD

COMMAND PARAMETER DATA (320 bits)

5/97

pl chgs	1 Subsys	2 Parameter (OASIS Command Name)	3 # of Bits	4 General Remarks	5 Prm ID#	6 Pkt Start Bit	7 Field 16-bit Word	8 Field Cum Bits

NOTES:

1. This table shows the layout of the command parameter status transfered once per scan as 20x16-bit words from the CP to the FR. The prime command list is Table 10-25, and Table 10-22 provides more definition of the parameter type commands.
2. Column 6 is the Packet start bit location. Bit positions are per MIL-STD-1750 notation with MSB=0, LSB=15.
3. Parameters for the Quick Look Flags (6 and 10), and CP_IMOK flag (17) are listed twice (at the same bit location) because two toggle commands exist for each (set/ reset).
4. Parameters after Fill_BITS at the end of the table are listed for completeness, but are not transferred in the block because they relate to short pulse commands in the CP or to Spares.

T30-6C Change History [X] = General table notes.

1. 11/24/95 Chg ECAL_V to VCAL 4pl PV05, 11, 17, 25.
2. 11/24/95 (other tables chged 11/4) Chg FR28 SET_FR_PC_DCR_TH to FR_SPARE, and SET_FR_PV_DCR_TH to FR_SPARE.
3. 11/24/95 Chg Remarks on FR17-FR21 (e.g.SET_FR_SD_DELAY) to note unit delay=0.02 IFOV (6.66μs), not 0.01 IFOV (3.33μs) and range=0-50 vs 100 units.
4. 11/24 (Other table chgs made 11/6) Chg RESET_FO to FO_SPARE.

——————Changes since 151840 initial 5/96 release——————

5. 8/15/96 Chg CP21, FR43, FR44 & FR45 to spares. See T10-25A Change History for names.
6. 9/18/96 Revise table # to T30-6C and use "Group" vs "Segment" terminology. Also packet location was changed.
7. 10/22/96 Minor syntax, or name correction, or values to be compatible with T10-25A.
8. 10/22/96 Reactivated FR16 to use as SET_FR_SCIABNORM to ABNORM/NORM to set flag for abnormal conditions other than MODIS.

[9] 10/22/96 Added inadvertent missing cmd parameters from #56 on (which were all in T10-22).

TABLE 30-7. MODIS ENGINEERING GROUP 2 PACKET 2 DATA FIELD
PV GAIN DATA (4400 bits)

Sort by Pkt Start Bit — 550 words x 8 bits

Pkt Start Bit	Memory Table Word Offset	Band	Det	Gain Hex	PC Comments
144	0	1	1	XX	
152	1	1	2	XX	
160	2	1	3	XX	
168	3	1	4	XX	
176	4	2	1	XX	
184	5	2	2	XX	
192	6	2	3	XX	
200	7	2	4	XX	
208	8	3	1	XX	
216	9	3	2	XX	
224	10	4	1	XX	
232	11	4	2	XX	
240	12	5	1	XX	
248	13	5	2	XX	
256	14	6	1	XX	
264	15	6	2	XX	
272	16	7	1	XX	
280	17	7	2	XX	
288	18	8	1	XX	
296	19	9	1	XX	
304	20	10	1	XX	
312	21	11	1	XX	
320	22	12	1	XX	
328	23	13L	1	XX	
336	24	13H	1	XX	
344	25	14L	1	XX	
352	26	14H	1	XX	
360	27	15	1	XX	
368	28	16	1	XX	
376	29	17	1	XX	
384	30	18	1	XX	
392	31	19	1	XX	
400	32	20	1	XX	
408	33	21	1	XX	
416	34	22	1	XX	
424	35	23	1	XX	
432	36	24	1	XX	
440	37	25	1	XX	
448	38	26	1	XX	
456	39	27	1	XX	
464	40	28	1	XX	
472	41	29	1	XX	
480	42	30	1	XX	
488	43	31	1	na	postamp
496	44	31	1	na	preamp
504	45	32	1	na	postamp
512	46	32	1	na	preamp
520	47	33	1	na	postamp
528	48	33	1	na	preamp
536	49	34	1	na	postamp
544	50	34	1	na	preamp
552	51	35	1	na	postamp
560	52	35	1	na	preamp
568	53	36	1	na	postamp
576	54	36	1	na	preamp
584	55	1	5	XX	
592	56	1	6	XX	

Reference Sort by Band/Det — 5/97

Pkt Start Bit	Memory Table Word Offset	Band	Det	PC Comments
144	0	1	1	
152	1	1	2	
160	2	1	3	
168	3	1	4	
584	55	1	5	
592	56	1	6	
600	57	1	7	
608	58	1	8	
1024	110	1	9	
1032	111	1	10	
1040	112	1	11	
1048	113	1	12	
1464	165	1	13	
1472	166	1	14	
1480	167	1	15	
1488	168	1	16	
1904	220	1	17	
1912	221	1	18	
1920	222	1	19	
1928	223	1	20	
2344	275	1	21	
2352	276	1	22	
2360	277	1	23	
2368	278	1	24	
2784	330	1	25	
2792	331	1	26	
2800	332	1	27	
2808	333	1	28	
3224	385	1	29	
3232	386	1	30	
3240	387	1	31	
3248	388	1	32	
3664	440	1	33	
3672	441	1	34	
3680	442	1	35	
3688	443	1	36	
4104	495	1	37	
4112	496	1	38	
4120	497	1	39	
4128	498	1	40	
176	4	2	1	
184	5	2	2	
192	6	2	3	
200	7	2	4	
616	59	2	5	
624	60	2	6	
632	61	2	7	
640	62	2	8	
1056	114	2	9	
1064	115	2	10	
1072	116	2	11	
1080	117	2	12	
1496	169	2	13	
1504	170	2	14	
1512	171	2	15	
1520	172	2	16	
1936	224	2	17	

TABLE 30-7. MODIS ENGINEERING GROUP 2 PACKET 2 DATA FIELD
PV GAIN DATA (4400 bits)

Sort by Pkt Start Bit — 550 words x 8 bits

Pkt Start Bit	Memory Table Word Offset	Band	Det	Gain Hex	PC Comments
600	57	1	7	XX	
608	58	1	8	XX	
616	59	2	5	XX	
624	60	2	6	XX	
632	61	2	7	XX	
640	62	2	8	XX	
648	63	3	3	XX	
656	64	3	4	XX	
664	65	4	3	XX	
672	66	4	4	XX	
680	67	5	3	XX	
688	68	5	4	XX	
696	69	6	3	XX	
704	70	6	4	XX	
712	71	7	3	XX	
720	72	7	4	XX	
728	73	8	2	XX	
736	74	9	2	XX	
744	75	10	2	XX	
752	76	11	2	XX	
760	77	12	2	XX	
768	78	13L	2	XX	
776	79	13H	2	XX	
784	80	14L	2	XX	
792	81	14H	2	XX	
800	82	15	2	XX	
808	83	16	2	XX	
816	84	17	2	XX	
824	85	18	2	XX	
832	86	19	2	XX	
840	87	20	2	XX	
848	88	21	2	XX	
856	89	22	2	XX	
864	90	23	2	XX	
872	91	24	2	XX	
880	92	25	2	XX	
888	93	26	2	XX	
896	94	27	2	XX	
904	95	28	2	XX	
912	96	29	2	XX	
920	97	30	2	XX	
928	98	31	2	na	postamp
936	99	31	2	na	preamp
944	100	32	2	na	postamp
952	101	32	2	na	preamp
960	102	33	2	na	postamp
968	103	33	2	na	preamp
976	104	34	2	na	postamp
984	105	34	2	na	preamp
992	106	35	2	na	postamp
1000	107	35	2	na	preamp
1008	108	36	2	na	postamp
1016	109	36	2	na	preamp
1024	110	1	9	XX	
1032	111	1	10	XX	
1040	112	1	11	XX	
1048	113	1	12	XX	

Reference Sort by Band/Det — 5/97

Pkt Start Bit	Memory Table Word Offset	Band	Det	PC Comments
1944	225	2	18	
1952	226	2	19	
1960	227	2	20	
2376	279	2	21	
2384	280	2	22	
2392	281	2	23	
2400	282	2	24	
2816	334	2	25	
2824	335	2	26	
2832	336	2	27	
2840	337	2	28	
3256	389	2	29	
3264	390	2	30	
3272	391	2	31	
3280	392	2	32	
3696	444	2	33	
3704	445	2	34	
3712	446	2	35	
3720	447	2	36	
4136	499	2	37	
4144	500	2	38	
4152	501	2	39	
4160	502	2	40	
208	8	3	1	
216	9	3	2	
648	63	3	3	
656	64	3	4	
1088	118	3	5	
1096	119	3	6	
1528	173	3	7	
1536	174	3	8	
1968	228	3	9	
1976	229	3	10	
2408	283	3	11	
2416	284	3	12	
2848	338	3	13	
2856	339	3	14	
3288	393	3	15	
3296	394	3	16	
3728	448	3	17	
3736	449	3	18	
4168	503	3	19	
4176	504	3	20	
224	10	4	1	
232	11	4	2	
664	65	4	3	
672	66	4	4	
1104	120	4	5	
1112	121	4	6	
1544	175	4	7	
1552	176	4	8	
1984	230	4	9	
1992	231	4	10	
2424	285	4	11	
2432	286	4	12	
2864	340	4	13	
2872	341	4	14	

TABLE 30-7. MODIS ENGINEERING GROUP 2 PACKET 2 DATA FIELD
PV GAIN DATA (4400 bits)

Sort by Pkt Start Bit — 550 words x 8 bits

Pkt Start Bit	Memory Table Word Offset	Band	Det	Gain Hex	PC Comments
1056	114	2	9	XX	
1064	115	2	10	XX	
1072	116	2	11	XX	
1080	117	2	12	XX	
1088	118	3	5	XX	
1096	119	3	6	XX	
1104	120	4	5	XX	
1112	121	4	6	XX	
1120	122	5	5	XX	
1128	123	5	6	XX	
1136	124	6	5	XX	
1144	125	6	6	XX	
1152	126	7	5	XX	
1160	127	7	6	XX	
1168	128	8	3	XX	
1176	129	9	3	XX	
1184	130	10	3	XX	
1192	131	11	3	XX	
1200	132	12	3	XX	
1208	133	13L	3	XX	
1216	134	13H	3	XX	
1224	135	14L	3	XX	
1232	136	14H	3	XX	
1240	137	15	3	XX	
1248	138	16	3	XX	
1256	139	17	3	XX	
1264	140	18	3	XX	
1272	141	19	3	XX	
1280	142	20	3	XX	
1288	143	21	3	XX	
1296	144	22	3	XX	
1304	145	23	3	XX	
1312	146	24	3	XX	
1320	147	25	3	XX	
1328	148	26	3	XX	
1336	149	27	3	XX	
1344	150	28	3	XX	
1352	151	29	3	XX	
1360	152	30	3	XX	
1368	153	31	3	na	postamp
1376	154	31	3	na	preamp
1384	155	32	3	na	postamp
1392	156	32	3	na	preamp
1400	157	33	3	na	postamp
1408	158	33	3	na	preamp
1416	159	34	3	na	postamp
1424	160	34	3	na	preamp
1432	161	35	3	na	postamp
1440	162	35	3	na	preamp
1448	163	36	3	na	postamp
1456	164	36	3	na	preamp
1464	165	1	13	XX	
1472	166	1	14	XX	
1480	167	1	15	XX	
1488	168	1	16	XX	
1496	169	2	13	XX	
1504	170	2	14	XX	

Reference Sort by Band/Det — 5/97

Pkt Start Bit	Memory Table Word Offset	Band	Det	PC Comments
3304	395	4	15	
3312	396	4	16	
3744	450	4	17	
3752	451	4	18	
4184	505	4	19	
4192	506	4	20	
240	12	5	1	
248	13	5	2	
680	67	5	3	
688	68	5	4	
1120	122	5	5	
1128	123	5	6	
1560	177	5	7	
1568	178	5	8	
2000	232	5	9	
2008	233	5	10	
2440	287	5	11	
2448	288	5	12	
2880	342	5	13	
2888	343	5	14	
3320	397	5	15	
3328	398	5	16	
3760	452	5	17	
3768	453	5	18	
4200	507	5	19	
4208	508	5	20	
256	14	6	1	
264	15	6	2	
696	69	6	3	
704	70	6	4	
1136	124	6	5	
1144	125	6	6	
1576	179	6	7	
1584	180	6	8	
2016	234	6	9	
2024	235	6	10	
2456	289	6	11	
2464	290	6	12	
2896	344	6	13	
2904	345	6	14	
3336	399	6	15	
3344	400	6	16	
3776	454	6	17	
3784	455	6	18	
4216	509	6	19	
4224	510	6	20	
272	16	7	1	
280	17	7	2	
712	71	7	3	
720	72	7	4	
1152	126	7	5	
1160	127	7	6	
1592	181	7	7	
1600	182	7	8	
2032	236	7	9	
2040	237	7	10	
2472	291	7	11	

TABLE 30-7. MODIS ENGINEERING GROUP 2 PACKET 2 DATA FIELD
PV GAIN DATA (4400 bits)

Sort by Pkt Start Bit — 550 words x 8 bits

Pkt Start Bit	Memory Table Word Offset	Band	Det	Gain Hex	PC Comments
1512	171	2	15	XX	
1520	172	2	16	XX	
1528	173	3	7	XX	
1536	174	3	8	XX	
1544	175	4	7	XX	
1552	176	4	8	XX	
1560	177	5	7	XX	
1568	178	5	8	XX	
1576	179	6	7	XX	
1584	180	6	8	XX	
1592	181	7	7	XX	
1600	182	7	8	XX	
1608	183	8	4	XX	
1616	184	9	4	XX	
1624	185	10	4	XX	
1632	186	11	4	XX	
1640	187	12	4	XX	
1648	188	13L	4	XX	
1656	189	13H	4	XX	
1664	190	14L	4	XX	
1672	191	14H	4	XX	
1680	192	15	4	XX	
1688	193	16	4	XX	
1696	194	17	4	XX	
1704	195	18	4	XX	
1712	196	19	4	XX	
1720	197	20	4	XX	
1728	198	21	4	XX	
1736	199	22	4	XX	
1744	200	23	4	XX	
1752	201	24	4	XX	
1760	202	25	4	XX	
1768	203	26	4	XX	
1776	204	27	4	XX	
1784	205	28	4	XX	
1792	206	29	4	XX	
1800	207	30	4	XX	
1808	208	31	4	na	postamp
1816	209	31	4	na	preamp
1824	210	32	4	na	postamp
1832	211	32	4	na	preamp
1840	212	33	4	na	postamp
1848	213	33	4	na	preamp
1856	214	34	4	na	postamp
1864	215	34	4	na	preamp
1872	216	35	4	na	postamp
1880	217	35	4	na	preamp
1888	218	36	4	na	postamp
1896	219	36	4	na	preamp
1904	220	1	17	XX	
1912	221	1	18	XX	
1920	222	1	19	XX	
1928	223	1	20	XX	
1936	224	2	17	XX	
1944	225	2	18	XX	
1952	226	2	19	XX	
1960	227	2	20	XX	

Reference Sort by Band/Det — 5/97

Pkt Start Bit	Memory Table Word Offset	Band	Det	PC Comments
2480	292	7	12	
2912	346	7	13	
2920	347	7	14	
3352	401	7	15	
3360	402	7	16	
3792	456	7	17	
3800	457	7	18	
4232	511	7	19	
4240	512	7	20	
288	18	8	1	
728	73	8	2	
1168	128	8	3	
1608	183	8	4	
2048	238	8	5	
2488	293	8	6	
2928	348	8	7	
3368	403	8	8	
3808	458	8	9	
4248	513	8	10	
296	19	9	1	
736	74	9	2	
1176	129	9	3	
1616	184	9	4	
2056	239	9	5	
2496	294	9	6	
2936	349	9	7	
3376	404	9	8	
3816	459	9	9	
4256	514	9	10	
304	20	10	1	
744	75	10	2	
1184	130	10	3	
1624	185	10	4	
2064	240	10	5	
2504	295	10	6	
2944	350	10	7	
3384	405	10	8	
3824	460	10	9	
4264	515	10	10	
312	21	11	1	
752	76	11	2	
1192	131	11	3	
1632	186	11	4	
2072	241	11	5	
2512	296	11	6	
2952	351	11	7	
3392	406	11	8	
3832	461	11	9	
4272	516	11	10	
320	22	12	1	
760	77	12	2	
1200	132	12	3	
1640	187	12	4	
2080	242	12	5	
2520	297	12	6	
2960	352	12	7	
3400	407	12	8	

TABLE 30-7. MODIS ENGINEERING GROUP 2 PACKET 2 DATA FIELD
PV GAIN DATA (4400 bits)

Sort by Pkt Start Bit — 550 words x 8 bits

Pkt Start Bit	Memory Table Word Offset	Band	Det	Gain Hex	PC Comments
1968	228	3	9	XX	
1976	229	3	10	XX	
1984	230	4	9	XX	
1992	231	4	10	XX	
2000	232	5	9	XX	
2008	233	5	10	XX	
2016	234	6	9	XX	
2024	235	6	10	XX	
2032	236	7	9	XX	
2040	237	7	10	XX	
2048	238	8	5	XX	
2056	239	9	5	XX	
2064	240	10	5	XX	
2072	241	11	5	XX	
2080	242	12	5	XX	
2088	243	13L	5	XX	
2096	244	13H	5	XX	
2104	245	14L	5	XX	
2112	246	14H	5	XX	
2120	247	15	5	XX	
2128	248	16	5	XX	
2136	249	17	5	XX	
2144	250	18	5	XX	
2152	251	19	5	XX	
2160	252	20	5	XX	
2168	253	21	5	XX	
2176	254	22	5	XX	
2184	255	23	5	XX	
2192	256	24	5	XX	
2200	257	25	5	XX	
2208	258	26	5	XX	
2216	259	27	5	XX	
2224	260	28	5	XX	
2232	261	29	5	XX	
2240	262	30	5	XX	
2248	263	31	5	na	postamp
2256	264	31	5	na	preamp
2264	265	32	5	na	postamp
2272	266	32	5	na	preamp
2280	267	33	5	na	postamp
2288	268	33	5	na	preamp
2296	269	34	5	na	postamp
2304	270	34	5	na	preamp
2312	271	35	5	na	postamp
2320	272	35	5	na	preamp
2328	273	36	5	na	postamp
2336	274	36	5	na	preamp
2344	275	1	21	XX	
2352	276	1	22	XX	
2360	277	1	23	XX	
2368	278	1	24	XX	
2376	279	2	21	XX	
2384	280	2	22	XX	
2392	281	2	23	XX	
2400	282	2	24	XX	
2408	283	3	11	XX	
2416	284	3	12	XX	

Reference Sort by Band/Det — 5/97

Pkt Start Bit	Memory Table Word Offset	Band	Det	PC Comments
3840	462	12	9	
4280	517	12	10	
360	27	15	1	
800	82	15	2	
1240	137	15	3	
1680	192	15	4	
2120	247	15	5	
2560	302	15	6	
3000	357	15	7	
3440	412	15	8	
3880	467	15	9	
4320	522	15	10	
368	28	16	1	
808	83	16	2	
1248	138	16	3	
1688	193	16	4	
2128	248	16	5	
2568	303	16	6	
3008	358	16	7	
3448	413	16	8	
3888	468	16	9	
4328	523	16	10	
376	29	17	1	
816	84	17	2	
1256	139	17	3	
1696	194	17	4	
2136	249	17	5	
2576	304	17	6	
3016	359	17	7	
3456	414	17	8	
3896	469	17	9	
4336	524	17	10	
384	30	18	1	
824	85	18	2	
1264	140	18	3	
1704	195	18	4	
2144	250	18	5	
2584	305	18	6	
3024	360	18	7	
3464	415	18	8	
3904	470	18	9	
4344	525	18	10	
392	31	19	1	
832	86	19	2	
1272	141	19	3	
1712	196	19	4	
2152	251	19	5	
2592	306	19	6	
3032	361	19	7	
3472	416	19	8	
3912	471	19	9	
4352	526	19	10	
400	32	20	1	
840	87	20	2	
1280	142	20	3	
1720	197	20	4	
2160	252	20	5	

TABLE 30-7. MODIS ENGINEERING GROUP 2 PACKET 2 DATA FIELD
PV GAIN DATA (4400 bits)

Sort by Pkt Start Bit — 550 words x 8 bits

Pkt Start Bit	Memory Table Word Offset	Band	Det	Gain Hex	PC Comments
2424	285	4	11	XX	
2432	286	4	12	XX	
2440	287	5	11	XX	
2448	288	5	12	XX	
2456	289	6	11	XX	
2464	290	6	12	XX	
2472	291	7	11	XX	
2480	292	7	12	XX	
2488	293	8	6	XX	
2496	294	9	6	XX	
2504	295	10	6	XX	
2512	296	11	6	XX	
2520	297	12	6	XX	
2528	298	13L	6	XX	
2536	299	13H	6	XX	
2544	300	14L	6	XX	
2552	301	14H	6	XX	
2560	302	15	6	XX	
2568	303	16	6	XX	
2576	304	17	6	XX	
2584	305	18	6	XX	
2592	306	19	6	XX	
2600	307	20	6	XX	
2608	308	21	6	XX	
2616	309	22	6	XX	
2624	310	23	6	XX	
2632	311	24	6	XX	
2640	312	25	6	XX	
2648	313	26	6	XX	
2656	314	27	6	XX	
2664	315	28	6	XX	
2672	316	29	6	XX	
2680	317	30	6	XX	
2688	318	31	6	na	postamp
2696	319	31	6	na	preamp
2704	320	32	6	na	postamp
2712	321	32	6	na	preamp
2720	322	33	6	na	postamp
2728	323	33	6	na	preamp
2736	324	34	6	na	postamp
2744	325	34	6	na	preamp
2752	326	35	6	na	postamp
2760	327	35	6	na	preamp
2768	328	36	6	na	postamp
2776	329	36	6	na	preamp
2784	330	1	25	XX	
2792	331	1	26	XX	
2800	332	1	27	XX	
2808	333	1	28	XX	
2816	334	2	25	XX	
2824	335	2	26	XX	
2832	336	2	27	XX	
2840	337	2	28	XX	
2848	338	3	13	XX	
2856	339	3	14	XX	
2864	340	4	13	XX	
2872	341	4	14	XX	

Reference Sort by Band/Det — 5/97

Pkt Start Bit	Memory Table Word Offset	Band	Det	PC Comments
2600	307	20	6	
3040	362	20	7	
3480	417	20	8	
3920	472	20	9	
4360	527	20	10	
408	33	21	1	
848	88	21	2	
1288	143	21	3	
1728	198	21	4	
2168	253	21	5	
2608	308	21	6	
3048	363	21	7	
3488	418	21	8	
3928	473	21	9	
4368	528	21	10	
416	34	22	1	
856	89	22	2	
1296	144	22	3	
1736	199	22	4	
2176	254	22	5	
2616	309	22	6	
3056	364	22	7	
3496	419	22	8	
3936	474	22	9	
4376	529	22	10	
424	35	23	1	
864	90	23	2	
1304	145	23	3	
1744	200	23	4	
2184	255	23	5	
2624	310	23	6	
3064	365	23	7	
3504	420	23	8	
3944	475	23	9	
4384	530	23	10	
432	36	24	1	
872	91	24	2	
1312	146	24	3	
1752	201	24	4	
2192	256	24	5	
2632	311	24	6	
3072	366	24	7	
3512	421	24	8	
3952	476	24	9	
4392	531	24	10	
440	37	25	1	
880	92	25	2	
1320	147	25	3	
1760	202	25	4	
2200	257	25	5	
2640	312	25	6	
3080	367	25	7	
3520	422	25	8	
3960	477	25	9	
4400	532	25	10	
448	38	26	1	
888	93	26	2	

TABLE 30-7. MODIS ENGINEERING GROUP 2 PACKET 2 DATA FIELD
PV GAIN DATA (4400 bits)

Sort by Pkt Start Bit — 550 words x 8 bits

Pkt Start Bit	Memory Table Word Offset	Band	Det	Gain Hex	PC Comments
2880	342	5	13	XX	
2888	343	5	14	XX	
2896	344	6	13	XX	
2904	345	6	14	XX	
2912	346	7	13	XX	
2920	347	7	14	XX	
2928	348	8	7	XX	
2936	349	9	7	XX	
2944	350	10	7	XX	
2952	351	11	7	XX	
2960	352	12	7	XX	
2968	353	13L	7	XX	
2976	354	13H	7	XX	
2984	355	14L	7	XX	
2992	356	14H	7	XX	
3000	357	15	7	XX	
3008	358	16	7	XX	
3016	359	17	7	XX	
3024	360	18	7	XX	
3032	361	19	7	XX	
3040	362	20	7	XX	
3048	363	21	7	XX	
3056	364	22	7	XX	
3064	365	23	7	XX	
3072	366	24	7	XX	
3080	367	25	7	XX	
3088	368	26	7	XX	
3096	369	27	7	XX	
3104	370	28	7	XX	
3112	371	29	7	XX	
3120	372	30	7	XX	
3128	373	31	7	na	postamp
3136	374	31	7	na	preamp
3144	375	32	7	na	postamp
3152	376	32	7	na	preamp
3160	377	33	7	na	postamp
3168	378	33	7	na	preamp
3176	379	34	7	na	postamp
3184	380	34	7	na	preamp
3192	381	35	7	na	postamp
3200	382	35	7	na	preamp
3208	383	36	7	na	postamp
3216	384	36	7	na	preamp
3224	385	1	29	XX	
3232	386	1	30	XX	
3240	387	1	31	XX	
3248	388	1	32	XX	
3256	389	2	29	XX	
3264	390	2	30	XX	
3272	391	2	31	XX	
3280	392	2	32	XX	
3288	393	3	15	XX	
3296	394	3	16	XX	
3304	395	4	15	XX	
3312	396	4	16	XX	
3320	397	5	15	XX	
3328	398	5	16	XX	

Reference Sort by Band/Det — 5/97

Pkt Start Bit	Memory Table Word Offset	Band	Det	PC Comments
1328	148	26	3	
1768	203	26	4	
2208	258	26	5	
2648	313	26	6	
3088	368	26	7	
3528	423	26	8	
3968	478	26	9	
4408	533	26	10	
456	39	27	1	
896	94	27	2	
1336	149	27	3	
1776	204	27	4	
2216	259	27	5	
2656	314	27	6	
3096	369	27	7	
3536	424	27	8	
3976	479	27	9	
4416	534	27	10	
464	40	28	1	
904	95	28	2	
1344	150	28	3	
1784	205	28	4	
2224	260	28	5	
2664	315	28	6	
3104	370	28	7	
3544	425	28	8	
3984	480	28	9	
4424	535	28	10	
472	41	29	1	
912	96	29	2	
1352	151	29	3	
1792	206	29	4	
2232	261	29	5	
2672	316	29	6	
3112	371	29	7	
3552	426	29	8	
3992	481	29	9	
4432	536	29	10	
480	42	30	1	
920	97	30	2	
1360	152	30	3	
1800	207	30	4	
2240	262	30	5	
2680	317	30	6	
3120	372	30	7	
3560	427	30	8	
4000	482	30	9	Gains are na
4440	537	30	10	to PC Bands
488	43	31	1	postamp
496	44	31	1	preamp
928	98	31	2	postamp
936	99	31	2	preamp
1368	153	31	3	postamp
1376	154	31	3	preamp
1808	208	31	4	postamp
1816	209	31	4	preamp
2248	263	31	5	postamp

TABLE 30-7. MODIS ENGINEERING GROUP 2 PACKET 2 DATA FIELD
PV GAIN DATA (4400 bits)

Sort by Pkt Start Bit — 550 words x 8 bits

Pkt Start Bit	Memory Table Word Offset	Band	Det	Gain Hex	PC Comments
3336	399	6	15	XX	
3344	400	6	16	XX	
3352	401	7	15	XX	
3360	402	7	16	XX	
3368	403	8	8	XX	
3376	404	9	8	XX	
3384	405	10	8	XX	
3392	406	11	8	XX	
3400	407	12	8	XX	
3408	408	13L	8	XX	
3416	409	13H	8	XX	
3424	410	14L	8	XX	
3432	411	14H	8	XX	
3440	412	15	8	XX	
3448	413	16	8	XX	
3456	414	17	8	XX	
3464	415	18	8	XX	
3472	416	19	8	XX	
3480	417	20	8	XX	
3488	418	21	8	XX	
3496	419	22	8	XX	
3504	420	23	8	XX	
3512	421	24	8	XX	
3520	422	25	8	XX	
3528	423	26	8	XX	
3536	424	27	8	XX	
3544	425	28	8	XX	
3552	426	29	8	XX	
3560	427	30	8	XX	
3568	428	31	8	na	postamp
3576	429	31	8	na	preamp
3584	430	32	8	na	postamp
3592	431	32	8	na	preamp
3600	432	33	8	na	postamp
3608	433	33	8	na	preamp
3616	434	34	8	na	postamp
3624	435	34	8	na	preamp
3632	436	35	8	na	postamp
3640	437	35	8	na	preamp
3648	438	36	8	na	postamp
3656	439	36	8	na	preamp
3664	440	1	33	XX	
3672	441	1	34	XX	
3680	442	1	35	XX	
3688	443	1	36	XX	
3696	444	2	33	XX	
3704	445	2	34	XX	
3712	446	2	35	XX	
3720	447	2	36	XX	
3728	448	3	17	XX	
3736	449	3	18	XX	
3744	450	4	17	XX	
3752	451	4	18	XX	
3760	452	5	17	XX	
3768	453	5	18	XX	
3776	454	6	17	XX	
3784	455	6	18	XX	

Reference Sort by Band/Det — 5/97

Pkt Start Bit	Memory Table Word Offset	Band	Det	PC Comments
2256	264	31	5	preamp
2688	318	31	6	postamp
2696	319	31	6	preamp
3128	373	31	7	postamp
3136	374	31	7	preamp
3568	428	31	8	postamp
3576	429	31	8	preamp
4008	483	31	9	postamp
4016	484	31	9	preamp
4448	538	31	10	postamp
4456	539	31	10	preamp
504	45	32	1	postamp
512	46	32	1	preamp
944	100	32	2	postamp
952	101	32	2	preamp
1384	155	32	3	postamp
1392	156	32	3	preamp
1824	210	32	4	postamp
1832	211	32	4	preamp
2264	265	32	5	postamp
2272	266	32	5	preamp
2704	320	32	6	postamp
2712	321	32	6	preamp
3144	375	32	7	postamp
3152	376	32	7	preamp
3584	430	32	8	postamp
3592	431	32	8	preamp
4024	485	32	9	postamp
4032	486	32	9	preamp
4464	540	32	10	postamp
4472	541	32	10	preamp
520	47	33	1	postamp
528	48	33	1	preamp
960	102	33	2	postamp
968	103	33	2	preamp
1400	157	33	3	postamp
1408	158	33	3	preamp
1840	212	33	4	postamp
1848	213	33	4	preamp
2280	267	33	5	postamp
2288	268	33	5	preamp
2720	322	33	6	postamp
2728	323	33	6	preamp
3160	377	33	7	postamp
3168	378	33	7	preamp
3600	432	33	8	postamp
3608	433	33	8	preamp
4040	487	33	9	postamp
4048	488	33	9	preamp
4480	542	33	10	postamp
4488	543	33	10	preamp
536	49	34	1	postamp
544	50	34	1	preamp
976	104	34	2	postamp
984	105	34	2	preamp
1416	159	34	3	postamp
1424	160	34	3	preamp

TABLE 30-7. MODIS ENGINEERING GROUP 2 PACKET 2 DATA FIELD
PV GAIN DATA (4400 bits)

Sort by Pkt Start Bit — 550 words x 8 bits

Pkt Start Bit	Memory Table Word Offset	Band	Det	Gain Hex	PC Comments
3792	456	7	17	XX	
3800	457	7	18	XX	
3808	458	8	9	XX	
3816	459	9	9	XX	
3824	460	10	9	XX	
3832	461	11	9	XX	
3840	462	12	9	XX	
3848	463	13L	9	XX	
3856	464	13H	9	XX	
3864	465	14L	9	XX	
3872	466	14H	9	XX	
3880	467	15	9	XX	
3888	468	16	9	XX	
3896	469	17	9	XX	
3904	470	18	9	XX	
3912	471	19	9	XX	
3920	472	20	9	XX	
3928	473	21	9	XX	
3936	474	22	9	XX	
3944	475	23	9	XX	
3952	476	24	9	XX	
3960	477	25	9	XX	
3968	478	26	9	XX	
3976	479	27	9	XX	
3984	480	28	9	XX	
3992	481	29	9	XX	
4000	482	30	9	XX	
4008	483	31	9	na	postamp
4016	484	31	9	na	preamp
4024	485	32	9	na	postamp
4032	486	32	9	na	preamp
4040	487	33	9	na	postamp
4048	488	33	9	na	preamp
4056	489	34	9	na	postamp
4064	490	34	9	na	preamp
4072	491	35	9	na	postamp
4080	492	35	9	na	preamp
4088	493	36	9	na	postamp
4096	494	36	9	na	preamp
4104	495	1	37	XX	
4112	496	1	38	XX	
4120	497	1	39	XX	
4128	498	1	40	XX	
4136	499	2	37	XX	
4144	500	2	38	XX	
4152	501	2	39	XX	
4160	502	2	40	XX	
4168	503	3	19	XX	
4176	504	3	20	XX	
4184	505	4	19	XX	
4192	506	4	20	XX	
4200	507	5	19	XX	
4208	508	5	20	XX	
4216	509	6	19	XX	
4224	510	6	20	XX	
4232	511	7	19	XX	
4240	512	7	20	XX	

Reference Sort by Band/Det — 5/97

Pkt Start Bit	Memory Table Word Offset	Band	Det	PC Comments
1856	214	34	4	postamp
1864	215	34	4	preamp
2296	269	34	5	postamp
2304	270	34	5	preamp
2736	324	34	6	postamp
2744	325	34	6	preamp
3176	379	34	7	postamp
3184	380	34	7	preamp
3616	434	34	8	postamp
3624	435	34	8	preamp
4056	489	34	9	postamp
4064	490	34	9	preamp
4496	544	34	10	postamp
4504	545	34	10	preamp
552	51	35	1	postamp
560	52	35	1	preamp
992	106	35	2	postamp
1000	107	35	2	preamp
1432	161	35	3	postamp
1440	162	35	3	preamp
1872	216	35	4	postamp
1880	217	35	4	preamp
2312	271	35	5	postamp
2320	272	35	5	preamp
2752	326	35	6	postamp
2760	327	35	6	preamp
3192	381	35	7	postamp
3200	382	35	7	preamp
3632	436	35	8	postamp
3640	437	35	8	preamp
4072	491	35	9	postamp
4080	492	35	9	preamp
4512	546	35	10	postamp
4520	547	35	10	preamp
568	53	36	1	postamp
576	54	36	1	preamp
1008	108	36	2	postamp
1016	109	36	2	preamp
1448	163	36	3	postamp
1456	164	36	3	preamp
1888	218	36	4	postamp
1896	219	36	4	preamp
2328	273	36	5	postamp
2336	274	36	5	preamp
2768	328	36	6	postamp
2776	329	36	6	preamp
3208	383	36	7	postamp
3216	384	36	7	preamp
3648	438	36	8	postamp
3656	439	36	8	preamp
4088	493	36	9	postamp
4096	494	36	9	preamp
4528	548	36	10	postamp
4536	549	36	10	preamp
336	24	13H	1	
776	79	13H	2	
1216	134	13H	3	

TABLE 30-7. MODIS ENGINEERING GROUP 2 PACKET 2 DATA FIELD

PV GAIN DATA (4400 bits)

Sort by Pkt Start Bit — 550 words x 8 bits

Pkt Start Bit	Memory Table Word Offset	Band	Det	Gain Hex	PC Comments
4248	513	8	10	XX	
4256	514	9	10	XX	
4264	515	10	10	XX	
4272	516	11	10	XX	
4280	517	12	10	XX	
4288	518	13L	10	XX	
4296	519	13H	10	XX	
4304	520	14L	10	XX	
4312	521	14H	10	XX	
4320	522	15	10	XX	
4328	523	16	10	XX	
4336	524	17	10	XX	
4344	525	18	10	XX	
4352	526	19	10	XX	
4360	527	20	10	XX	
4368	528	21	10	XX	
4376	529	22	10	XX	
4384	530	23	10	XX	
4392	531	24	10	XX	
4400	532	25	10	XX	
4408	533	26	10	XX	
4416	534	27	10	XX	
4424	535	28	10	XX	
4432	536	29	10	XX	
4440	537	30	10	XX	
4448	538	31	10	na	postamp
4456	539	31	10	na	preamp
4464	540	32	10	na	postamp
4472	541	32	10	na	preamp
4480	542	33	10	na	postamp
4488	543	33	10	na	preamp
4496	544	34	10	na	postamp
4504	545	34	10	na	preamp
4512	546	35	10	na	postamp
4520	547	35	10	na	preamp
4528	548	36	10	na	postamp
4536	549	36	10	na	preamp

• Pkt end bit = 4543. Subtract 144 to obtain local field bit.

Reference Sort by Band/Det — 5/97

Pkt Start Bit	Memory Table Word Offset	Band	Det	PC Comments
1656	189	13H	4	
2096	244	13H	5	
2536	299	13H	6	
2976	354	13H	7	
3416	409	13H	8	
3856	464	13H	9	
4296	519	13H	10	
328	23	13L	1	
768	78	13L	2	
1208	133	13L	3	
1648	188	13L	4	
2088	243	13L	5	
2528	298	13L	6	
2968	353	13L	7	
3408	408	13L	8	
3848	463	13L	9	
4288	518	13L	10	
352	26	14H	1	
792	81	14H	2	
1232	136	14H	3	
1672	191	14H	4	
2112	246	14H	5	
2552	301	14H	6	
2992	356	14H	7	
3432	411	14H	8	
3872	466	14H	9	
4312	521	14H	10	
344	25	14L	1	
784	80	14L	2	
1224	135	14L	3	
1664	190	14L	4	
2104	245	14L	5	
2544	300	14L	6	
2984	355	14L	7	
3424	410	14L	8	
3864	465	14L	9	
4304	520	14L	10	

Notes:

1. This table contains 550words x 8 bits = 4400 bits total, and includes Gain values for all PV detectors (1km IFOV's, including 13Hi/13Lo and 14Hi/14Lo, and multiple detectors related to the 250m and 500m IFOV's). This table is not applicable to PC Gains (bands 30-36), but it has a parallel structure to Table 30-4 FPA DCR Offsets.

2. In Memory Table 10-24, the locations for Memory Table 4 PV Gains, are shown in Column 2 as Word-Offsets from zero location for use in 1553 Bus upload or download (16 bit memory words).

T30-7 Change History

1. 9/17/96 New table. PV gains in this table parallels structure of T30-4 for PV DCR offsets.
2. 4/97 EO1122D incorporation for Rev B to emphasize Gain data does not apply to PC Bands.

TABLE 30-7. MODIS ENGINEERING GROUP 2 PACKET 2 DATA FIELD
PV GAIN DATA (4400 bits)

Sort by Pkt Start Bit — 550 words x 8 bits

Pkt Start Bit	Memory Table Word Offset	Band	Det	Gain Hex	PC Comments

Reference Sort by Band/Det — 5/97

Pkt Start Bit	Memory Table Word Offset	Band	Det	PC Comments

SHEET 11 IS INTENTIONALLY BLANK

TABLE 30-8A. MODIS TEST DAY GROUP PACKET 1 DATA FIELD

Test Day Packet 1 contains Test IFOV 1-5 data (4980 bits).

IFOV 1 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value
144	1	1	1	1
156	1	2	1	2
168	1	3	1	3
180	1	4	1	4
192	1	1	2	5
204	1	2	2	6
216	1	3	2	7
228	1	4	2	8
240	1	1	3	9
252	1	2	3	10
264	1	3	3	11
276	1	4	3	12
288	1	1	4	13
300	1	2	4	14
312	1	3	4	15
324	1	4	4	16
336	2	1	1	17
348	2	2	1	18
360	2	3	1	19
372	2	4	1	20
384	2	1	2	21
396	2	2	2	22
408	2	3	2	23
420	2	4	2	24
432	2	1	3	25
444	2	2	3	26
456	2	3	3	27
468	2	4	3	28
480	2	1	4	29
492	2	2	4	30
504	2	3	4	31
516	2	4	4	32
528	3	1	1	33
540	3	2	1	34
552	3	1	2	35
564	3	2	2	36
576	4	1	1	37
588	4	2	1	38
600	4	1	2	39
612	4	2	2	40
624	5	1	1	41
636	5	2	1	42
648	5	1	2	43
660	5	2	2	44
672	6	1	1	45

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IFOV 2 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value
1140	1	5	1	84
1152	1	6	1	85
1164	1	7	1	86
1176	1	8	1	87
1188	1	5	2	88
1200	1	6	2	89
1212	1	7	2	90
1224	1	8	2	91
1236	1	5	3	92
1248	1	6	3	93
1260	1	7	3	94
1272	1	8	3	95
1284	1	5	4	96
1296	1	6	4	97
1308	1	7	4	98
1320	1	8	4	99
1332	2	5	1	100
1344	2	6	1	101
1356	2	7	1	102
1368	2	8	1	103
1380	2	5	2	104
1392	2	6	2	105
1404	2	7	2	106
1416	2	8	2	107
1428	2	5	3	108
1440	2	6	3	109
1452	2	7	3	110
1464	2	8	3	111
1476	2	5	4	112
1488	2	6	4	113
1500	2	7	4	114
1512	2	8	4	115
1524	3	3	1	116
1536	3	4	1	117
1548	3	3	2	118
1560	3	4	2	119
1572	4	3	1	120
1584	4	4	1	121
1596	4	3	2	122
1608	4	4	2	123
1620	5	3	1	124
1632	5	4	1	125
1644	5	3	2	126
1656	5	4	2	127
1668	6	3	1	128

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IFOV 3 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value
2136	1	9	1	167
2148	1	10	1	168
2160	1	11	1	169
2172	1	12	1	170
2184	1	9	2	171
2196	1	10	2	172
2208	1	11	2	173
2220	1	12	2	174
2232	1	9	3	175
2244	1	10	3	176
2256	1	11	3	177
2268	1	12	3	178
2280	1	9	4	179
2292	1	10	4	180
2304	1	11	4	181
2316	1	12	4	182
2328	2	9	1	183
2340	2	10	1	184
2352	2	11	1	185
2364	2	12	1	186
2376	2	9	2	187
2388	2	10	2	188
2400	2	11	2	189
2412	2	12	2	190
2424	2	9	3	191
2436	2	10	3	192
2448	2	11	3	193
2460	2	12	3	194
2472	2	9	4	195
2484	2	10	4	196
2496	2	11	4	197
2508	2	12	4	198
2520	3	5	1	199
2532	3	6	1	200
2544	3	5	2	201
2556	3	6	2	202
2568	4	5	1	203
2580	4	6	1	204
2592	4	5	2	205
2604	4	6	2	206
2616	5	5	1	207
2628	5	6	1	208
2640	5	5	2	209
2652	5	6	2	210
2664	6	5	1	211

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IFOV 4 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value
3132	1	13	1	250
3144	1	14	1	251
3156	1	15	1	252
3168	1	16	1	253
3180	1	13	2	254
3192	1	14	2	255
3204	1	15	2	256
3216	1	16	2	257
3228	1	13	3	258
3240	1	14	3	259
3252	1	15	3	260
3264	1	16	3	261
3276	1	13	4	262
3288	1	14	4	263
3300	1	15	4	264
3312	1	16	4	265
3324	2	13	1	266
3336	2	14	1	267
3348	2	15	1	268
3360	2	16	1	269
3372	2	13	2	270
3384	2	14	2	271
3396	2	15	2	272
3408	2	16	2	273
3420	2	13	3	274
3432	2	14	3	275
3444	2	15	3	276
3456	2	16	3	277
3468	2	13	4	278
3480	2	14	4	279
3492	2	15	4	280
3504	2	16	4	281
3516	3	7	1	282
3528	3	8	1	283
3540	3	7	2	284
3552	3	8	2	285
3564	4	7	1	286
3576	4	8	1	287
3588	4	7	2	288
3600	4	8	2	289
3612	5	7	1	290
3624	5	8	1	291
3636	5	7	2	292
3648	5	8	2	293
3660	6	7	1	294

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IFOV 5 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value
4128	1	17	1	333
4140	1	18	1	334
4152	1	19	1	335
4164	1	20	1	336
4176	1	17	2	337
4188	1	18	2	338
4200	1	19	2	339
4212	1	20	2	340
4224	1	17	3	341
4236	1	18	3	342
4248	1	19	3	343
4260	1	20	3	344
4272	1	17	4	345
4284	1	18	4	346
4296	1	19	4	347
4308	1	20	4	348
4320	2	17	1	349
4332	2	18	1	350
4344	2	19	1	351
4356	2	20	1	352
4368	2	17	2	353
4380	2	18	2	354
4392	2	19	2	355
4404	2	20	2	356
4416	2	17	3	357
4428	2	18	3	358
4440	2	19	3	359
4452	2	20	3	360
4464	2	17	4	361
4476	2	18	4	362
4488	2	19	4	363
4500	2	20	4	364
4512	3	9	1	365
4524	3	10	1	366
4536	3	9	2	367
4548	3	10	2	368
4560	4	9	1	369
4572	4	10	1	370
4584	4	9	2	371
4596	4	10	2	372
4608	5	9	1	373
4620	5	10	1	374
4632	5	9	2	375
4644	5	10	2	376
4656	6	9	1	377

TABLE 30-8A. MODIS TEST DAY GROUP PACKET 1 DATA FIELD

415Wx12B

Test Day Packet 1 contains Test IFOV 1-5 data (4980 bits).

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IFOV 1 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value
684	6	2	1	46
696	6	1	2	47
708	6	2	2	48
720	7	1	1	49
732	7	2	1	50
744	7	1	2	51
756	7	2	2	52
768	8	1	1	53
780	9	1	1	54
792	10	1	1	55
804	11	1	1	56
816	12	1	1	57
828	13L	1	1	58
840	13H	1	1	59
852	14L	1	1	60
864	14H	1	1	61
876	15	1	1	62
888	16	1	1	63
900	17	1	1	64
912	18	1	1	65
924	19	1	1	66
936	20	1	1	67
948	21	1	1	68
960	22	1	1	69
972	23	1	1	70
984	24	1	1	71
996	25	1	1	72
1008	26	1	1	73
1020	27	1	1	74
1032	28	1	1	75
1044	29	1	1	76
1056	30	1	1	77
1068	31	1	1	78
1080	32	1	1	79
1092	33	1	1	80
1104	34	1	1	81
1116	35	1	1	82
1128	36	1	1	83

• 1st column is packet start bit for entry

IFOV 2 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value
1680	6	4	1	129
1692	6	3	2	130
1704	6	4	2	131
1716	7	3	1	132
1728	7	4	1	133
1740	7	3	2	134
1752	7	4	2	135
1764	8	2	1	136
1776	9	2	1	137
1788	10	2	1	138
1800	11	2	1	139
1812	12	2	1	140
1824	13L	2	1	141
1836	13H	2	1	142
1848	14L	2	1	143
1860	14H	2	1	144
1872	15	2	1	145
1884	16	2	1	146
1896	17	2	1	147
1908	18	2	1	148
1920	19	2	1	149
1932	20	2	1	150
1944	21	2	1	151
1956	22	2	1	152
1968	23	2	1	153
1980	24	2	1	154
1992	25	2	1	155
2004	26	2	1	156
2016	27	2	1	157
2028	28	2	1	158
2040	29	2	1	159
2052	30	2	1	160
2064	31	2	1	161
2076	32	2	1	162
2088	33	2	1	163
2100	34	2	1	164
2112	35	2	1	165
2124	36	2	1	166

• All items have 12 bits

IFOV 3 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value
2676	6	6	1	212
2688	6	5	2	213
2700	6	6	2	214
2712	7	5	1	215
2724	7	6	1	216
2736	7	5	2	217
2748	7	6	2	218
2760	8	3	1	219
2772	9	3	1	220
2784	10	3	1	221
2796	11	3	1	222
2808	12	3	1	223
2820	13L	3	1	224
2832	13H	3	1	225
2844	14L	3	1	226
2856	14H	3	1	227
2868	15	3	1	228
2880	16	3	1	229
2892	17	3	1	230
2904	18	3	1	231
2916	19	3	1	232
2928	20	3	1	233
2940	21	3	1	234
2952	22	3	1	235
2964	23	3	1	236
2976	24	3	1	237
2988	25	3	1	238
3000	26	3	1	239
3012	27	3	1	240
3024	28	3	1	241
3036	29	3	1	242
3048	30	3	1	243
3060	31	3	1	244
3072	32	3	1	245
3084	33	3	1	246
3096	34	3	1	247
3108	35	3	1	248
3120	36	3	1	249

• Total Field = 4980 bits

IFOV 4 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value
3672	6	8	1	295
3684	6	7	2	296
3696	6	8	2	297
3708	7	7	1	298
3720	7	8	1	299
3732	7	7	2	300
3744	7	8	2	301
3756	8	4	1	302
3768	9	4	1	303
3780	10	4	1	304
3792	11	4	1	305
3804	12	4	1	306
3816	13L	4	1	307
3828	13H	4	1	308
3840	14L	4	1	309
3852	14H	4	1	310
3864	15	4	1	311
3876	16	4	1	312
3888	17	4	1	313
3900	18	4	1	314
3912	19	4	1	315
3924	20	4	1	316
3936	21	4	1	317
3948	22	4	1	318
3960	23	4	1	319
3972	24	4	1	320
3984	25	4	1	321
3996	26	4	1	322
4008	27	4	1	323
4020	28	4	1	324
4032	29	4	1	325
4044	30	4	1	326
4056	31	4	1	327
4068	32	4	1	328
4080	33	4	1	329
4092	34	4	1	330
4104	35	4	1	331
4116	36	4	1	332

• Last Field bit in Pkt-> 5123

IFOV 5 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value
4668	6	10	1	378
4680	6	9	2	379
4692	6	10	2	380
4704	7	9	1	381
4716	7	10	1	382
4728	7	9	2	383
4740	7	10	2	384
4752	8	5	1	385
4764	9	5	1	386
4776	10	5	1	387
4788	11	5	1	388
4800	12	5	1	389
4812	13L	5	1	390
4824	13H	5	1	391
4836	14L	5	1	392
4848	14H	5	1	393
4860	15	5	1	394
4872	16	5	1	395
4884	17	5	1	396
4896	18	5	1	397
4908	19	5	1	398
4920	20	5	1	399
4932	21	5	1	400
4944	22	5	1	401
4956	23	5	1	402
4968	24	5	1	403
4980	25	5	1	404
4992	26	5	1	405
5004	27	5	1	406
5016	28	5	1	407
5028	29	5	1	408
5040	30	5	1	409
5052	31	5	1	410
5064	32	5	1	411
5076	33	5	1	412
5088	34	5	1	413
5100	35	5	1	414
5112	36	5	1	415

TABLE 30-8A. MODIS TEST DAY GROUP PACKET 1 DATA FIELD

Test Day Packet 1 contains Test IFOV 1-5 data (4980 bits).

IFOV 1 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value

IFOV 2 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value

IFOV 3 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value

IFOV 4 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value

IFOV 5 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value

T30-1. Change History

1. 9/17/96 Change title to Group vs Segment terminology.

TABLE 30-8B. MODIS TEST DAY GROUP PACKET 2 DATA FIELD

Test Day Packet 2 contains Test IFOV 6-10 data (4980 bits).

IFOV 6 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value
144	1	21	1	1
156	1	22	1	2
168	1	23	1	3
180	1	24	1	4
192	1	21	2	5
204	1	22	2	6
216	1	23	2	7
228	1	24	2	8
240	1	21	3	9
252	1	22	3	10
264	1	24	3	11
276	1	23	3	12
288	1	21	4	13
300	1	22	4	14
312	1	23	4	15
324	1	24	4	16
336	2	21	1	17
348	2	22	1	18
360	2	23	1	19
372	2	24	1	20
384	2	21	2	21
396	2	22	2	22
408	2	23	2	23
420	2	24	2	24
432	2	21	3	25
444	2	22	3	26
456	2	24	3	27
468	2	23	3	28
480	2	21	4	29
492	2	22	4	30
504	2	23	4	31
516	2	24	4	32
528	3	11	1	33
540	3	12	1	34
552	3	11	2	35
564	3	12	2	36
576	4	11	1	37
588	4	12	1	38
600	4	11	2	39
612	4	12	2	40
624	5	11	1	41
636	5	12	1	42
648	5	11	2	43
660	5	12	2	44
672	6	11	1	45

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IFOV 7 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value
1140	1	25	1	84
1152	1	26	1	85
1164	1	27	1	86
1176	1	28	1	87
1188	1	25	2	88
1200	1	26	2	89
1212	1	27	2	90
1224	1	28	2	91
1236	1	25	3	92
1248	1	26	3	93
1260	1	27	3	94
1272	1	28	3	95
1284	1	25	4	96
1296	1	26	4	97
1308	1	27	4	98
1320	1	28	4	99
1332	2	25	1	100
1344	2	26	1	101
1356	2	27	1	102
1368	2	28	1	103
1380	2	25	2	104
1392	2	26	2	105
1404	2	27	2	106
1416	2	28	2	107
1428	2	25	3	108
1440	2	26	3	109
1452	2	27	3	110
1464	2	28	3	111
1476	2	25	4	112
1488	2	26	4	113
1500	2	27	4	114
1512	2	28	4	115
1524	3	13	1	116
1536	3	14	1	117
1548	3	13	2	118
1560	3	14	2	119
1572	4	13	1	120
1584	4	14	1	121
1596	4	13	2	122
1608	4	14	2	123
1620	5	13	1	124
1632	5	14	1	125
1644	5	13	2	126
1656	5	14	2	127
1668	6	13	1	128

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IFOV 8 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value
2136	1	29	1	167
2148	1	30	1	168
2160	1	31	1	169
2172	1	32	1	170
2184	1	29	2	171
2196	1	30	2	172
2208	1	31	2	173
2220	1	32	2	174
2232	1	29	3	175
2244	1	30	3	176
2256	1	31	3	177
2268	1	32	3	178
2280	1	29	4	179
2292	1	30	4	180
2304	1	31	4	181
2316	1	32	4	182
2328	2	29	1	183
2340	2	30	1	184
2352	2	31	1	185
2364	2	32	1	186
2376	2	29	2	187
2388	2	30	2	188
2400	2	31	2	189
2412	2	32	2	190
2424	2	29	3	191
2436	2	30	3	192
2448	2	31	3	193
2460	2	32	3	194
2472	2	29	4	195
2484	2	30	4	196
2496	2	31	4	197
2508	2	32	4	198
2520	3	15	1	199
2532	3	16	1	200
2544	3	15	2	201
2556	3	16	2	202
2568	4	15	1	203
2580	4	16	1	204
2592	4	15	2	205
2604	4	16	2	206
2616	5	15	1	207
2628	5	16	1	208
2640	5	15	2	209
2652	5	16	2	210
2664	6	15	1	211

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IFOV 9 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value
3132	1	33	1	250
3144	1	34	1	251
3156	1	35	1	252
3168	1	36	1	253
3180	1	33	2	254
3192	1	34	2	255
3204	1	35	2	256
3216	1	36	2	257
3228	1	33	3	258
3240	1	34	3	259
3252	1	35	3	260
3264	1	36	3	261
3276	1	33	4	262
3288	1	34	4	263
3300	1	35	4	264
3312	1	36	4	265
3324	2	33	1	266
3336	2	34	1	267
3348	2	35	1	268
3360	2	36	1	269
3372	2	33	2	270
3384	2	34	2	271
3396	2	35	2	272
3408	2	36	2	273
3420	2	33	3	274
3432	2	34	3	275
3444	2	35	3	276
3456	2	36	3	277
3468	2	33	4	278
3480	2	34	4	279
3492	2	35	4	280
3504	2	36	4	281
3516	3	7	1	282
3528	3	8	1	283
3540	3	7	2	284
3552	3	8	2	285
3564	4	17	1	286
3576	4	18	1	287
3588	4	17	2	288
3600	4	18	2	289
3612	5	17	1	290
3624	5	18	1	291
3636	5	17	2	292
3648	5	18	2	293
3660	6	17	1	294

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IFOV 10 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value
4128	1	37	1	333
4140	1	38	1	334
4152	1	39	1	335
4164	1	40	1	336
4176	1	37	2	337
4188	1	38	2	338
4200	1	39	2	339
4212	1	40	2	340
4224	1	37	3	341
4236	1	38	3	342
4248	1	39	3	343
4260	1	40	3	344
4272	1	37	4	345
4284	1	38	4	346
4296	1	39	4	347
4308	1	40	4	348
4320	2	37	1	349
4332	2	38	1	350
4344	2	39	1	351
4356	2	40	1	352
4368	2	37	2	353
4380	2	38	2	354
4392	2	39	2	355
4404	2	40	2	356
4416	2	37	3	357
4428	2	38	3	358
4440	2	39	3	359
4452	2	40	3	360
4464	2	37	4	361
4476	2	38	4	362
4488	2	39	4	363
4500	2	40	4	364
4512	3	19	1	365
4524	3	20	1	366
4536	3	19	2	367
4548	3	20	2	368
4560	4	19	1	369
4572	4	20	1	370
4584	4	19	2	371
4596	4	20	2	372
4608	5	19	1	373
4620	5	20	1	374
4632	5	19	2	375
4644	5	20	2	376
4656	6	19	1	377

TABLE 30-8B. MODIS TEST DAY GROUP PACKET 2 DATA FIELD

Test Day Packet 2 contains Test IFOV 6-10 data (4960 bits).

IFOV 6 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value
684	6	12	1	46
696	6	11	2	47
708	6	12	2	48
720	7	11	1	49
732	7	12	1	50
744	7	11	2	51
756	7	12	2	52
768	8	6	1	53
780	9	6	1	54
792	10	6	1	55
804	11	6	1	56
816	12	6	1	57
828	13L	6	1	58
840	13H	6	1	59
852	14L	6	1	60
864	14H	6	1	61
876	15	6	1	62
888	16	6	1	63
900	17	6	1	64
912	18	6	1	65
924	19	6	1	66
936	20	6	1	67
948	21	6	1	68
960	22	6	1	69
972	23	6	1	70
984	24	6	1	71
996	25	6	1	72
1008	26	6	1	73
1020	27	6	1	74
1032	28	6	1	75
1044	29	6	1	76
1056	30	6	1	77
1068	31	6	1	78
1080	32	6	1	79
1092	33	6	1	80
1104	34	6	1	81
1116	35	6	1	82
1128	36	6	1	83

• 1st column is packet start bit for entry

IFOV 7 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value
1680	6	14	1	129
1692	6	13	2	130
1704	6	14	2	131
1716	7	13	1	132
1728	7	14	1	133
1740	7	13	2	134
1752	7	14	2	135
1764	8	7	1	136
1776	9	7	1	137
1788	10	7	1	138
1800	11	7	1	139
1812	12	7	1	140
1824	13L	7	1	141
1836	13H	7	1	142
1848	14L	7	1	143
1860	14H	7	1	144
1872	15	7	1	145
1884	16	7	1	146
1896	17	7	1	147
1908	18	7	1	148
1920	19	7	1	149
1932	20	7	1	150
1944	21	7	1	151
1956	22	7	1	152
1968	23	7	1	153
1980	24	7	1	154
1992	25	7	1	155
2004	26	7	1	156
2016	27	7	1	157
2028	28	7	1	158
2040	29	7	1	159
2052	30	7	1	160
2064	31	7	1	161
2076	32	7	1	162
2088	33	7	1	163
2100	34	7	1	164
2112	35	7	1	165
2124	36	7	1	166

• All items have 12 bits

IFOV 8 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value
2676	6	16	1	212
2688	6	15	2	213
2700	6	16	2	214
2712	7	15	1	215
2724	7	16	1	216
2736	7	15	2	217
2748	7	16	2	218
2760	8	8	1	219
2772	9	8	1	220
2784	10	8	1	221
2796	11	8	1	222
2808	12	8	1	223
2820	13L	8	1	224
2832	13H	8	1	225
2844	14L	8	1	226
2856	14H	8	1	227
2868	15	8	1	228
2880	16	8	1	229
2892	17	8	1	230
2904	18	8	1	231
2916	19	8	1	232
2928	20	8	1	233
2940	21	8	1	234
2952	22	8	1	235
2964	23	8	1	236
2976	24	8	1	237
2988	25	8	1	238
3000	26	8	1	239
3012	27	8	1	240
3024	28	8	1	241
3036	29	8	1	242
3048	30	8	1	243
3060	31	8	1	244
3072	32	8	1	245
3084	33	8	1	246
3096	34	8	1	247
3108	35	8	1	248
3120	36	8	1	249

• Total Field = 4980 bits

IFOV 9 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value
3672	6	18	1	295
3684	6	17	2	296
3696	6	18	2	297
3708	7	17	1	298
3720	7	18	1	299
3732	7	17	2	300
3744	7	18	2	301
3756	8	9	1	302
3768	9	9	1	303
3780	10	9	1	304
3792	11	9	1	305
3804	12	9	1	306
3816	13L	9	1	307
3828	13H	9	1	308
3840	14L	9	1	309
3852	14H	9	1	310
3864	15	9	1	311
3876	16	9	1	312
3888	17	9	1	313
3900	18	9	1	314
3912	19	9	1	315
3924	20	9	1	316
3936	21	9	1	317
3948	22	9	1	318
3960	23	9	1	319
3972	24	9	1	320
3984	25	9	1	321
3996	26	9	1	322
4008	27	9	1	323
4020	28	9	1	324
4032	29	9	1	325
4044	30	9	1	326
4056	31	9	1	327
4068	32	9	1	328
4080	33	9	1	329
4092	34	9	1	330
4104	35	9	1	331
4116	36	9	1	332

IFOV 10 (1km) 5/97

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value
4668	6	20	1	378
4680	6	19	2	379
4692	6	20	2	380
4704	7	19	1	381
4716	7	20	1	382
4728	7	19	2	383
4740	7	20	2	384
4752	8	10	1	385
4764	9	10	1	386
4776	10	10	1	387
4788	11	10	1	388
4800	12	10	1	389
4812	13L	10	1	390
4824	13H	10	1	391
4836	14L	10	1	392
4848	14H	10	1	393
4860	15	10	1	394
4872	16	10	1	395
4884	17	10	1	396
4896	18	10	1	397
4908	19	10	1	398
4920	20	10	1	399
4932	21	10	1	400
4944	22	10	1	401
4956	23	10	1	402
4968	24	10	1	403
4980	25	10	1	404
4992	26	10	1	405
5004	27	10	1	406
5016	28	10	1	407
5028	29	10	1	408
5040	30	10	1	409
5052	31	10	1	410
5064	32	10	1	411
5076	33	10	1	412
5088	34	10	1	413
5100	35	10	1	414
5112	36	10	1	415

• Last Field bit in Pkt-> 5123

TABLE 30-8B. MODIS TEST DAY GROUP PACKET 2 DATA FIELD

415Wx12B

Test Day Packet 2 contains Test IFOV 6-10 data (4980 bits).

5/97

IFOV 6 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value

IFOV 7 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value

IFOV 8 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value

IFOV 9 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value

IFOV 10 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value

T30-8B. Change History

1. 9/1/96 New table.

TABLE 30-8C. MODIS TEST NIGHT GROUP PACKET DATA FIELD

171Wx12B=2052 bits

NIGHT VALUES ARE SAME AS IN TEST DAY PACKET FOR SAME BAND/DETECTOR

5/97

IFOV#1 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value
144	20	1	1	67
156	21	1	1	68
168	22	1	1	69
180	23	1	1	70
192	24	1	1	71
204	25	1	1	72
216	26	1	1	73
228	27	1	1	74
240	28	1	1	75
252	29	1	1	76
264	30	1	1	77
276	31	1	1	78
288	32	1	1	79
300	33	1	1	80
312	34	1	1	81
324	35	1	1	82
336	36	1	1	83

IFOV#2 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value
348	20	2	1	150
360	21	2	1	151
372	22	2	1	152
384	23	2	1	153
396	24	2	1	154
408	25	2	1	155
420	26	2	1	156
432	27	2	1	157
444	28	2	1	158
456	29	2	1	159
468	30	2	1	160
480	31	2	1	161
492	32	2	1	162
504	33	2	1	163
516	34	2	1	164
528	35	2	1	165
540	36	2	1	166

IFOV#3 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value
552	20	3	1	233
564	21	3	1	234
576	22	3	1	235
588	23	3	1	236
600	24	3	1	237
612	25	3	1	238
624	26	3	1	239
636	27	3	1	240
648	28	3	1	241
660	29	3	1	242
672	30	3	1	243
684	31	3	1	244
696	32	3	1	245
708	33	3	1	246
720	34	3	1	247
732	35	3	1	248
744	36	3	1	249

IFOV#4 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value
756	20	4	1	316
768	21	4	1	317
780	22	4	1	318
792	23	4	1	319
804	24	4	1	320
816	25	4	1	321
828	26	4	1	322
840	27	4	1	323
852	28	4	1	324
864	29	4	1	325
876	30	4	1	326
888	31	4	1	327
900	32	4	1	328
912	33	4	1	329
924	34	4	1	330
936	35	4	1	331
948	36	4	1	332

IFOV#5 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value
960	20	5	1	399
972	21	5	1	400
984	22	5	1	401
996	23	5	1	402
1008	24	5	1	403
1020	25	5	1	404
1032	26	5	1	405
1044	27	5	1	406
1056	28	5	1	407
1068	29	5	1	408
1080	30	5	1	409
1092	31	5	1	410
1104	32	5	1	411
1116	33	5	1	412
1128	34	5	1	413
1140	35	5	1	414
1152	36	5	1	415

IFOV#6 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value
1164	20	6	1	67
1176	21	6	1	68
1188	22	6	1	69
1200	23	6	1	70
1212	24	6	1	71
1224	25	6	1	72
1236	26	6	1	73
1248	27	6	1	74
1260	28	6	1	75
1272	29	6	1	76
1284	30	6	1	77
1296	31	6	1	78
1308	32	6	1	79
1320	33	6	1	80
1332	34	6	1	81
1344	35	6	1	82
1356	36	6	1	83

IFOV#7 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value
1368	20	7	1	150
1380	21	7	1	151
1392	22	7	1	152
1404	23	7	1	153
1416	24	7	1	154
1428	25	7	1	155
1440	26	7	1	156
1452	27	7	1	157
1464	28	7	1	158
1476	29	7	1	159
1488	30	7	1	160
1500	31	7	1	161
1512	32	7	1	162
1524	33	7	1	163
1536	34	7	1	164
1548	35	7	1	165
1560	36	7	1	166

IFOV#8 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value
1572	20	8	1	233
1584	21	8	1	234
1596	22	8	1	235
1608	23	8	1	236
1620	24	8	1	237
1632	25	8	1	238
1644	26	8	1	239
1656	27	8	1	240
1668	28	8	1	241
1680	29	8	1	242
1692	30	8	1	243
1704	31	8	1	244
1716	32	8	1	245
1728	33	8	1	246
1740	34	8	1	247
1752	35	8	1	248
1764	36	8	1	249

IFOV#9 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value
1776	20	9	1	316
1788	21	9	1	317
1800	22	9	1	318
1812	23	9	1	319
1824	24	9	1	320
1836	25	9	1	321
1848	26	9	1	322
1860	27	9	1	323
1872	28	9	1	324
1884	29	9	1	325
1896	30	9	1	326
1908	31	9	1	327
1920	32	9	1	328
1932	33	9	1	329
1944	34	9	1	330
1956	35	9	1	331
1968	36	9	1	332

IFOV#10 (1km)

Pkt Start Bit	Ref Band	Ref Det	Ref Sample	Decimal Value
1980	20	10	1	399
1992	21	10	1	400
2004	22	10	1	401
2016	23	10	1	402
2028	24	10	1	403
2040	25	10	1	404
2052	26	10	1	405
2064	27	10	1	406
2076	28	10	1	407
2088	29	10	1	408
2100	30	10	1	409
2112	31	10	1	410
2124	32	10	1	411
2136	33	10	1	412
2148	34	10	1	413
2160	35	10	1	414
2172	36	10	1	415

• 1st column is packet start bit for entry

• All items have 12 bits

• Total Field = 2052 bits with 12 fill bits

• 2195 <--Last Field bit in Pkt with added 12 fill bits

T30-3 Change History

1. 9/17/96 Change title to Group vs Segment terminology.
2. 4/97 EO1122D incorporation to Rev B corrected table number.

APPENDIX D. MODIS COMMAND AND TELEMETRY RELATIONS

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40.1 SCOPE

Appendix D primarily relates MODIS command and telemetry responses. It also presents summary information on redundancies/dependencies, control processor startup/reset defaults, control and format processor event codes.

40.2 MODIS OPERATIONAL GROUPS

Figure 40-1 partitions the various MODIS subsystems into four operational groups. It illustrates the relationship of the subsystems to produce the function of each group. The upper block of each subsystem contains its name and a brief command and telemetry number count in the form of #C and #T. The lower block contains a summary of the types of commands associated with that subsystem.

Note, as the name implies, the Telemetry Only Group contains subsystems that only have telemetry.

The MODIS two-character subsystem abbreviations defined in Figure 11 and Table 10 are used in this Appendix.

40.3 SUBSYSTEM REDUNDANCIES & DEPENDENCIES

Table 40-1 provides a summary of MODIS subsystem redundancies and dependencies.

Most MODIS subsystems are fully redundant. However, some subsystems have functional redundancy or limited redundancy. These are listed in Table 40-1.

It is intended to operate MODIS in a Side_A or Side_B configuration unless forced to a cross-strap configuration. However, there are 3 subsystems that have side dependencies. These are listed in Table 40-1.

40.4 COMMAND & TELEMETRY RESPONSE

Table 40-2 contains all the MODIS commands listed in Table 10-25A, and the related direct telemetry responses listed in Table 20-2A to each individual command. Explicit direct bilevel telemetry responses only exist for configuration type of commands. Indirect telemetry responses are also indicated. Many commands are related to setting values or flags in the CCSDS packet headers of the high rate science link data. These responses are only available in the Science and Engineering packets. There are other science related commands whose response only shows up as a change in the FPA detector Science data.

Also, Reset type of commands are transient in nature, and are too fast for the MODIS telemetry system. But there will be indirect indications, such as, a temporary interruption of normal telemetry data, or the subsequent logging of an event by the CP or FR single board computers.

The CP does not perform normal 1553 command and telemetry processes during major memory upload or download activity. Processing ability only exists to accomplish the upload/download, RAM transfer and restart functions needed to complete the major overall task.

Multiple telemetry responses exist for a significant number of commands because of the inherent nature of the MODIS subsystem command structure. That is, most subsystems have an A__On/B_Off, B_On/A_Off or both A/B_Off control. This results in at least two telemetry responses when turning one side On. There are a handful of spacecraft BDU direct point-point telemetry, which also have similar 1553 bus telemetry points. This results in four explicit telemetry responses to a single command.

There are three MODIS subsystems that can have both sides On at the same time, although this is not a normal configuration setup. They are the Power Supplies (PS), the FAM (PC) and the Scan Mirror Assembly (SA). It will be noted that in Table 10-25A Command List, each of these have both an A/B_On command as well as the standard A_On/B_Off, B_On/A_Off commands.

A small number of commands that set particular PV FPA biases, have a 1553 HK telemetry value and also show up in engineering packets. There are also a small number of non-command telemetry points that are in the engineering packets.

40.5 CP POWER ON AND RESET DEFAULTS

Table 40-3 provides a summary of Control Processor defaults that occur when first powering up MODIS, or, when a commanded Reset or a powered CPA/CPB (not recommended) is made.

40.6 CP LOG EVENT CODES (Reference)

Table 40-4 provides a summary of Control Processor log event codes for telemetry word SS_CP_LAST_EVENT. Telemetry word SS_CP_LOG_EVENT is a 1-bit word that indicates an event has occurred. Telemetry word SS_CP_LAST_EVENT is a 16-bit word expressed in 4 Hex values, which indicates the nature of the event. The 2-digit MSB's are simply a sequence count that rolls over. The 2-digit LSB's are the specific event message code ID. This table is for reference information. For latest updates see 152932 Maintenance Manual of the MODIS Flight Software System.

40.7 FR LOG EVENT CODES (Reference)

Table 40-5 provides a summary of Format Processor log event codes for telemetry word SS_FR_LAST_EVENT. Telemetry word SS_FR_LOG_EVENT is a 1-bit word that indicates an event has occurred. Telemetry word SS_FR_LAST_EVENT is a 16-bit word expressed in 4 Hex values, which indicates the nature of the event. The 2-digit MSB's are simply a sequence count that rolls over. The 2-digit LSB's are the specific event message code ID. This table is for reference information. For latest updates see 152932 Maintenance Manual of the MODIS Flight Software System.

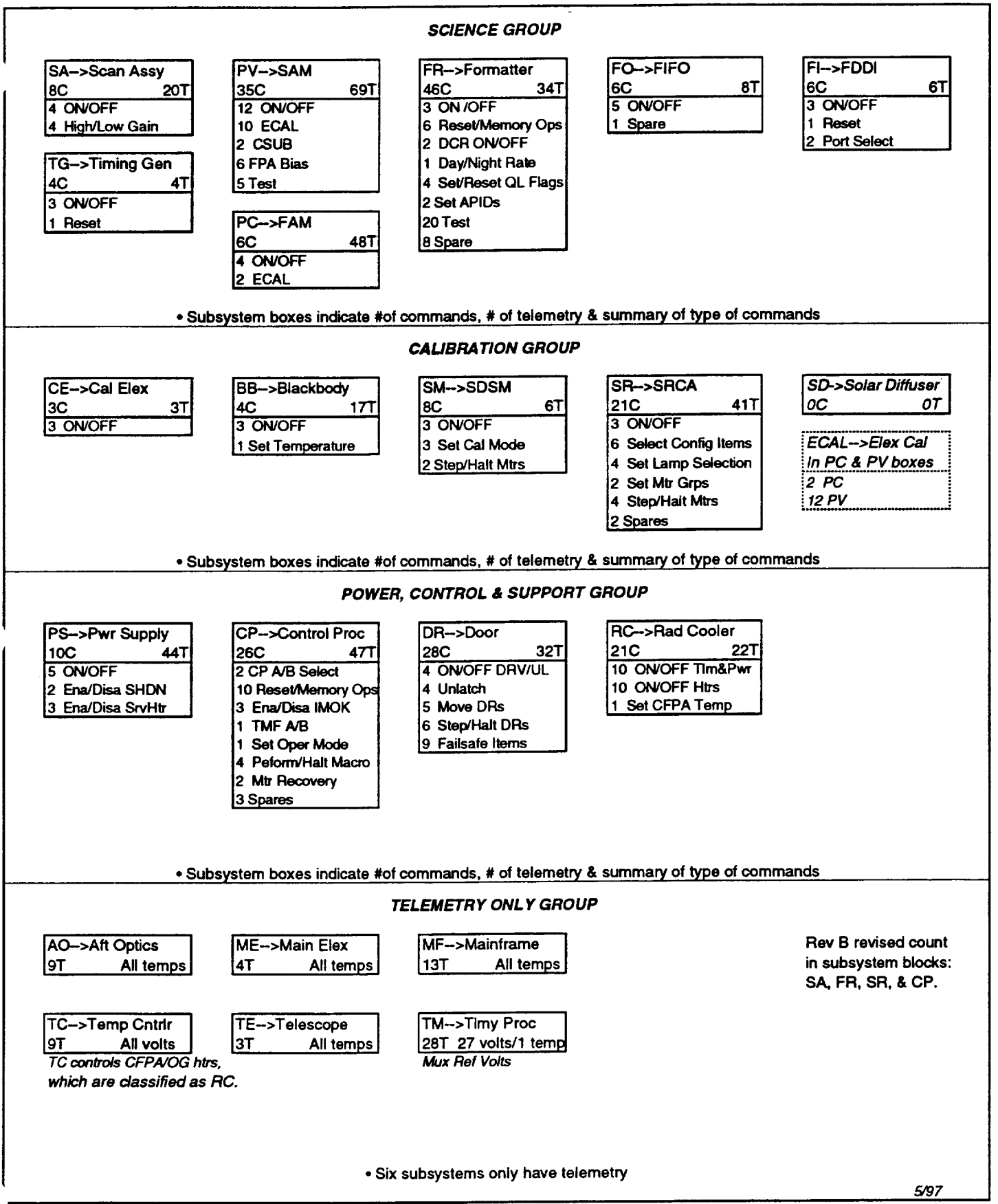

Figure 40-1. MODIS Related Operational Subsystem Groups

TABLE 40-1. MODIS SUBSYSTEM REDUNDANCIES & DEPENDENCIES

See Notes

5/97

21 Subsys	Function	Full Redundancy	Functional Redundancy	Limited Redundancy	Side Dependancy	Telemetry Only	Remarks
BB	A/B_Power & Control	√					Single BB with redundant heaters
BB	Passive Temperatures		√				12 separate BB temperatures
CE	A/B_Power & Control	√					Single CAL 2 CCA temperature
CP	A/B_Power & Control	√					1 temperature/ea
DR	Unlatch Functions	√					Redundant heaters in single mechanism
DR	Motor Drive			√			SDD has redundant motor windings; NAD & SVD single windings
DR	Failsafe Functions			√			NAD & SVD have single mechanism with redundant FS heaters; SDD single FS heater
FI	A/B_Power & Control	√					
FO	A/B_Power & Control	√					Any 2 of 4 FIFO blocks needed
FR	A/B_Power & Control	√					1 temperature/ea
PC	A/B_Power & Control	√					PC also has dual A/B ops capability for shorted load isolation
PC	Active & Passive Temperatures		√				6 active & 1 passive FAM temperatures (passive is radiator)
PC	CLAM (FAM Preamp)					√	No redundancy; 1 passive temperature
PS	A/B_Power & Control	√					4 temperature sensors/ea
PV	LWIR A/B_Power & Control	√			√		1 temperature/ea; LWIR CSUB dependent on CPA/PVA or CPB/PVB
PV	NIR A/B_Power & Control	√					2 temperatures/ea
PV	SMIR A/B_Power & Control	√			√		2 temperatures/ea; SMIR CSUB dependent on CPA/PVA or CPB/PVB
PV	VIS A/B_Power & Control	√					1 temperature/ea
PV	Radiator Temperature					√	No redundancy
RC	LWIR/SMIR CFPA Htr & Tlmy		√				LWIR/SMIR Heater control & temperature telemetry/ea with backup by the other
RC	CS/IS/OS Outgas Htr & Tlmy			√			Cold/Intermediate/Outer OG Heater control & temperature telemetry/ea with limited backup by each other
SA	A/B_Power & Control	√					SA also has dual A/B ops capability; I motor temperature and 2 mirror radiatively coupled temperatures
SM	A/B_Power & Control	√					Single pointing mirror with redundant motor driver and windings.
SR	A/B_Power & Control	√			√		Single wheel, slit and grating mechanisms with redundant motor drivers and windings. 11 temperature sensors, 4 of which form 2 redundant sets.
TG	A/B_Power & Control	√					
TELEMETRY ONLY							
AO	Active & Passive Temperatures		√			√	9 separate AO temperature points; some adjacent points provide backup relative temperature
ME	Passive Temperatures			√		√	3 MEM temperature points (1 is radiator); functionality allocated to subsystems
MF	Passive Temperatures		√			√	13 MF temperture points
TC	Voltage circuits for OG Htr & Tlmy			√		√	Plus voltage circuit/ea for CS, IS & OS OG heaters & telemetry cited in RC subsystem
TC	Voltage circuits CFPA Htr & Tlmy			√		√	Plus/minus voltage circuit/ea for LWIR & SMIR CFPA heaters & telemetry cited in RC subsystem
TC	Voltage circuits VIS/NIR FPA Tlmy			√		√	Plus/minus voltage circuit/ea for VIS & NIR telemetry cited in AO subsystem.
TE	Passive Temperatures			√		√	3 separate temperature points. Any two could provide related backup for the third.
TM	Active & Passive Telemetry	√				√	1 temperature/ea; 14/ea passive & 13/ea active telemetry reference points

TABLE 40-1. MODIS SUBSYSTEM REDUNDANCIES & DEPENDENCIES

See Notes

5/97

21 Subsys Function	Full Redundancy	Functional Redundancy	Limited Redundancy	Side Dependancy	Telemetry Only	Remarks

Notes:

1. This table summarizes the MODIS subsystem redundancies and dependencies. This is difficult to do in brief matrix form because some subsystems are fully redundant, while other subsystems have several unique functions which are not fully redundant, but may range from functionally redundant, to limited redundancy, to no redundancy. No temperarture points are literally redundant. However, subsystems with multi-temperature points will have historical relativity for all points.

2. The table also identifies 2 subsystems that have side A/B dependencies (PV LWIR, PV SMIR, and SR). Dependent upon viewpoint, these might also have been classified as constaints in 10.9. They were not classified as constraints because the initial intent is to operate all Side_A or all Side_B.

3. Subsystems that do not have any commandable choices, i.e. only contain telemetry functions, are listed in the bottom part of the table.

4. Recall the Section 7 box note, explains that the 2-character subsystem designations are based on an enduser functional interest, which may differ from how commands are routed to HW elements. For example, commands to control the Radiative Cooler (RC) are really routed to the Temperature Controller (TC), but are identified with an RC tag from a functional interest. Similarly, the FPAs are tagged as PC or PV instead of FAM and SAM, because of the PC and PV detector technology interest.

Table 40-1 Change History [#s] are general items.

[1] 12/7/96 This table is new with Rev A.

TABLE 40-2. MODIS COMMAND & TELEMETRY RESPONSE

Sort by Subsystem — *A/B redundant subsystems have general A_On/B_Off command structure, except PC, PS & SA can have both sides on at same time.* — *5/97*

pf chgs	1 Subsys	2 OASIS Command Name	3 Qualifier or Value	4 Cmd Type	5 Primary Verification	6 Continuing/Indirect Verification	7 Additional Data	8 Remarks	9 Tlmy Type
8	BB01	TURN_ON_BBA		R	CR_BB_A_PWR_ON =1	CR_BB_B_PWR_ON =0		Both s/b true	D
8	BB02	TURN_ON_BBB		R	CR_BB_B_PWR_ON =1	CR_BB_A_PWR_ON =0		Both s/b true	D
	BB03	TURN_OFF_BB		R	CR_BB_A_PWR_ON =0	CR_BB_B_PWR_ON =0		Both s/b true	D
18,23	BB04	SET_BB_HTR_TEMP	TO D#XXXX	SW	all TP_BB_TEMP01 -12	About 2hr for total chg	If heated T s/b = new pt	Delayed response	SW
8,18	CE01	TURN_ON_CEA		R	CR_CE_A_ON =1	CR_CE_B_ON =0		Both s/b true	D
8,18	CE02	TURN_ON_CEB		R	CR_CE_B_ON =1	CR_CE_A_ON =0		Both s/b true	D
	CE03	TURN_OFF_CE		R	CR_CE_A_ON =0	CR_CE_B_ON =0		Both s/b true	D
9	CP01	TURN ON_CPA		RS	CR_CP_A_ON_S =0	CR_CP_B_ON_S =1	CR_CP_A_ON_M=1, CR_CP_B_ON_M=0	All s/b true	D,DS
9	CP02	TURN ON_CPB		RS	CR_CP_B_ON_S =0	CR_CP_A_ON_S =1	CR_CP_A_ON_M=0, CR_CP_B_ON_M=1	All s/b true	D,DS
	CP03	RESET_CP_STD		RS	SS_CP_RESET_SRC =010			s/b true after reset recovery	SW
	CP04	ENABLE_CP_IMOK		SW	SS_CP_IMOK_ON =1			As noted	SW
	CP05	DISABLE_CP_IMOK		SW	SS_CP_IMOK_ON =0			As noted	SW
9	CP06	SET_CP_TMF_BUS	TO A/B	SWD	CR_CP_SET_TMF_A =0/B=1			As noted	D
	CP07	SET_CP_OPER_MODE	TO SRV/SAF/STBY/OG/SCI	SW	SS_CP_MODE =001 SRV,	010 SAFE, 011 STDBY,	100 OG, 101 SCI	Match selected mode	SW
18,27	CP08	PERFORM_CP_MACRO	WITH NUMBER X	SW	Only indirect macro events			No direct indiation	SW
27	CP09	SET_CP_MACRDELAY	WITH SCANS X	SW	Only indirect macro events			No direct indiation	SW
27	CP10	CLOSE_CP_MACRO		SW	Only indirect macro events			No direct indiation	SW
27	CP11	HALT_CP_MACRO	WITH NUMBER X	SW	Only indirect macro events			No direct indiation	SW
18	CP12	DUMP_MEM	(Select 8 items, see Op Code T10-21)	SW	Memory selection per T10-21 appears in HK			HK tlmy	SW
	CP13	RESET_CP_UPLD		RS	SS_CP_RESET_SRC =011			s/b true after reset recovery	SW
18	CP14	LOAD_CP_RAM	(Select 10 items, see Op Code T10-17)	SW	Dump memory to verify			Memory should match upload	SW
17	CP15	SET_CP_RESTART	WITH ASTATE X#X	SW	Resumption of tlmy			No tlmy until after restart	SW
26	CP16	ENABLE_CPA_EPWRT		RS	CR_CPA_EEP_WRE_S =1	CR_CPA_EEP_WRE_M =0		Both s/b true	D,DS
26	CP17	ENABLE_CPB_EPWRT		RS	CR_CPB_EEP_WRE_S =1	CR_CPB_EEP_WRE_M =0		Both s/b true	D,DS
16	CP18	CP_SPARE		SW	na			na	SW
	CP19	HALT_CP_RAM_XFER		SW	Event will be issued			Recover event	SW
	CP20	DISABLE_CP_EPWRT		RD	CR_CPA_EEP_WRE_M =0	CR_CPB_EEP_WRE_M =0	CR_CPA_EEP_WRE_S =0, CR_CPB_EEP_WRE_S =0	All s/b true	D,DS
27	CP22	SET_CP_SAFE_MODE		SW	SS_CP_MODE =010			As noted	SW
	CP23	CP_SC_SPARE	***S/C SPARE***	RS	na				RS
10	CP24	GET_CP_MTR_HOME	WITH MTR D#X, DIR B#X	SW	CR_DR_SVD,NAD,SDD _CLSD =1, CR_SM_MIR_HOME_A =0, CR_SM_MIR_HOME_B =0	CR_SR_WHL_HOMEA =0, CR_SR_WHL_HOMEB =0, CR_SR_SLIT_HOMEA =0, CR_SR_SLIT_HOMEB =0	CR_SR_GRAT_CH_A =0, CR_SR_GRAT_FH_A =0, CR_SR_GRAT_CH_B =0, CR_SR_GRAT_FH_B =0,	Match mtr tlmy to cmded mtr, Grating has coarse & fine	D, DCE
10	CP25	SET_CP_MTR_SWPOS	WITH MTR D#X, STEP X#XXXX	SW	SS_DR_NAD_STEP, SS_DR_SDD_STEP, SS_DR_SVD_STEP	CS_SM_MIR_STEP, CS_SR_GRAT_STEP,	CS_SR_GRAT_STEP, CS_SR_GRAT_STEP	Selected mtr tlmy should update	SW
10	CP26	SET_CP_LOG_STATE	TO D#XX (0 TO 15)	SW	SS_CP_LOG_STATE			Match cmded value	SW
	DR01	TURN_ON_DR_ULA		R	CR_DR_UNLACH_AON =1	CR_DR_UNLACH_BON =0	CR_DR_DRV_ON =0	All s/b true	D
	DR02	TURN_ON_DR_ULB		R	CR_DR_UNLACH_BON =1	CR_DR_UNLACH_AON =0	CR_DR_DRV_ON =0	All s/b true	D

TABLE 40-2. MODIS COMMAND & TELEMETRY RESPONSE

Sort by Subsystem — *A/B redundant subsystems have general A_On/B_Off command structure, except PC, PS & SA can have both sides on at same time.* — *5/97*

pf chgs	1 Subsys	2 OASIS Command Name	3 Qualifier or Value	4 Cmd Type	5 Primary Verification	6 Continuing/Indirect Verification	7 Additional Data	8 Remarks	9 Tlmy Type
18	DR03	OPEN_DR_UL_LOCK		SW	Slight PS current increase if DR04, 05 or 06 enter DR03 10 sec window			As noted	SW
18	DR04	SET_DR_SVD_UL_ON		SWD	CR_DRSVD_1LATCHD =0	CR_DRSVD_2LATCHD =0		Both true after about 5 min	DS
18	DR05	SET_DR_NAD_UL_ON		SWD	CR_DRNAD_1LATCHD =0	CR_DRNAD_2LATCHD =0		Both true after about 5 min	DS
18	DR06	SET_DR_SDD_UL_ON		SWD	CR_DRSDD_LATCHD =0			True after about 5 min	DS
	DR07	TURN_OFF_DR_PWR		R	CR_DR_DRV_ON =0	CR_DR_UNLACH_AON =0	CR_DR_UNLACH_BON =0	All s/b true	D
	DR08	TURN_ON_DR_DRV		R	CR_DR_DRV_ON =1	CR_DR_UNLACH_AON =0	CR_DR_UNLACH_BON =0	All s/b true	D
18	DR09	MOVE_DR_SVD	TO CLOSED/OG/OPEN	SW	CR_DR_SVD_CLSD =1/0	CS_DR_SVD_AT_OG =1/0	CR_DR_SVD_OPEN =1/0	Match cmd: OG by SW; Clsd/Open by limit switches	D,SW
18	DR10	M OVE_DR_NAD	TO CLOSED/OPEN	SW	CR_DR_NAD_CLSD =1/0	CR_DR_NAD_OPEN =1/0		Match cmd: Clsd/Open by limit switches	D
	DR11	SET_DR_SDD_DRVA		R	CR_DR_SDD_DRV_A =1			As noted	D
	DR12	SET_DR_SDD_DRVB		R	CR_DR_SDD_DRV_A =0			As noted	D
6,18	DR13	MOVE_DR_SDD	TO CLOSED/SCREEN CLOSED/OPEN	SW	CR_DR_SDD_CLSD =1/0, CR_DR_SDD_OPEN =1/0, CR_DR_SDS_OPEN =1/0	Both SDD/SDS Closed CLSD=1 with OPEN = 0,0	SDD Open/SDS Closed CLSD=0 with OPEN=1, 0	Both SDD/SDS Open CLSD=0 with OPEN = 1,1	D
18	DR14	STEP_DR_SVD	BY D#XXXX IN/OUT	SW	SS_DR_SVD_STEP	(tlmy in absolute step count)		Delta steps match cmd	SW
18	DR15	STEP_DR_NAD	BY D#XXXX IN/OUT	SW	SS_DR_NAD_STEP	(tlmy in absolute step count)		Delta steps match cmd	SW
18	DR16	STEP_DR_SDD	BY D#XXXX IN/OUT	SW	SS_DR_SDD_STEP	(tlmy in absolute step count)		Delta steps match cmd	SW
	DR17	HALT_DR_STEP_SVD		SW	SS_DR_SVD_STEP, CR_DR_SVD_CLSD	CS_DR_SVD_AT_OG, CR_DR_SVD_OPEN	<-any may stop short for DR09 or DR14	As noted	SW
	DR18	HALT_DR_STEP_NAD		SW	SS_DR_NAD_STEP, CR_DR_NAD_CLSD	CR_DR_NAD_OPEN	<-any may stop short for DR10 or DR15	As noted	SW
	DR19	HALT_DR_STEP_SDD		SW	SS_DR_SDD_STEP, CR_DR_SDD_CLSD, CR_DR_SDS_CLSD	CR_DR_SDD_OPEN, CR_DR_SDS_OPEN	<-any may stop short for DR11 or DR19	As noted	SW
	DR20	SELECT_DR_PRI_FS		R	CR_DR_PRI_FS_SEL =1		FS rtn path for NAD & SVD	As noted	D
18	DR21	SELECT_DR_RDT_FS		R	CR_DR_PRI_FS_SEL =0		FS rtn path for NAD & SVD	As noted	D
18,22,26	DR22	ENABLE_DR_FS		R/S	CR_DR_FS_ENABL_S =0	CR_DR_FS_ENABL_M =1	+30V becomes available	Both s/b true	D,DS
18	DR23	CLOSE_DR_FS_SW2		R	CR_DR_FS_SW_CLSD =1		2nd step of FS sequence	As noted	D
18	DR24	FIRE_DR_SVD_FS		R	CR_DR_SVD_FS_ON =1	CR_DR_SVD_OPEN	3rd & final SVD FS Step	As noted, 5 min for Open	D
18	DR25	FIRE_DR_NAD_FS		R	CR_DR_NAD_FS_ON =1	CR_DR_NAD_OPEN	3rd & final NAD FS Step	As noted, 5 min for Open	D
18	DR26	TURN_ON_DR_SDDFS		R	CR_DR_SDFS_DRVON =1		3rd of 4 SDD FS steps	As noted	D
18,21	DR27	SET_DR_SDD_FS	TO ON/OFF	SWD	CR_DR_SDD_CLSD =0, CR_DR_SDD_OPEN =1	CR_DR_SDS_OPEN =0	4th & final SDD FS step	All true after about 5 min	D
	DR28	OPEN_DR_FS_SWS		R	CR_DR_FS_SW_CLSD =0	CR_DR_FS_ENABL_S =0	CR_DR_FS_ENABL_M =0	All s/b true	D,DS
	FI01	TURN_ON_FIA		R	CR_FI_A_ON =1	CR_FI_B_ON =0		Both s/b true	D
	FI02	TURN_ON_FIB		R	CR_FI_B_ON =1	CR_FI_A_ON =0		Both s/b true	D
	FI03	TURN_OFF_FI		R	CR_FI_A_ON =0	CR_FI_B_ON =0		Both s/b true	D
18	FI04	RESET_FI		SWD	CR_FI_A_RESET =0	CR_FI_B_RESET=0	1=RUNNING	Active side s/b true	D
18,26	FI05	SELECT_FI_PORTA		R	CR_FI_PORT_A_ON =1	CR_FI_PORT_B_ON =0		Active side s/b true	D
18,26	FI06	SELECT_FI_PORTB		R	CR_FI_PORT_B_ON =1	CR_FI_PORT_A_ON =0		Active side s/b true	D
18	FO01	TURN_ON_FO_BLK1		R	CR_FO_BLK1_ON =1		2 of 4 needed	As noted	D
18	FO02	TURN_ON_FO_BLK2		R	CR_FO_BLK2_ON =1		2 of 4 needed	As noted	D
18	FO03	TURN_ON_FO_BLK3		R	CR_FO_BLK3_ON =1		2 of 4 needed	As noted	D
18	FO04	TURN_ON_FO_BLK4		R	CR_FO_BLK4_ON =1		2 of 4 needed	As noted	D
18	FO05	TURN_OFF_FO		R	CR_FO_BLK1_ON =0	<--Also, BLK2,3,4 =0		Active blocks to Off	D

TABLE 40-2. MODIS COMMAND & TELEMETRY RESPONSE

Sort by Subsystem *A/B redundant subsystems have general A_On/B_Off command structure, except PC, PS & SA can have both sides on at same time.* *5/97*

pf chgs	1 Subsys	2 OASIS Command Name	3 Qualifier or Value	4 Cmd Type	5 Primary Verification	6 Continuing/Indirect Verification	7 Additional Data	8 Remarks	9 Tlmy Type
4	FO06	FO_SPARE		SWD	na			na	D
	FR01	TURN_ON_FRA		R	CR_FR_A_ON =1	CR_FR_B_ON =0		All s/b true	D
	FR02	TURN_ON_FRB		R	CR_FR_B_ON =1	CR_FR_A_ON =0		All s/b true	D
	FR03	TURN_OFF_FR		R	CR_FR_A_ON =0	CR_FR_B_ON =0		All s/b true	D
15	FR04	TOGGLE_FR_INT02		SWD	Indirect tlmy by an event			Recover event	SW
	FR05	RESET_FR_STD		SWD	CR_FR_A_RESET =0	CR_FR_B_RESET =0	1=RUNNING	Active side s/b true	SW
	FR06	FR_SPARE	na	na	na			na	na
13	FR07	SET_FR_RATE	TO DAY/NIGHT	SW	CS_FR_DAY_RATE = 1/0			State follows cmd	SW
14	FR08	SET_FR _SCI_APID	TO D#XXX	SW	All pkt headers & Eng pkt			In pkts	SW
14	FR09	SET_FR_SCI_QLK		SW	All pkt headers & Eng pkt			In pkts	SW
14	FR10	RESET_FR_SCI_QLK		SW	All pkt headers & Eng pkt			In pkts	SW
14	FR11	SET_FR_ENG_APID	TO D#XXX	SW	All pkt headers & Eng pkt			In pkts	SW
14	FR12	SET_FR_ENG_QLK		SW	All pkt headers & Eng pkt			In pkts	SW
14	FR13	RESET_FR_ENG_QLK		SW	All pkt headers & Eng pkt			In pkts	SW
14	FR14	FR_SPARE		SW	Was deleted mem pkt item			na	SW
20	FR15	SET_FR_RESTART	WITH ASTATE X#X	SW	Resumption of tlmy			No tlmy until after restart	SW
14,25	FR16	SET_FR_SCIABNORM	TO ABNORM/NORM	SW	SS_FR_SCIABNORM= ABNORM=0/NORM=1			Match cmd value	SW
3	FR17	SET_FR_SD_DELAY	TO D#XX	SW	CS_FR_DELAY_SD			Match cmd value	SW
3	FR18	SET_FR_SR_DELAY	TO D#XX	SW	CS_FR_DELAY_SR			Match cmd value	SW
3	FR19	SET_FR_BB_DELAY	TO D#XX	SW	CS_FR_DELAY_BB			Match cmd value	SW
3	FR20	SET_FR_SP_DELAY	TO D#XX	SW	CS_FR_DELAY_SP			Match cmd value	SW
3	FR21	SET_FR_EA_DELAY	TO D#XX	SW	CS_FR_DELAY_EA			Match cmd value	SW
	FR22	RESET_FR_UPLD		SWD	SS_FR_RESET_SRC =011			As noted after reset recovery	SW
	FR23	ENABLE_FRA_EPWRT		R	CR_FRA_EEP_WRE =1			s/b true	D
	FR24	ENABLE_FRB_EPWRT		R	CR_FRB_EEP_WRE =1			s/b true	D
16	FR25	FR_SPARE		SW	na			na	SW
18,19	FR26	SET_FR_PKT_TYPE	TO NORMAL/TEST	SW	SS_FR_PKT_TYPE	Normal/Test = o/1	TEST also results in Test Pkt	Match cmd value	SW
18	FR27	SET_FR_PC_DCRCMP	TO ON/OFF	SW	CS_FR_PC_DCR_ON =1	0=false		Match cmd value	SW
2	FR28	FR_SPARE	na	SW	na				SW
18	FR29	SET_FR_PV_DCRCMP	TO ON/OFF	SW	CS_FR_PV_DCR_ON =1	0=false		Match cmd value	SW
2	FR30	FR_SPARE	na	SW	na				SW
10,21	FR31	SET_FR_ENC_DELTA	TO 0, -8192,+8191	SW	CS_FR_ENC_DELTA			Match cmd value	SW
10	FR32	SET_FR_BBRADTAB	TO NORMAL/TEST	SW	CS_FR_BBRADTAB =1/0			Match cmd value	SW
10	FR33	SET_FR_OFFSETTAB	TO NORMAL/TEST	SW	CS_FR_OFFSETTAB = 1/0			Match cmd value	SW
10	FR34	SET_FR_GAINTAB	TO NORMAL/TEST	SW	CS_FR_GAINTAB = 1/0			Match cmd value	SW
10,24	FR35	TEST_FR_BBRAD	WITH OS X#XXX	SW	Effect in Sci Pkt			Sci Pkt	SW
10,24	FR36	TEST_FR_PVOFFSET	WITH OS X#XX	SW	Effect in Sci Pkt			Sci Pkt	SW
10,24	FR37	TEST_FR_PCOFFSET	WITH OS X#XXXX	SW	Effect in Sci Pkt			Sci Pkt	SW
10,24	FR38	TEST_FR_PVGAIN	WITH GN X#XX	SW	Effect in Sci Pkt			Sci Pkt	SW
10	FR39	SET_FR_PVGN1C	WITH B D#XX, C D#XX, V X#XX	SW	Effect in Sci Pkt			Sci Pkt	SW
10	FR40	SET_FR_PVOS1C	WITH B D#XX, C D#XX, V X#XX	SW	Effect in Sci Pkt			Sci Pkt	SW

TABLE 40-2. MODIS COMMAND & TELEMETRY RESPONSE

Sort by Subsystem — *A/B redundant subsystems have general A_On/B_Off command structure, except PC, PS & SA can have both sides on at same time.* — *5/97*

pf chgs	1 Subsys	2 OASIS Command Name	3 Qualifier or Value	4 Cmd Type	5 Primary Verification	6 Continuing/Indirect Verification	7 Additional Data	8 Remarks	9 Tlmy Type
10	FR41	SET_FR_PCPREOS1C	WITH B D#XX, C D#XX, V X#XX	SW	Effect in Sci Pkt			Sci Pkt	SW
10	FR42	SET_FR_PCPSTOS1C	WITH B D#XX, C D#XX, V X#XX	SW	Effect in Sci Pkt			Sci Pkt	SW
10	FR46	SET_FR_LOG_STATE	TO D#XX (0 TO 15)	SW	SS_FR_LOG_STATE			Match cmd value	SW
	PC01	TURN_ON_PCLWA		RD	CR_PCLW_A_ON =1			s/b true	D
	PC02	TURN_ON_PCLWB		RD	CR_PCLW_B_ON =1			s/b true	D
	PC03	TURN_ON_PCLW_AB		RD	CR_PCLW_A_ON =1	CR_PCLW_B_ON =1	(PS& SA can be both On)	Both s/b true	D
	PC04	TURN_OFF_PCLW		RD	CR_PCLW_A_ON =0	CR_PCLW_B_ON =0		Both s/b true	D
18	PC05	TURN_ON_PC_ECAL		R	CR_PCLWA_ECAL_ON =1	CR_PCLWB_ECAL_ON =1		Active side s/b true	D
18	PC06	TURN_OFF_PC_ECAL		R	CR_PCLWA_ECAL_ON =0	CR_PCLWB_ECAL_ON =0		Active side s/b true	D
	PS01	TURN_ON_PS1		RS	CR_PS1_ON =1			s/b true	DS
	PS02	TURN_ON_PS2		RS	CR_PS2_ON =1			s/b true	DS
	PS03	TURN_ON_PS1_PS2		RS	CR_PS1_ON =1	CR_PS2_ON =1	(PC & SA can be both On)	Both s/b true	DS
	PS04	TURN_OFF_PS1PS2A		RS	CR_PS1_ON =0	CR_PS2_ON =0		Both s/b true	DS
	PS05	TURN_OFF_PS1PS2B		RS	CR_PS1_ON =0	CR_PS2_ON =0		Both s/b true	DS
	PS06	ENABLE_PS12SHDN		RS	CR_PS1SHDN_ENA_S =1, CR_PS2SHDN_ENA_S =1	CR_PS1SHDN_ENA_M =1, CR_PS2SHDN_ENA_M =1		All s/b true	DS
	PS07	DISABLE_PS12SHDN		RS	CR_PS1SHDN_ENA_S =0, CR_PS2SHDN_ENA_S =0	CR_PS1SHDN_ENA_M =0, CR_PS2SHDN_ENA_M =0		All s/b true	DS
	PS08	ENABLE_PS1_SVHTR		RS	CR_PS1SRVHTR_ENA=1			s/b true	DS
	PS09	ENABLE_PS2_SVHTR		RS	CR_PS2SRVHTR_ENA=1			s/b true	DS
	PS10	DISABLE_PS_SVHTR		RS	CR_PS1SRVHTR_ENA=0	CR_PS2SRVHTR_ENA=0		Both s/b true	DS
	PV01	TURN_ON_PVVISA		R	CR_VIS_A_ON =1	CR_VIS_B_ON =0		Both s/b true	D
	PV02	TURN_ON_PVVISB		R	CR_VIS_B_ON =1	CR_VIS_A_ON =0		Both s/b true	D
	PV03	TURN_OFF_PVVIS		R	CR_VIS_A_ON =0	CR_VIS_B_ON =0		Both s/b true	D
18	PV04	SET_PVVIS_ECAL	TO ON/OFF	SWD	CR_VISA_ECAL_ON =1/0	CR_VISB_ECAL_ON =1/0		Active side s/b true	D
1,18	PV05	SET_PVVIS_VCAL	TO X#XX	SW	VR_PVVIS_VCALH	Eng Pkt T30-5C or T30-5D		Match tlmy or pkt value	APV
	PV06	SET_PVVIS_ITWK_V	TO X#XX	SW	Eng Pkt			Eng Pkt	APV
	PV07	TURN_ON_PVNIRA		R	CR_NIR_A_ON =1	CR_NIR_B_ON =0		Both s/b true	D
	PV08	TURN_ON_PVNIRB		R	CR_NIR_B_ON =1	CR_NIR_A_ON =0		Both s/b true	D
	PV09	TURN_OFF_PVNIR		R	CR_NIR_A_ON =0	CR_NIR_B_ON =0		Both s/b true	D
	PV10	SET_PVNIR_ECAL	TO ON/OFF	SWD	CR_NIRA_ECAL_ON =1/0	CR_NIRB_ECAL_ON =1/0		Active side s/b true	D
1,18	PV11	SET_PVNIR_V CAL	TO X#XX	SW	VR_PVNIR_VCALH	Eng Pkt T30-5C or T30-5D		Match tlmy or pkt value	APV
	PV12	SET_PVNIR_ITWK_V	TO X#XX	SW	Eng Pkt			Eng Pkt	APV
	PV13	TURN_ON_PVSMIRA		R	CR_SMIR_A_ON =1	CR_SMIR_B_ON =0		Both s/b true	D
	PV14	TURN_ON_PVSMIRB		R	CR_SMIR_B_ON =1	CR_SMIR_A_ON =0		Both s/b true	D
	PV15	TURN_OFF_PVSMIR		R	CR_SMIR_A_ON =0	CR_SMIR_B_ON =0		Both s/b true	D
	PV16	SET_PVSMIR_ECAL	TO ON/OFF	SWD	CR_SMIRA_ECAL_ON =1/0	CR_SMIRB_ECAL_ON =1/0		Active side s/b true	D
1,18	PV17	SET_PVSM_VCAL	TO X#XX	SW	VR_PVSM_VCALH	Eng Pkt T30-5C or T30-5D		Match tlmy or pkt value	APV
	PV18	SET_PVSMIR_CSUB	TO ON/OFF	SWD	CR_SMIRA_CSUB_ON =1/0	CR_SMIRB_CSUB_ON =1/0		Active side s/b true	D
	PV19	SET_PVSM_ITWK_V	TO X#XX	SW	Eng Pkt			Eng Pkt	APV
	PV20	SET_PVSM_VDET_V	TO X#XX	SW	Eng Pkt			Eng Pkt	APV
	PV21	TURN_ON_PVLWA		R	CR_LWIR_A_ON =1	CR_LWIR_B_ON =0		Both s/b true	D

TABLE 40-2. MODIS COMMAND & TELEMETRY RESPONSE

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	PV22	TURN_ON_PVLWB		R	CR_LWIR_B_ON =1	CR_LWIR_A_ON =0		Both s/b true	D
	PV23	TURN_OFF_PVLW		R	CR_LWIR_A_ON =0	CR_LWIR_B_ON =0		Both s/b true	D
	PV24	SET_PVLW_ECAL	TO ON/OFF	SWD	CR_LWIRA_ECAL_ON =1/0	CR_LWIRB_ECAL_ON =1/0		Active side s/b true	D
1,18	PV25	SET_PVLW_VCAL	TO X#XX	SW	VR_PVLW_VCALH	Eng Pkt T30-5C or T30-5D		Match tlmy or pkt value	APV
	PV26	SET_PVLW_CSUB	TO ON/OFF	SWD	CR_LWIRA_CSUB_ON =1/0	CR_LWIRB_CSUB_ON =1/0		Active side s/b true	D
	PV27	SET_PVLW_ITWK_V	TO X#XX	SW	Eng Pkt			Eng Pkt	APV
	PV28	SET_PVLW_VDET_V	TO X#XX	SW	Eng Pkt			Eng Pkt	APV
	PV29	ENABLE_PV_ECAL		R	CR_PV_ECAL_ENA_A =1	CR_PV_ECAL_ENA_B =1		Active side s/b true	D
	PV30	DISABLE_PV_ECAL		R	CR_PV_ECAL_ENA_A =0	CR_PV_ECAL_ENA_B =0		Active side s/b true	D
	PV31	SET_PV_MEM	TO ROM/RAM	SWD	CR_PV_A_MEM_RAM =1/0	CR_PV_B_MEM_RAM -1/0		Active side s/b true	D
10	PV32	SET_PVVIS_NSTEP	TO D#XX	SW	Effect in Sci Pkt			Sci Pkt	na
10	PV33	SET_PVNIR_NSTEP	TO D#XX	SW	Effect in Sci Pkt			Sci Pkt	na
10	PV34	SET_PVSM_NSTEP	TO D#XX	SW	Effect in Sci Pkt			Sci Pkt	na
10	PV35	SET_PVLW_NSTEP	TO D#XX	SW	Effect in Sci Pkt			Sci Pkt	na
18	RC01	TURN_ON_RCLWTLM		R	CR_RC_LWTLM_ON =1			As noted	D
18	RC02	TURN_ON_RCLWHTR		R	CR_RC_LWHTR_ON =1		RC01 S/B On to get RC02 On	As noted	D
18	RC03	TURN_OFF_RCLWHTR		R	CR_RC_LWHTR_ON =0			As noted	D
18	RC04	TURN_OFF_RCLWTLM		R	CR_RC_LWTLM_ON =0			As noted	D
18	RC05	TURN_ON_RCSMTLM		R	CR_RC_SMTLM_ON =1			As noted	D
18	RC06	TURN_ON_RCSMHTR		R	CR_RC_SMHTR_ON =1		RC05 S/B On to get RC06 On	As noted	D
18	RC07	TURN_OFF_RCSMHTR		R	CR_RC_SMHTR_ON =0			As noted	D
18	RC08	TURN_OFF_RCSMTLM		R	CR_RC_SMTLM_ON =0			As noted	D
	RC09	SET_RC_CFPA_TEMP	TO T1/T2/T3	R R R	CR_RC_CFPA_T1SET =1, CR_RC_CFPA_T3SET =0	CR_RC_CFPA_T1SET =0, CR_RC_CFPA_T3SET =0	CR_RC_CFPA_T1SET =0, CR_RC_CFPA_T3SET =3	Selected T1/T2/T3 set s/b true (T2 is indirect from T1/T3)	D
	RC10	TURN_ON_RCCSTLM		R	CR_RC_CSTLM_ON =1			As noted	D
	RC11	TURN_ON_RCCSHTR		R	CR_RC_CSHTR_ON =1		RC10 S/B On to get RC11 On	As noted	D
	RC12	TURN_OFF_RCCSHTR		R	CR_RC_CSHTR_ON =0			As noted	D
	RC13	TURN_OFF_RCCSLTM		R	CR_RC_CSTLM_ON =0			As noted	D
18	RC14	TURN_ON_RCISTLM		R	CR_RC_ISTLM_ON =1			As noted	D
18	RC15	TURN_ON_RCISHTR		R	CR_RC_ISHTR_ON =1		RC14 S/B On to get RC15 On	As noted	D
18	RC16	TURN_OFF_RCISHTR		R	CR_RC_ISHTR_ON =0			As noted	D
18	RC17	TURN_OFF_RCISLTM		R	CR_RC_ISTLM_ON =0			As noted	D
18	RC18	TURN_ON_RCOSTLM		R	CR_RC_ISTLM_ON =1		RC18 S/B On to get RC19 On	As noted	D
18	RC19	TURN_ON_RCOSHTR		R	CR_RC_OSHTR_ON =1			As noted	D
18	RC20	TURN_OFF_RCOSHTR		R	CR_RC_OSHTR_ON =0			As noted	D
18	RC21	TURN_OFF_RCOSLTM		R	CR_RC_OSTLM_ON =0			As noted	D
	SA01	TURN_ON_SAA		R	CR_SA_A_SCAN_ON =1			As noted	D
	SA02	TURN_ON_SAB		RD	CR_SA_B_SCAN_ON =1			As noted	D
	SA03	TURN_ON_SA_AB		RD	CR_SA_A_SCAN_ON =1	CR_SA_B_SCAN_ON =1	(PS& PC can be both On)	Both s/b true, A/B both On	D
	SA04	TURN_OFF_SA		RD	CR_SA_A_SCAN_ON =0	CR_SA_B_SCAN_ON =0		Both s/b true	D
	SA05	SET_SA_HIGAIN		R	CR_SA_A_HI_GAIN =1			As noted	D
	SA06	SET_SA_LOGAIN		R	CR_SA_A_HI_GAIN =0			As noted	D
	SA07	SET_SB_HIGAIN		R	CR_SA_B_HI_GAIN =1			As noted	D

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pf chgs	1 Subsys	2 OASIS Command Name	3 Qualifier or Value	4 Cmd Type	5 Primary Verification	6 Continuing/Indirect Verification	7 Additional Data	8 Remarks	9 Tlmy Type
	SA08	SET_SB_LOGAIN		R	CR_SA_B_HI_GAIN =0			As noted	D
5	SM01	TURN_ON_SMA		R	CR_SM_SDSM_A_ON =1	CR_SM_SDSM_B_ON =0		As noted	D
5	SM02	TURN_ON_SMB		R	CR_SM_SDSM_B_ON =1	CR_SM_SDSM_A_ON =0		As noted	D
	SM03	TURN_OFF_SM		R	CR_SM_SDSM_A_ON =0	CR_SM_SDSM_B_ON =0		Both s/b true	D
7	SM04	SET_SM _FULL_CAL	WITH SCANS D#XX	SW	CR_SM_MIR_HOME_A =0	CR_SM_MIR_HOME_B =0	1 at start, repeating 0/1 then end at 0; also by Eng Pkt	True at spots; also in Eng Pkt	SW
7	SM05	SET_SM _SD_CAL	WITH SCANS D#XX	SW	CR_SM_MIR_HOME_A =0	CR_SM_MIR_HOME_B =0	1 at start, repeating 0/1 then end at 0; also by Eng Pkt	True at spots; also in Eng Pkt	SW
7	SM06	SET_SM _SUN_CAL	WITH SCANS D#XX	SW	CR_SM_MIR_HOME_A =0	CR_SM_MIR_HOME_B =0	1 at start, repeating 0/1 then end at 0; also by Eng Pkt	True at spots; also in Eng Pkt	SW
13	SM07	STEP_SM_MIR	BY D#XX FORWARD/BACKWARD	SW	CS_SM_MIR_STEP	(tlmy is in absolute step count, see T20-2A)		New tlmy s/b cmded delta from prior tlmy	SW
	SM08	HALT_SM_MIR_MTR		SW	CR_SM_MIR_HOME_A =1, CS_SM_MIR_STEP	CR_SM_MIR_HOME_B =1	<-any may stop short for SM05,06,07,08	As noted	SW
18	SR01	TURN_ON_SRA		R	CR_SR_A_ON =1	CR_SR_B_ON =0		Both s/b true	D
18	SR02	TURN_ON_SRB		R	CR_SR_B_ON =1	CR_SR_A_ON =0		Both s/b true	D
	SR03	TURN_OFF_SR		R	CR_SR_A_ON =0	CR_SR_B_ON =0		Both s/b true	D
11	SR04	SET_SR_SIPD_HTR	TO ON/OFF	SW	CR_SR_SISHTR_OFF =0/1			Match cmd HK or Eng Pkt	SW
11	SR05	SET_SR_L10Wx3	TO B#ABCD (4 items)	SW	CS_SR_USE_L10WX3	B#1/0 for ea bit for lamps 1,2,3,4		Match cmd HK or Eng Pkt	SW
11	SR06	SET_SR_L10WX2	TO B#ABCD (4 items)	SW	CS_SR_USE_L10WX2	B#1/0 for ea bit for lamps 1,2,3,4		Match cmd HK or Eng Pkt	SW
11	SR07	SET_SR_L10WX1	TO B#ABCD (4 items)	SW	CS_SR_USE_L10WX1	B#1/0 for ea bit for lamps 1,2,3,4		Match cmd HK or Eng Pkt	SW
11	SR08	SET_SR_L1WX1	TO B#AB (2 items)	SW	CS_SR_USE_L1WX1	B#1/0 ea AB from lamps 5,6		Match cmd HK or Eng Pkt	SW
11	SR09	SET_SR_SIS_FB	TO RADIANCE/CURRENT	SW	CR_SR_SISFB_RAD = 0/1			Match cmd HK or Eng Pkt	SW
11	SR10	SET_SR_LOV_SHDN	TO ENABLE/DISABLE	SW	CR_SR_L_SHDN_ENA = 0/1			Match cmd HK or Eng Pkt	SW
11	SR11	SET_SR_LAMPLEVEL	TO HIGH/LOW	SW	CR_SR_LAMPS_LOW = 0/1			Match cmd HK or Eng Pkt	SW
11,25,26	SR12	SET_SR_LAMPS	TO OFF/W1/W10/W20/W30	SW	CS_SR_LAMPS =	OFF/WATT_ONE/WATT10/WATT20/WATT30=000/001/010/011/100		Match cmd HK or Eng Pkt	SW
18	SR13	SET_SR_MTR_GRP	WITH WH D#X, SL D#X, GR D#XXXXX	SW	CS_SR_SRCWH_STEP, CS_SR_SLIT_STEP	CS_SR_GRAT_STEP, by step count in tlmy	In Eng Pkt by functional position	Match cmd HK or Eng Pkt	SW
13	SR14	STEP_SR_WHEEL	BY D#XXX FORWARD/BACKWARD	SW	CS_SR_SRCWH_STEP	(tlmy is in absolute step count, see T20-2A)		New tlmy s/b cmded delta from prior tlmy	SW
16	SR15	SR_SPARE		SW	na			na	SW
13	SR16	STEP_SR_SLIT	BY D#XX FORWARD/BACKWARD	SW	CS_SR_SLIT_STEP	(tlmy is in absolute step count, see T20-2A)		New tlmy s/b cmded delta from prior tlmy	SW
16	SR17	SR_SPARE		SW	tbd				SW
13	SR18	STEP_SR_GRT	BY D#XXXXX FORWARD/BACKWARD	SW	CS_SR_GRAT_STEP	(tlmy is in absolute step count, see T20-2A)		New tlmy s/b cmded delta from prior tlmy	SW
18	SR19	STEP_SR_GR_BSS	WITH BURST D#XXX, STEPS D#XX FORWARD /BACKWARD, SCANS D#XXX	SW	CS_SR_GRAT_STEP			Observe tlmy for step chg & pause sequences	SW
18	SR20	HALT_SR_GRT_MTR		SW	CS_SR_GRAT_STEP			Halt in changing step count	SW
10	SR21	SET_SR_IR_SRC	TO ON/OFF	SW	CR_SR_IR_SRC_OFF =0/1			As noted	SW
	TG01	TURN_ON_TGA		R	CR_TG_A_ON =1	CR_TG_B_ON =0		Both s/b true	D
	TG02	TURN_ON_TGB		R	CR_TG_B_ON =1	CR_TG_A_ON =0		Both s/b true	D

TABLE 40-2. MODIS COMMAND & TELEMETRY RESPONSE

Sort by Subsystem *A/B redundant subsystems have general A_On/B_Off command structure, except PC, PS & SA can have both sides on at same time.* *5/97*

pf chgs	1 Subsys	2 OASIS Command Name	3 Qualifier or Value	4 Cmd Type	5 Primary Verification	6 Continuing/Indirect Verification	7 Additional Data	8 Remarks	9 Tlmy Type
	TG03	TURN_OFF_TG		R	CR_TG_A_ON =0	CR_TG_B_ON =0		Both s/b true	D
	TG04	RESET_TG		SWD	tbd				
	216	*<--Total cmds*							

NOTES

1. All subsystem configuration ON/OFF cmds have HK tlmy status words. Most other configuration parameter selections also have HK tlmy points. Other command selections only appear in the Engineering Pkts or have direct video effects in the Science Pkts.
2. Shaded items are processed as spacecraft pt-pt items.

TABLE 40-2. MODIS COMMAND & TELEMETRY RESPONSE

Sort by Subsystem *A/B redundant subsystems have general A_On/B_Off command structure, except PC, PS & SA can have both sides on at same time.* *5/97*

pf chgs	1 Subsys	2 OASIS Command Name	3 Qualifier or Value	4 Cmd Type	5 Primary Verification	6 Continuing/Indirect Verification	7 Additional Data	8 Remarks	9 Tlmy Type

PF Chg History to T40-1 Starting 8/95

1. 11/24/95 chg ECAL_V to VCAL in 4 cmds: PV05, 11, 17, 25; also add tlmy name in Col 5 and move Eng Pkt to Col6.
2. 11/24/95 (other tables chged 11/4) Chg FR28 SET_FR_PC_DCR_TH to FR_SPARE and FR30 for PV.
3. 11/24 added Col 5 tlmy for 5 view sector delay cmds, e.g., CS_FR_DELAY_SD, BB, SR, SP, EA.
4. 11/24 (Other tables changed 11/6) Chg FO06 from RESET_FO to FO_SPARE.
5. 11/24 Add Col 6 veirfication for SM01 & SM02, the relate A/B sides.
6. 11/24 On DR13, deleted Col 6 tlmy CR_DR_SDS_CLSD as it as become a spare since SDD_CLSD indicates SDS is closed.
7. 11/24 Revised mtr home logic start/end on SM04, 05, 06 such that at start & end, home true is 0.
8. 12/3 Added missing 2nd verification states to BB01, BB02, CE01, CE02. E.G., BB01s/b CR_BB_A_PWR_ON =1 & CR_BB_B_PWR_ON =0, etc.
9. 12/3 Corrected 3 logic states: CP01 is CR_CP_A_ON_S =0 not 1, CP02 is CR_CP_B_ON_S =0 not 1, and CP06 is CR_CP_SET_TMF_A =0 not 1.
10. 3/22/96 17 New cmds CP24-26, FR31-FR46 & SR21.
11. 3/22/96 Revised 9 SR cmds SR04-SR12.
12. 3/22/96 Revised DR13 tlmy logic to show states for 3 cases SDD_Clsd/SCRN-Clsd, SDD_Open/SCRN-Clsd, SDD_Open/SCRN_Open.
13. 3/23/96 Added missing HK tlmy for FR07, SM07, SR14, SR16, SR18
14. 3/22/96 Clarify FR APID/Quick look flag items, including deletion of prior memory pkt items FR14, 15 & 16.
15. 3/23/96 Revise FR04 to TOGGLE_FR_INT02 from TEST_FR_SELF.
16. 3/24/96 ReVised to Spares: CP18 to CP_SPARE, FR25 to FR_SPARE, SR15, 17 to SR_SPARE.
17. 3/24/96 CP15 revise qualifier.
18. 3/26/96 Minor clarifications on response.
19. 4/7/96 Minor FR26 name chg to SET_FR_PKT_TYPE from SET_FR_SCI_PKT to be consisitent with other new items. And to SS_FR_PKT_TYPE from SS_FR_SCI_PKT.
20. 4/29/96 Revise FR15 to SET_FR_RESTART WITH ASTATE X#X from Chg#14 FR_SPARE.

----------Changes since 151840 initial 5/96 release----------

21. 8/12/96 Slightly revise DR27 & FR31 Col 3 so they match T10-25A DR27 & FR31 syntax.

[22] 8/15/96 Delete cmds CP21, FR43, FR44 & FR45 and related tlmy. Chgs are carried as spares in T10-25A & T20-2A, but not in T40-1.

23. 9/29/96 Add 4th character to BB04 Qualifer to get D#XXXX.
24. 9/26/96 Correct Qualifer syntax on FR35,36,37,38 & SR12 to match OASIS rqmts and T10-25A.
25. 10/18/96 Reactivate FR16 to be SET_FR_SCIABNORM TO ABNORM/NORM and add tlmy SS_FR_SCIABNORM (ABNORM/NORM).
26. 4/97 EO1122D incoporation for Rev B. See EO1122D, released 970305 for details.
27. 5/97 Direct Rev B change on qualifiers to match same changes in Table 10-25A.

[28] 5/97 Direct Rev B change to revise last Col number from 10 to 9 for Tlmy Type.

TABLE 40-3. MODIS CONTROL PROCESSOR DEFAULTS

5/97

Param ID#	Cmd#	Command Mnemonic	Parameter Description	SW Range HEX, unless noted	Default Value HEX, unless noted
1	BB04	SET_BB_HTR_TEMP TO D#XXX	BB Heater Temp Set Point, nominal T=315K=D#151DN=X#0097	0062-0F44	0093
2	CP06	SET_CP_TMF_BUS TO A/B	Select CP TMF Bus 0=A, 1=B	0000=A 0001=B	0000=A
3	TG04	RESET_TG	Reset Timing Generator (Reset=0; negative transition created by Flt SW stepping 1, then 0; no gnd Set cmd)	0000=RESET	na
4	-	SPARE	na	na	na
5	FR08	SET_FR_SCI_APID TO D#XXX	Science Data Packet APID	0040-007F	0040
6	FR09	SET_FR_SCI_QLK, RESET_FR_SCI_QLK	Science Data Packet QL bit	0001=SET 0000=RESET	0000=RESET
7	FR11	SET_FR_ENG_APID TO D#XXX	Engineering Packet APID	0040-007F	0040
8	FR12	SET_FR_ENG_QLK, RESET_FR_ENG_QLK	Engineering Packet QL bit	0001=SET 0000=RESET	0000=RESET
9	FR14	SPARE	(Was Memory Data Packet APID)	na	na
10	FR16	SPARE	(Was Memory Data Packet QL bit)	na	na
11	FR17	SET_FR_SD_DELAY TO D#XXX	SD Sector Delay (1=6.66us) All band operational test delay	0000-0032	0000
12	FR18	SET_FR_SR_DELAY TO D#XXX	SR Sector Delay (1=6.66us) All band operational test delay	0000-0032	0000
13	FR19	SET_FR_BB_DELAY TO D#XXX	BB Sector Delay (1=6.66us) All band operational test delay	0000-0032	0000
14	FR20	SET_FR_SP_DELAY TO D#XXX	SPACE Sector Delay (1=6.66us) All band operational test delay	0000-0032	0000
15	FR21	SET_FR_EA_DELAY TO D#XXX	EARTH Sector Delay (1=6.66us) All band operational test delay	0000-0032	0000
16	CP07	SET_CP_OPER_MODE TO SRV/SAF/STBY/OG/SCI	MODIS Operating MODE	0001=SURVIVAL, 0002=SAFE, 0003=STANDBY, 0004=OUTGAS, 0005=SCIENCE	0003=STANDBY
17	CP04,05	ENABLE_CP_IMOK DISABLE_CP_IMOK	Enable Autonomous Safe Mode (monitor S/C IMOK over 1553)	0001=ENABLED 0000=DISABLED	0000=DISABLED
18	SR05	SET_SR_L10WX3 TO B#ABCD	Set 3x10W Lamp Config (selects 3 particular lamps)	B#1110=Lamps 1,2,3 B#1101=Lamps 1,2,4 B#1011=Lamps 1,3,4 B#0111=Lamps 2,3,4	B#1110 = 1,2,3
19	SR06	SET_SR_L10WX2 TO B#ABCD	Set 2x10W Lamp Config (selects 2 particular lamps)	B#1100=Lamps 1,2 B#1010=Lamps 1,3 B#1001=Lamps 1,4 B#0110=Lamps 2,3 B#0101=Lamps 2,4 B#0011=Lamps 3,4	B#0110 = 2,3
20	SR07	SET_SR_L10WX3 TO B#ABCD	Set 1x10W Lamp Config (selects 1 particular lamp)	B#1000=Lamp 1, B#0100=Lamp 2 B#0010=Lamp 3, B#0001=Lamp 4	B#1000 = 1
21	FR08	SET_SR_L1WX1 TO B#AB	Set 1x 1W Lamp Config (selects 1 particular lamp)	B#10=Lamp 5 B#01=Lamp 6	B#10 = 5
22	CP21	SET_CP_PK_PWR TO D#XXXX	(Was SET_CP_PEAK_PWR)	na	na
23	FR07	SET_FR_RATE TO DAY/NIGHT	Formatter Day/Night Rate	0001=Day 0000=Night	0001=Day
24	FR04	TOGGLE_FR_INT02	Formatter Interrupt02 Toggle FLT SW toggles B#0,1,0 for test	0000=TOGGLE	na

TABLE 40-3. MODIS CONTROL PROCESSOR DEFAULTS

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Param ID#	Cmd#	Command Mnemonic	Parameter Description	SW Range HEX, unless noted	Default Value HEX, unless noted
25	FR05	RESET_FR_STD	Reset Formatter Standard (Reset=0; negative transition created by Flt SW stepping 1, then 0; no gnd Set cmd)	0000=RESET	na
26	FR22	RESET_FR_UPLD	Reset Formatter Upload (Reset=0; negative transition created by Flt SW stepping 1, then 0; no gnd Set cmd)	0000=RESET	na
27	FO06	SPARE	(Was Reset FIFO)	na	na
28	FI04	RESET_FI	Reset FDDI (Reset=0; negative transition created by Flt SW stepping 1, then 0; no gnd Set cmd)	0000=RESET	na
29	DR03	OPEN_DR_UL_LOCK	Must be issued prior to param#30,#31 & #32; SW cancels cmd automatically after 10 sec	0001=OPEN	NOT OPEN
30	DR04	SET_DR_SVD_UL TO ON/OFF	SVD paraffin htr: 0=ON, 1=OFF (irreversible; must occur within 10 sec of param#29; SW timer OFF at 11.6 min.	0000=ON 11.6 min 0001=OFF	0001=OFF
31	DR05	SET_DR_NAD_UL TO ON/OFF	NAD paraffin htr: 0=ON, 1=OFF (irreversible; must occur within 10 sec of param#29; SW timer OFF at 11.6 min.	0000=ON 11.6 min 0001=OFF	0001=OFF
32	DR06	SET_DR_SDD_UL TO ON/OFF	SDD paraffin htr: 0=ON, 1=OFF (irreversible; must occur within 10 sec of param#29; SW timer OFF at 11.6 min.	0000=ON 11.6 min 0001=OFF	0001=OFF
33	DR27	SET_DR_SDD_FS TO ON/OFF	SDD FS parafin htr: 0=ON,1=OFF (irreversible; must occur within 10 min of SDD FS circuit turn ON; SW timer OFF at 11.6 min.	0000=ON 11.6 min 0001=OFF	0001=OFF
34	PV04	SET_PVVIS_ECAL TO ON/OFF	PV VIS ECAL ON/OFF Electronic Calibation	0000=OFF 0001=ON	0000=Off
35	PV05	SET_PVVIS_VCAL	PV VIS VCAL Volts -8V to +1V over 8 bits	0000=+1V 00FF=-8V	001D=D#29
36	PV06	SET_PVVIS_ITWK_V	PV VIS ITWK Volts -2.5V to -4.5V over 8 bits	0000=-2.5V 00FF=-4.5V	004F=D#79
37	PV10	SET_PVNIR_ECAL TO ON/OFF	PV NIR ECAL ON/OFF Electronic Calibation	0000=OFF 0001=ON	0000=Off
38	PV11	SET_PVNIR_VCAL	PV NIR VCAL Volts -8V to +1V over 8 bits	0000=+1V 00FF=-8V	001D=D#29
39	PV12	SET_PVNIR_ITWK_V	PV NIR ITWK Volts -2.5V to -4.5V over 8 bits	0000=-2.5V 00FF=-4.5V	004F=D#79
40	PV16	SET_PVSMIR_ECAL TO ON/OFF	PV SWIR/MWIR ECAL ON/OFF Electronic Calibation	0000=OFF 0001=ON	0000=Off
41	PV17	SET_PVSM_VCAL	PV SWIR/MWIR VCAL Volts -8V to +1V over 8 bits	0000=+1V 00FF=-8V	001D=D#29
42	PV19	SET_PVSM_ITWK_V	PV SWIR/MWIR ITWK Volts -2.5V to -4.5V over 8 bits	0000=-2.5V 00FF=-4.5V	004F=D#79
43	PV20	SET_PVSM_VDET_V	PV SMIR/MWIR VDET Volts 0V to -8V over 8 bits	0000=-8V 00FF=0V	00BE=D#190
44	PV24	SET_PVLWIR_ECAL TO ON/OFF	PV LWIR ECAL ON/OFF Electronic Calibation	0000=OFF 0001=ON	0000=Off
45	PV25	SET_PVLW_VCAL	LWIR VCAL Volts -8V to +1V over 8 bits	0000=+1V 00FF=-8V	001D=D#29
46	PV27	SET_PVLW_ITWK_V	PV LWIR ITWK Volts -2V to -4V over 8 bits	0000=-2.5V 00FF=-4.5V	004F=D#79
47	PV28	SET_PVLW_VDET_V	PV LWIR VDET Volts 0V to -8V over 8 bits	0000=-8V 00FF=0V	00B9=D#185
48	PV18	SET_PVSMIR_CSUB TO ON/OFF	SWIR/MWIR Chrg Subtraction ON/OFF, uses ECAL_V for volts	0000=OFF 0001=ON	0000=Off
49	PV26	SET_PVLW_CSUB TO ON/OFF	LWIR Chrg Subtraction ON/OFF, uses ECAL_V for volts	0000=OFF 0001=ON	0000=Off
50	PV31	SET_PV_MEM TO ROM/RAM	PV Memory ROM/RAM normal:RAM; test only:ROM	0000=ROM 0001=RAM	0001=RAM

TABLE 40-3. MODIS CONTROL PROCESSOR DEFAULTS

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Param ID#	Cmd#	Command Mnemonic	Parameter Description	SW Range HEX, unless noted	Default Value HEX, unless noted
51	FR26	SET_FR_PKT_TYPE TO NORMAL/TEST	FR Packet, Normal is Science, Test creates a fixed CCSDS test packet to check link	0000=NORMAL 0001=TEST	0000=NORMAL
52	FR29	SET_FR_PV_DCRCMP TO ON/OFF	PV DCR computation: 1=ON,0=OFF	0000=OFF 0001=ON	0001=ON
53	FR27	SET_FR_PC_DCRCMP TO ON/OFF	PC DCR computation: 1=ON,0=OFF	0000=OFF 0001=ON	0001=ON
54	FR30	SPARE	(Was PV DCR threshold of BB)	na	na
55	FR28	SPARE	(Was PC DCR threshold of BB)	na	na
56	FR44	SET_FR_PCDCRPRE TO ON/OFF	(Was SET_FR_PCDCRPRE)	na	na
57	FR45	SET_FR_PCDCRPOST TO ON/OFF	(Was SET_FR_PCDCRPOST)	na	na
58	FR43	SET_FR_PCDCRDBG TO ON/OFF	(SET_FR_PCDCRDBG)	na	na
59	FR31	SET_FR_ENC_DELTA	Delta rotates all 5 MODIS views by fixed encoder count	E000=MIN (-8192) 1FFF=MAX (+8191)	0000
60	FR32	SET_FR_BBRADTAB TO NORMAL/TEST	Uses value fixed by FR35 for all ideal BBDY values	0000=TEST 0001=NORMAL	0001=NORMAL
61	FR33	SET_FR_OFFSETTAB TO NORMAL/TEST	Uses value fixed by FR36 and FR37 for offset loading	0000=TEST 0001=NORMAL	0001=NORMAL
62	FR34	SET_FR_GAINTAB TO NORMAL/TEST	Uses value fixed by FR38 for gain loading	0000=TEST 0001=NORMAL	0001=NORMAL
63	FR35	TEST_FR_BBRAD	Specifies 8 bit value for use by FR32	0000=MIN 00FF=MAX	03E8
64	FR36	TEST_FR_PVOFFSET	Specifies 8 bit value for use by FR33	0000=MIN 00FF=MAX	0080
65	FR37	TEST_FR_PCOFFSET	Specifies 14-bit value for use by FR33	0000=MIN 3FFF=MAX	2080
66	FR38	TEST_FR_PVGAIN	Specifies 8 bit value for use by FR34	0000=MIN 00FF=MAX	0000
67	PV32	SET_PVVIS_NSTEP	Sets PV VIS FPA step count for ECAL/CSUB mode.	0001=MIN 0028=MAX	000A
68	PV33	SET_PVNIR_NSTEP	Sets PV VIS FPA step count for ECAL/CSUB mode.	0001=MIN 0028=MAX	000A
69	PV34	SET_PVSM_NSTEP	Sets PV VIS FPA step count for ECAL/CSUB mode.	0001=MIN 0028=MAX	0028
70	PV35	SET_PVLW_NSTEP	Sets PV VIS FPA step count for ECAL/CSUB mode.	0001=MIN 0028=MAX	000A
71	SR04	SET_SR_SIPD_HTR TO ON/OFF	Turns SRCA SIS RAD SiPD Heater to ON or OFF	0000=OFF 0001=ON	0000=OFF
72	SR09	SET_SR_SIS_FB TO RADIANCE/CURRENT	Turns SIS Feedback Control to RADIANCE or CURRENT	0000=CURRENT 0001=RADIANCE	0001=RADIANCE (SEE NOTE 1)
73	SR10	SET_SR_LOV_SHDN TO ENABLE/DISABLE	Set SIS Lamp Overvoltage Shutdown to ENABLE or DISABLE.	0000=ENABLE 0001=DISABLE	0001=DISABLE (SEE NOTE 1)
74	SR11	SET_SR_LAMPLEVEL TO HIGH/LOW	Set SRCA Lamp Level to HIGH or LOW.	0000=LOW 0001=HIGH	0001=HIGH
75	SR12	SET_SR_LAMPS TO OFF/1W/10W/20W/30W	Sets SRCA Lamps to the configuration set by this commands and SR05-SR08	0000=OFF 0001=1W 0010=10W 0011=20W 0100=30W	0000=Off (SEE NOTE 1)
76	SR21	SET_SR_IR_SRC TO ON/OFF	Turns SRCA IR Source ON or OFF	0000=OFF 0001=ON	0000=Off
77	CP26	SET_CP_LOG_STATE TO D#XX	Sets Operand & Instruction class of loads & dumps	0000=00 000F=15	0000
78	FR46	SET_CP_LOG_STATE TO D#XX	Sets Operand & Instruction class of loads & dumps	0000=00 000F=15	0000

TABLE 40-3. MODIS CONTROL PROCESSOR DEFAULTS

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Param ID#	Cmd#	Command Mnemonic	Parameter Description	SW Range HEX, unless noted	Default Value HEX, unless noted

Notes:

1. For any of these commands, before the new setting is sent to the calibrator, the SRCA lamps are turn off, and a 3 second delay is enforced. After the delay, the new command is sent. When changing the feedback control mode, the lamps are returned to their prior state with the new feedback mode set. When disabling the Overvoltage Shutdown, the lamps are left off.

Table 40-3 Change History

1. 12/10/96 Table is new for Rev A.
2. 4/97 direct change for Rev B incorporation: 1) all 4 PV FPA VCAL's to 29, 2) all 4 PV FPA ITWK_V's to79, 3) PV_SM_VDET_V to 190 and 4) PV_LW_VDET to 185.

TABLE 40-4. CONTROL PROCESSOR LOG EVENT CODES

Reference information only. See 152932 Maintenance Manual of the MODIS Flight Software System.

Msg Hex Code	Msg	Interpretation/Description
00	W IURT IUART Status Error	A status error occurred on the internal UART. This usually means the SW did not read a byte from the UART before the next byte arrived.
01	W CPMT Multiple Loads Disallowed	A Load Init command was received while a prior load command was still in process.
02	W CPMT Multiple Dumps Disallowed	A Dump Init command was received while a prior dump command was still in process.
03	W CPMT Internal Mem Xfer Failed	An attempt to read dump data or write load data was unsuccessful. For dumps, all zeros is returned.
04	W CPMT Invalid Dump Data from FP	Dump data was received from the formatter when none was expected.
05	W CPMT Invalid Dump Read by SC	The spacecraft read the dump data buffer before the data to be dumped was present in the buffer.
06	W CPMT Invalid Load Verify by FP	The FP sent a load verification message when no such message was expected
07	W CPMT Invalid Load Data from SC	Load data was received without a prior Load Init command.
08	W CPMT Invalid Load Count	The count of words received at the Load Data subaddress does not match the word count field of the Load Init command.
09	W CPMT Load Checksum Failed	The checksum in the Load command did not match the checksum computed on the load data. The load data will be discarded.
0A	W CPMT EEPROM Load Failed	This obsolete messages should never occur. Formerly indicated an error in the LOAD_EEPROM command.
0B	I CPMT Memory Transfers Cleared	Any Load or Dump commands currently in process have been cancelled.
0C	W CPMC CP Bad Message - Ignored	The SW which processes messages received by the CP was instructed to process a message which should only be transmitted by the CP.
0D	W MSGC Msg Registration Failed	Invalid parameters were specified in the call to register a message.
0E	W MSGC Invalid Xmit Parameters	The Send_Msg routine was called specifying an illegal or unregistered message, a message which has been registered as "receive-only", or with an invalid word count for the message.
0F	W MSGC Message Framing Error 1	An error was detected in the prefix of a message packet on the internal serial link. This is most likely due to an overwritten byte in the UART.
10	W MSGC Message Framing Error 2	The End of Packet delimiter was not found when expected on the internal serial link. This is usually due to an overwritten byte in the UART.
11	W MSGC Message Buffer Overflow	More data has arrived for a message than can be held by the buffer allocated to that message.
12	W CAL Invalid SDSM 10 offset	An invalid value was specified for SDSM detector 10 offset. OBSOLETE.
13	W CAL Invalid SDSM 11 offset	An invalid value was specified for SDSM detector 11 offset. OBSOLETE.
14	W CAL Bad 1 10W Lamp Config	An Invalid 1x10W lamp configuration was specified.
15	W CAL Bad 2 10W Lamp Config	An Invalid 2x10W lamp configuration was specified.
16	W CAL Bad 3 10W Lamp Config	An Invalid 3x10W lamp configuration was specified.
17	W CAL Bad 1 1W Lamp Config	An Invalid 1x1W lamp configuration was specified.
18	W CAL Bad Lamp Command Received	An lamp command was received which specified an illegal configuration
19	W CAL Bad Calib Motor Phase	An invalid Motor phase was commanded.
1A	W CAL Bad Calib Motor Type	An invalid calibration motor was specified.
1B	W MTR Invalid Motor Position	A motor was ordered to MOVE to an out of range position.
1C	W MTR Motor In Use	A motor was ordered to move while already in motion.
1D	W SDSM State Machine Failure	The SDSM State machine was INACTIVE during Trigger SDSM command execution.
1E	W SDSM Invalid SDSM Scan Count	SDSM_Control detected a negative scan count while processing a Trigger SDSM command.
1F	W SDSM Invalid Index parameter	SDSM_Control was told to collect samples outside of index range 1..3
20	W SRCA Grating Command Clash	A "Step_Grating" command was overridden by a "Set SRCA Motors" command.

TABLE 40-4. CONTROL PROCESSOR LOG EVENT CODES

Reference information only. See 152932 Maintenance Manual of the MODIS Flight Software System.

Msg Hex Code	Msg	Interpretation/Description
21	W SRCA Bad Filter Position	An invalid Filter position was specified as part of a "Set SRCA Motors" command. The entire command is discarded.
22	W SRCA Bad Slit Position	An invalid Slit position was specified as part of a "Set SRCA Motors" command. The entire command is discarded.
23	W SRCA Bad Grating Position	An invalid Grating position was specified as part of a "Set SRCA Motors" command. The entire command is discarded.
24	W BBDY BBDY algo high:using max	The BBDY heater control algorithm has resulted in too large a value.
25	W BBDY BBDY algo low:using min	The BBDY heater control algorithm has resulted in too low a value.
26	W DOOR Bad Door Parameters	An invalid door position was selected for the specified door.
27	W DOOR Doors locked by Safe/Srv	An attempt was made to open the doors while in SAFE or SURVIVAL mode.
28	W SUPR Bad SCC_OK Message	A message with the wrong value arrived at the SCC_OK subaddress. It will be ignored.
29	W SUPR Bad Safe Command Message	A message with the wrong value arrived at the Safe command subaddress. It will be ignored.
2A	W SUPR Bad Synch Data Word	An illegal Synch Data word was received. It will be ignored.
2B	W CIN Received Queue Overflow	The instrument command receive queue is full. The most recently received command cannot be placed in the queue and will be discarded.
2C	W CIN Received Queue Underflow	An attempt was made to read from the instrument command receive queue while is was empty.
2D	W CIN Command Queue Overflow	The Validated command queue is full. The most recently validated command cannot be placed in the queue and will be discarded.
2E	W CIN Received Queue Garbled	Data in the received command queue failed its validation. All data remaining in the receive queue is discarded.
2F	W CIN Load EEPROM Cmd Rejected	This obsolete message should never be received.
30	W CIN Restart Cmd Rejected	An invalid restart command was received.
31	W CIN Delay Macro Cmd Rejected	A Delay_Macro command was detected in the receive queue
32	W CIN Break Cmd Rejected	A Break command was detected in the receive queue
33	W CIN Unexpected Load Init	A Load Init command was received when a prior load command was still in process.
34	W CIN Unexpected Dump Init	A Dump Init command was received when a prior dump command was still in process.
35	W ICP Invalid Cmd Received	An attempt was made to execute a command with an unknown opcode.
36	W ICP Truncated Command Ignored	A multi-word command was truncated. The partial command is discarded.
37	W ICP Validated Command Garbled	The size field in a validated command does not match the command data table., or the parameters for the command fall outside their legal range.
38	W ICP Trigger SDSM Command Busy	A "Trigger_SDSM" command was received while an earlier one was still executing. The new command is ignored. If the new command came from a macro, the macro is aborted.
39	W ICP Step SRCA Command Busy	A "Step_SRCA_Grating" command was received while an earlier one was still executing. The new command is ignored. If the new command came from a macro, the macro is aborted.
3A	W ICP Delay Macro Cmd Ignored	A Delay_Macro command was found in the validated command queue. The queue is flushed.
3B	W ICP All Macros Busy	This obsolete event should never be received.
3C	W ICP Macro Already Running	A Macro command was received to run a macro when a macro was already running.
3D	W ICP Macro Cmd Ignored	A macro command was found inside another macro. The new command is ignored, and the running macro is aborted.
3E	W ICP Macro Cmd not Active	This obsolete message should never be received.
3F	W ICP Abort Macro Cmd Ignored	An Abort_Macro command specified a macro which was not active.
40	W ICP Break Cmd Ignored	A Break command was found in the validated command queue.

TABLE 40-4. CONTROL PROCESSOR LOG EVENT CODES

Reference information only. See 152932 Maintenance Manual of the MODIS Flight Software System.

Msg Hex Code	Msg	Interpretation/Description
41	W ICP Xfer Clear Cmd Ignored	A Halt Memory Transfer command had invalid parameters.
42	W ICP Load Init Cmd Ignored	A Load_Init command was found in the validated command queue.
43	W ICP Dump Init Cmd Ignored	A Dump_Init command was found in the validated command queue.
44	W ICP Load EEPROM Cmd Ignored	A Load_EEPROM command was found in the validated command queue.
45	W ICP Restart Cmd Ignored	A Restart command was found in the validated command queue.
46	W ICP Failsafe Circuitry Reset	The timeout on the failsafe circuitry has expired. The proper relay and digital commands have been sent to reset the failsafe circuitry.
47	W TLM Invalid Tlm. Request	A Non-Analog telemetry point was specified as the parameter to the Collect_Single_Point routine.
48	W LLC Invalid Param. Choice	An invalid parameter number has been specified in a command.
49	W LLC Invalid Param. Value	An out of range value has been specified for a legal parameter.
4A	W LLC Invalid Relay Choice	A non-existent relay has been commanded for execution.
4B	W LLC Restricted Cmd. Tried	A macro attempted to execute a restricted command.
4C	W LLC Unlatch Cmd Rejected	An unlatch command was attempted without first sending the SW enable for the unlatch commands.
4D	W LLC Invalid Power Telemetry	The Telemetry table has been altered, and the LLC unit can no longer determine the current power usage.
4E	W LLC Invalid Power Check Index	An out of range command has been selected for a power check.
4F	W LLC Power Limit Exceeded	A legal command would exceed the Current MODIS Power Limit
50	W CIE Undefined Interrupt-IRQ 5	An unused expansion interrupt (number 5) occurred
51	W CIE Undefined Interrupt-IRQ 6	An unused expansion interrupt (number 6) occurred
52	W CIE Float. Overflow Received	A floating point overflow interrupt occurred
53	W CIE Fixed Overflow Received	A fixed point overflow interrupt occurred
54	W CIE Float. Underflow Received	A floating point underflow interrupt occurred.
55	W CIE Byte Arrived at Test Port	A key was pressed on the CP monitor, causing a receive interrupt on the test UART
56	I BCFG High Pri Interrupt Recvd	A high priority BCRT interrupt was detected.
57	I CBAK CP IUART Reinitialized	The CP task has not received any messages from the formatter for two full scans. The internal UART is reinitialized. This will corrupt messages in progress going to the FP, if any.
58	I DBG Debug Message 1 Received	A generic event message used during integration which should not occur during normal operation.
59	I DBG Debug Message 2 Received	A generic event message used during integration which should not occur during normal operation.
5A	I DBG Debug Message 3 Received	A generic event message used during integration which should not occur during normal operation.
5B	I DBG Debug Message 4 Received	A generic event message used during integration which should not occur during normal operation.
5C	I Main MODIS TCP Flight Software	A startup event posted just before entering normal background processing for the first time. Should only appear on startup and reset.
5D	W TLM Format/Collect Mismatch	The telemetry subcommutation just formatted was not one of the two subcommutations collected during the most recent scan
5E	W SDSM Motor not at Target	The Trigger SDSM command was not able to reach its desired position during the most recent scan before the start of SD sector
5F	I SDSM Motor at Target	The Trigger SDSM command was able to reach its desired position during the most recent scan before the start of SD sector
60	I SUPR Serial Link Established	The CP has received a message from the FP after having previously lost communications.
61	W CIE Machine Error - RIP	A Machine Error interrupt has occurred. Since this is an unrecoverable error, the processor enters a loop waiting for the watchdog interrupt.
62	W CIE One Bit Error Corrected	The EDAC circuitry has detected and corrected a one-bit memory error.

TABLE 40-4. CONTROL PROCESSOR LOG EVENT CODES

Reference Information only. See 152932 Maintenance Manual of the MODIS Flight Software System.

Msg Hex Code	Msg	Interpretation/Description
63	W CIE Bogus Int 15 Handled	Processor interrupt 15 has occurred. There is a known CPU error which can cause this unused interrupt to occur. This event indicates that the processor has detected and handled this erroneous case.
64	W TLM Bad SDSM Table	This error indicates a coding error has developed in which the table used to store telemetry mux addresses for the SDSM detectors no longer matches the master lookup table.
65	W LLC Bad Mode Transition Cmd	The software attempted to process a mode sequence command which was not a parameter command, a relay command, a door command, or a relative motor step command.
66	W MTR Limit Steps to Maximum	The routine to initiate relative motor steps was invoked with a step count greater than the range from minimum to maximum for the motor. The step count was reduced to the maximum limit.
67	W MTR Clip Steps to Range	The routine to initiate relative motor steps was invoked for a motor with a hard stop and a step count which would drive the motor into the hard stop. The step count was reduced to halt stepping at the hard stop.
68	W MTR Bad Trigger Value	A coding error exists which specifies an improper trigger for a motor
69	W MTR NAD Trigger Not Found	The NAD motor was expecting a telemetry indication and reached the end of its stepping without receiving it. The software position of the motor is adjusted to the appropriate extreme limit.
6A	W MTR SDD Trigger Not Found	The SDD motor was expecting a telemetry indication and reached the end of its stepping without receiving it. The software position of the motor is adjusted to the appropriate extreme limit.
6B	W MTR SVD Trigger Not Found	The SVD motor was expecting a telemetry indication and reached the end of its stepping without receiving it. The software position of the motor is adjusted to the appropriate extreme limit.
6C	W MTR SDSM Trigger Not Found	The SDSM motor was expecting a telemetry indication and reached the end of its stepping without receiving it.
6D	W MTR GRAT Trigger Not Found	The SRCA Grating motor was expecting a telemetry indication and reached the end of its stepping without receiving it.
6E	W MTR FILT Trigger Not Found	The Filter Wheel motor was expecting a telemetry indication and reached the end of its stepping without receiving it.
6F	W MTR SLIT Trigger Not Found	The SRCA Slit motor was expecting a telemetry indication and reached the end of its stepping without receiving it. The software position of the motor is adjusted to the appropriate extreme limit.
70	W LLC Obs. Parameter Command	An obsolete parameter command was received and ignored.
71	W Main Bad Memory Block Found	The startup memory check detected at least one failed RAM page.
72	W Main Address State 1 Unmapped	The startup memory check detected so many failed RAM pages that it was unable to fully map the spare address state 1.
73	W BCRT Bad BCRT Interrupt Log	The BCRT interrupt handler was unable to decode the Interrupt Log data
74	W MCRO Bad Macro Index	An illegal macro index was specified.
75	W MCRO Unable to Load Macro	A memory transfer from EEPROM to RAM failed in the process of loading a macro. The macro command is aborted.
76	W LLC Lamps OFF Timer Violation	An attempt was made to send a new SRCA lamp command (SR12) within 3 seconds of the prior lamp command.
77	W TLM Late Telemetry Formatting	Telemetry was not completed by the fourth Synch with data word mode code since the last telemetry pickup, as required by the SRS
78	W LLC Illegal Mode Action	Certain CE/SR actions are not allowed in mode transition lists. One of these restricted commands was attempted during a mode transition.
79	W ICP Bad ROM CRC Detected	The background test of ROM completed a 4K page with a different result than the prior pass. The EEPROM has been modified or corrupted.

TABLE 40-4. CONTROL PROCESSOR LOG EVENT CODES

Reference information only. See 152932 Maintenance Manual of the MODIS Flight Software System.

Msg Hex Code	Msg	Interpretation/Description

NOTES

1. The SS_CP_LAST EVENT is a 16-bit word expressed as 4 hex values, which are partitioned as upper and lower 2-digits. The MSB, or upper 2-digits, is simply a sequence count that rolls over. The LSB, or lower 2-digits, are the Msg Hex Code listed in the table.

Table 40-4 Change History

1. 12/10/96 Table is new for Rev A.

TABLE 40-5. FORMAT PROCESSOR LOG EVENT CODES

Reference information only. See 152932 Maintenance Manual of the MODIS Flight Software System.

Msg Hex Code	Msg	Interpretation/Description
00	W IURT IUART Status Error	A status error occurred on the internal UART. This usually means the SW did not read a byte from the UART before the next byte arrived.
01	W FPMT Invalid Load Cmd Received	A Load Init command was received while a prior load command was still in process.
02	W FPMT Invalid Dump Cmd Received	A Dump Init command was received while a prior dump command was still in process.
03	W FPMT Internal Mem Xfer Failed	An attempt to read dump data or write load data was unsuccessful. For dumps, all zeros is returned.
04	W FPMT Invalid Dump Data from CP	Data to be loaded was received from the CP without a prior Load Init command.
05	W FPMT Invalid Load Data from CP	Data to be dumped was received from the CP without a prior Dump Init command.
06	W FPMT Load Checksum Failed	The checksum in the Load command did not match the checksum computed on the load data. The load data will be discarded.
07	W FPMT Load Init Cmd Garbled	An invalid load command was received over the serial link. The
08	W FPMT Dump Init Cmd Garbled	An invalid dump command was received. It is ignored and no data will be sent. This will cause an event on the CP when the dump data is
09	W FPMT EEPROM Load Failed	This obsolete event formerly indicated that an error occurred in the loading of EEPROMs via bus command
0A	I FPMT Memory Transfers Cleared	Any Load or Dump commands currently in process have been cancelled
0B	W FPMC Invalid Message - Ignored	The SW which processes messages received by the FP was instructed
0C	W MSGC Msg Registration Failed	Invalid parameters were specified in the call to register a message.
0D	W MSGC Invalid Xmit Parameters	The Send_Msg routine was called specifying an illegal or unregistered
0E	W MSGC Message Framing Error 1	An error was detected in the prefix of a message packet. This is most likely due to an overwritten byte in the UART.
0F	W MSGC Message Framing Error 2	The End of Packet delimiter was not found when expected. Most likely due to an overwritten byte in the UART.
10	W MSGC Message Buffer Overflow	More data has arrived for a message than can be held by the buffer allocated to that message
11	W ENCD Bad Frame State	The Frame Clock State machine was not in the DONE state when the Encoder State machine reached the START state.
12	W ENCD Linearity Check Bypassed	The SW controlling the linearity check has fallen behind. Enough linearity checks as required will be skipped to bring the SW up to date.
13	W ENCD Late Encoder Completion	The SW was unable to service the Encoder interrupt within the frame clock time which triggered the interrupt
14	W SECT Frame State Corrupted	The Frame Clock interrupt occurred with the Frame Clock State machine in the DONE or ERROR state. This occurs when the scan mirror electronics are not powered on, or are not receiving encoder pulses.
15	W SECT Invalid Sector	The mirror sector has changed within a single pass through the Frame Clock state machine.
16	W SECT Slow Header Generation	Packet header generation was incomplete when the Format Engine was disabled. This will often be accompanied by one or more of the PHG_SYNC_ERROR events.
17	W SECT Non-empty FIFO 1 swapped	FIFO 1 was swapped away from the FDDI before it emptied. Science data has been lost
18	W SECT Non-empty FIFO 2 swapped	FIFO 2 was swapped away from the FDDI before it emptied. Science data has been lost
19	W SECT Non-empty FIFO 3 swapped	FIFO 3 was swapped away from the FDDI before it emptied. Science data has been lost
1A	W SECT Non-empty FIFO 4 swapped	FIFO 4 was swapped away from the FDDI before it emptied. Science data has been lost

TABLE 40-5. FORMAT PROCESSOR LOG EVENT CODES

Reference information only. See 152932 Maintenance Manual of the MODIS Flight Software System.

Msg Hex Code	Msg	Interpretation/Description
1B	W SECT Bad Frame Count - End	The SW was unable to service the Frame clock interrupt within the frame clock time which triggered the interrupt
1C	W SECT APG Busy at FIFO Swap	The Aux Packets were not fully loaded when the FIFO swap occurred. An incomplete packet is in the FIFO.
1D	W PHG PHG Sync Error 1	At the start of a sector, the processing from the prior sector was not complete.
1E	W PHG PHG Sync Error 2	All the Dummy headers were consumed before the first set of real headers could be generated.
1F	W PHG PHG Sync Error 3	Headers are being consumed faster than they are being generated
20	W PHG PHG Sync Error 4	Headers are being consumed faster than they are being generated
21	W PHG PHG Sync Error 5	Headers are being consumed faster than they are being generated
22	W PHG PHG Sync Error 6	Headers from a prior sector remain to be loaded when it is time to send the dummy headers
23	W PHG PHG Sync Error 7	Headers were consumed during the loading of the dummy headers.
24	W PHG PHG Sync Error 8	THIS MESSAGE HAS BEEN REMOVED. IT SHOULD NEVER OCCUR.
25	W PHG SDB Init 1 Failed	A memory transfer failed while attempting to initialize the SDB during startup.
26	W PHG SDB Init 2 Failed	A memory transfer failed while attempting to load the fixed header fields into the SDB.
27	W PHG SDB Update Failed	A memory transfer failed while attempting to refresh the fixed header fields into the SDB.
28	W FIE Float. Overflow Received	A floating point overflow interrupt occurred
29	W FIE Fixed Overflow Received	A fixed point overflow interrupt occurred
2A	W FIE Float. Underflow Received	A floating point underflow interrupt occurred.
2B	W FIE Byte Arrived at Test Port	A key was pressed on the FP Monitor causing a receive interrupt on the test UART
2C	W APG Invalid Fill Bit Count	A fill bit count was specified which did not result in an integer number of 12-bit words
2D	W APG Checksum Algo Failed-Size	The checksum algorithm failed because a call to Load_FIFO specified a length greater than 32.
2E	W ACE Bad Readback FIFO Count	An incorrect amount of data is present in the Readback FIFO.
2F	W ACE Bad AEM Parameters	A command to set a single gain or offset was received with invalid parameters.
30	W ACE ACE Load Overrun	The mirror was not between the EARTH and SD sectors when the loading of gains and offsets was completed.
31	W FBAK FP IUART Reinitialized	The background task has not received any messages from the CP for two full scans. The internal UART is reinitialized. This will corrupt and messages in progress going to the CP, if any.
32	W Main WCS Load Failed	An memory transfer failed during the loading of the WCS from EEPROM
33	I DBG Debug Message 1 Received	A generic event message used during integration which should not be issued during normal operation.
34	I DBG Debug Message 2 Received	A generic event message used during integration which should not be issued during normal operation.
35	I DBG Debug Message 3 Received	A generic event message used during integration which should not be issued during normal operation.
36	I DBG Debug Message 4 Received	A generic event message used during integration which should not be issued during normal operation.
37	I Main MODIS FP Flight Software	A startup event posted just before entering normal background processing for the first time. Should only appear on startup and reset.
38	I MON Serial Link Established	The FP has received a message from the CP after having previously lost communications.

TABLE 40-5. FORMAT PROCESSOR LOG EVENT CODES

Reference information only. See 152932 Maintenance Manual of the MODIS Flight Software System.

Msg Hex Code	Msg	Interpretation/Description
39	W FIE Machine Error - RIP	A Machine Error interrupt has occurred. Since this is an unrecoverable error, the processor enters a loop waiting for the watchdog interrupt.
3A	W FIE One Bit Error Corrected	The EDAC circuitry has detected and corrected a one-bit memory error.
3B	W FIE Bogus Int 15 Handled	Processor interrupt 15 has occurred. There is a known CPU error which can cause this unused interrupt to occur. This event indicates that the processor has detected and handled this erroneous case.
3C	W FIE FIFO R/W Error Occurred	The FP attempted to access the FIFO memory when the FIFO was not in its test mode, or to access the Format engine memory while the format engine was running. A value of zero was returned for the read.
3D	W FIE Pixel Clock Unmasked	The FP received one or more pixel interrupts. The FP responds by masking out the interrupt.
3E	W Main Bad Memory Block Found	The startup memory check detected at least one failed RAM page.
3F	W Main Address State 1 Unmapped	The startup memory check detected so many failed RAM pages that it was unable to fully map the spare address state 1.
40	W FMC Bad Restart Address State	An invalid address state was received in a Restart command. The command is ignored.
41	W FIE FR_Int_02 Received	The level 2 interrupt was received from the CP. This interrupt is currently unused.
42	W FPMT Normal WCS Loaded	The Normal Mode WCS has been loaded into the Format Engine and the encoder state machine restarted.
43	W FPMT Test WCS Loaded	The Test Mode WCS has been loaded into the format engine and the encoder state machine restarted.
44	W MON Bad ROM CRC Detected	The background test of ROM completed a 4K page with a different result than the prior pass. The EEPROM has been modified or

NOTES

1. The SS_FR_LAST EVENT is a 16-bit word expressed as 4 hex values, which are partitioned as upper and lower 2-digits. The MSB, or upper 2-digits, is simply a sequence count that rolls over. The LSB, or lower 2-digits, are the Msg Hex Codes listed in the table.

Table 40-5 Change History

1. 12/10/96 Table is new for Rev A.

APPENDIX E. MODIS MISCELLANEOUS REFERENCE DATA

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Flight Software information presented here is for reference purposes. For more details or current data, see 152930 MODIS Flight Software Detailed Design (CDRL F306E).

HUGHES AIRCRAFT COMPANY

Santa Barbara Remote Sensing

Internal Memorandum

50.1

To: E. Clement

cc: L. Tessmer
R. Durham

Date: 12/11/96

Ref: PL3095-N02646B

Subject: MODIS Software Commands for On-Board Calibrator Control

From: D. Rogers/J.Auchter

Bldg. B32 **Mail Sta.** 58
Ext. 7146/7008

REFERENCE: 3/1/94 PL3095-N02646A MODIS Software Commands for On-Board Calibrator Control, to R. Julian, From D. Hanevich

INTRODUCTION

This memo completely replaces the Reference, and contains significant revisions. Figure 1 shows how three MODIS On Board Calibrators (OBCs) are controlled. It indicates that power for individual OBCs is directly controlled by Telemetry and Command Processor (CP) relay commands, and that all other OBC configuration commands and bilevel telemetry are processed over 16-bit serial links. This memo defines the software (SW) protocol for the 16-bit links. MODIS Flight SW accommodates The lamp commands defined here have simpler user-friendly commands described in the 151840 MODIS Command, Telemetry, Science and Engineering Description, which must be transformed by the Flight SW into the following protocol definitions.

HARDWARE

The hardware elements addressed here are 1) redundant TCP 3-CCA set: 404873 SBC A11/12A1, 404879 Digital TLMY A11/12A2 & 404882 Analog Tlmy A11/12A3, 2) the 404903 Cal Control 1 A17 CCA, 3) 404904 Cal Control 2 A18 CCA, 4) 405360 BB Assy, 5) 405500 SDSM and 6) 405400 SRCA Assy. The Cal 1 and CAL 2 CCAs function together to provide the overall required cal driver and OBC support functions. The Cal 1 CCA and Cal 2 have unique functions, which are redundant on each CCA. The serial link to Cal 1 has command, telemetry, clock and control lines.

SOFTWARE SERIAL DATA FORMAT

All calibrator commands and telemetry are written or read from CP address CXX01. The 16-bit words are partitioned into an address high byte and a data low byte.

Commands - - OBC function commands are sent as 16 bit words with the MSB of the command address byte sent first, followed by the MSB of the command data byte. Data is clocked in on the rising edge of the serial clock after the command enable signal rises. A function command sets the address MSB low (0). Initiation of a command automatically results in a Command Echo Telemetry.

Command Echo Telemetry - - When a command is sent with its address low, a telemetry command echo is returned, which exactly matches the 16 bit command. This can be used to verify link interface integrity.

Telemetry Request - - A telemetry request is initiated by setting the address MSB high (1) and the LSB of the data byte is set to select either the telemetry low status byte or the telemetry high status byte.

Tables 1 - 9 provide particular OBC command and telemetry protocol definitions.

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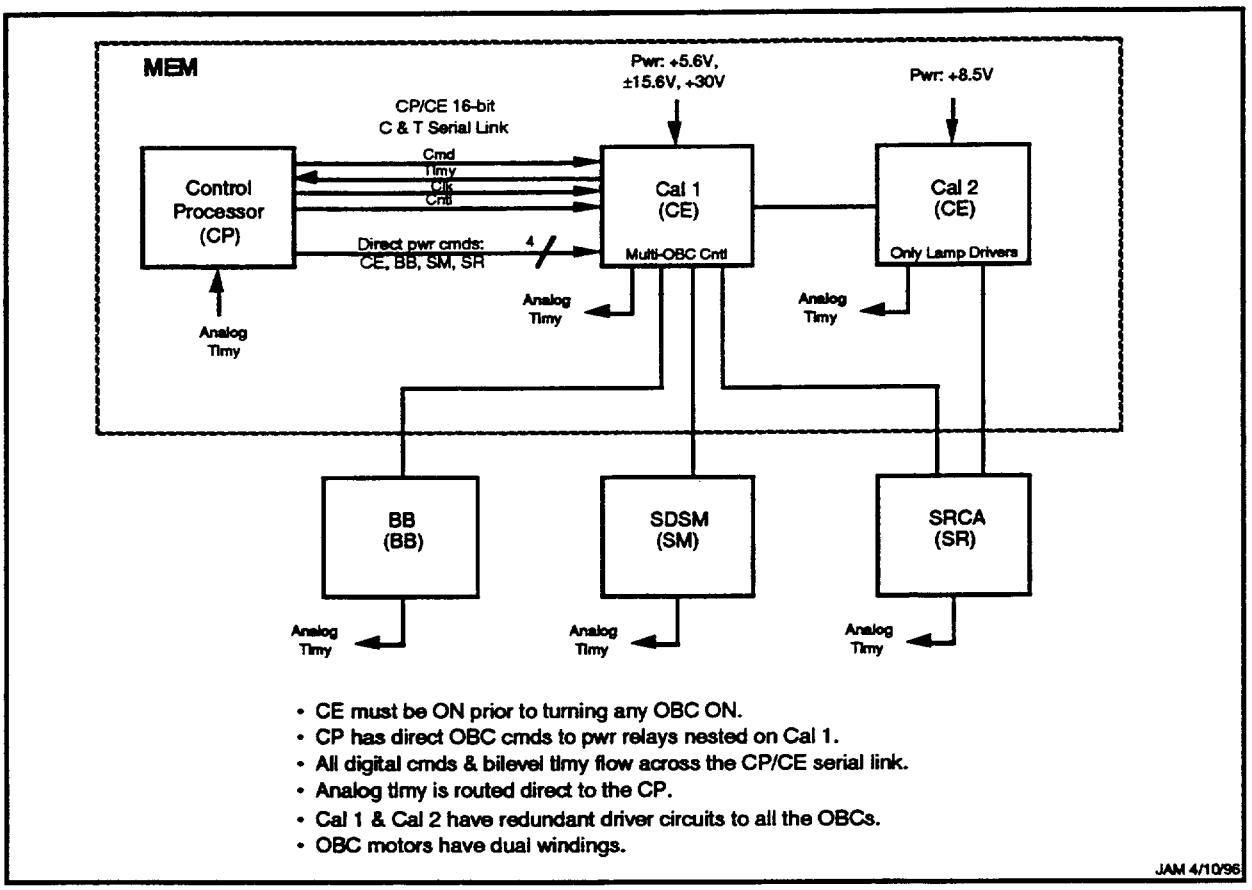

Figure 1. MODIS OBC CONTROL DIAGRAM

GENERAL FEATURES

As mentioned in the Introduction, the Control Processor Flt SW transforms OBC user-friendly command formats into the structured 16-bit form needed to flow over the serial link for proper control of the OBC's. The low byte data control word contains several individual functional control bits. The Flt SW maintains relational cognizance of these when a single bit may be the only changed bit for a new functional selection.

The Control Processor Flt SW provides all algorithms or special control routines, e.g., heated BB control, OBC motor stepping, etc.

A sample of a special control routine, is the initiation sequence for properly turning the SRCA lamps ON/OFF due to the initial unknown state of the HW. This is addressed in detail under Table 6.

Table 1. Blackbody Commands

Bits (MSB=15)	Function	Value
15-8	Opcode	00000000
7-1	Spare	Don't Care
0	BBDY Heater Control	0 = Heater OFF 1 = Heater ON

Table 1 shows the command format for control of the blackbody heater. A simple control equation that will serve as a basis for the blackbody is as follows: (Tnow + (2*(Tnow-Told) is compared to the set point where (Tnow) is the present temperature and (Told) is the temperature from the last reading. Temperture T is the weighted average of the 12 BB temperature sensors. Present SW weighting is such that only sensors 3, 4, 9 & 10 are used.

Table 2. OBC Stepper Motor Commands

Bits (MSB=15)	Function	Value
15-8	Opcode (Selects Motor)	FILT = 00000011 SDSM = 00000100 GRAT = 00000101 SLIT = 00000110
7-3	Spare	Don't Care
2-0	Phase Control (D2, D1, D0)	See Table 3 for phase codes

Table 3. OBC Motor CW Phase Sequence

Sequence	D2 (Ph A)	D1 (Ph B)	D0 (Ph C)
1	1	1	0
2	1	0	0
3	1	0	1
4	0	0	1
5	0	1	1
6	0	1	0

Tables 2 and 3 show the command format for control of the stepper motors in the calibrator. The sequence given in Table 3 produces clockwise rotation of the motor per 151785 MEM Spec. For rotation of related mechanism and additional data regarding stepper motor operation, see 151840 Commands, Telemetry, Science & Engineering Description . To increase step count, some motors go CW and some go CCW.

In order to initialize motor drive phase sequence after turn ON, the OBC motors are advanced forward 6 steps minimum, then commanded to find Home by external STE CSTOL command procedures.

Table 4. SRCA Mode Command 1

Bits (MSB=15)	Function	Value
15-8	Opcode	00000001
7-4	Spare	Don't Care
3	SIS SiPD Heater Control	0=OFF, 1=ON
2	SIS Lamp Control	0=OFF, 1=ON
1	IR Source Control	0=OFF, 1=ON
0	SIS Feedback Mode	0=CURRENT 1=RADIANCE

Table 4 shows the format for controlling a number of bit settings in the SRCA. Since the entire word must be written, the state of each bit must be maintained in software and resent to the calibrator each time any of the bit settings needs to be changed. The Lamp Control bit is used to send power to the configuration of lamps selected by the Lamp command shown in table 6.

Table 5. SRCA Mode Command 2

Bits (MSB=15)	Function	Value
15-8	Opcode	00001000
7-2	Spare	Don't Care
1	Overvoltage Shutdown	0 = ENABLED 1 = DISABLED
0	SRCA Lamp Level	0 = LOW 1 = HIGH

Table 5 shows the format for controlling additional settings in the SRCA. Since the entire word must be written, the state of both bits must be maintained in software and resent to the calibrator each time either of the bit settings needs to be changed. The lamp level HIGH is the normal operating mode.

Table 6. SRCA Lamp Commands

Bits (MSB=15)	Function	Value
15-8	Opcode	00000010
7-6	Spare	Don't Care
5	Lamp 6 Control	0=OFF, 1=ON
4	Lamp 5 Control	0=OFF, 1=ON
3	Lamp 4 Control	0=OFF, 1=ON
2	Lamp 3 Control	0=OFF, 1=ON
1	Lamp 2 Control	0=OFF, 1=ON
0	Lamp 1 Control	0=OFF, 1=ON

Table 6 shows the format for commands used to control the selection of SRCA visible lamps. Lamps 1-4 are 10W lamps. Lamps 5 and 6 are 1W lamps. The calibrator has a hardware lockout that shuts all lamps off (which triggers the over voltage shutdown if it is enabled) if an invalid command is requested. Requesting more than 3 of the 10 watt lamps (#1,2,3 or 4), more than 1 of the 1 watt lamps (#5,6) or requesting any combination of 10 watt and 1 watt lamps are invalid commands, which should also be rejected by Flight SW.

Due to unknown HW states, Flight SW will provide the following automatic initializing sequence whenever the CE or SR are turned on: 1) Turn Lamps Off, 2) disable lamp overvoltage shutdown, 3) wait 3 sec, then load lamp codes to all zeros (0000-00), & 4) enable lamp overvoltage shutdown. During the 3 sec delay, Flight SW will reject CP/CE link commands for lamps to Off/W1/W10/W20/W30.

Table 7. Command To Send Telemetry

Bits (MSB=15)	Function	Value
15-9	Opcode	1000000
8	Byte to Send	0=LOW, 1=HIGH
7-0	Spare	Don't Care

Table 7 shows the format for the commands used to request telemetry from the calibrator. The telemetry data can be read back from the calibrator port 20 microseconds after the command is sent to the calibrator.

Table 8. Telemetry Low Byte Format

Bits (MSB=15)	Function	Value
15-8	Unused	Don't Care
7	* BBDY Heater State	0=ON, 1=OFF
6	* IR Source State	0=ON, 1=OFF
5	* SIS SiPD Heater State	0=ON, 1=OFF
4	* SIS Feedback Mode	0=RADIANCE 1=CURRENT
3	* Overvoltage Shutdown	0=DISABLED 1=ENABLED
2	* SIS Lamps State	0=ON, 1=OFF
1	SDSM Encoder A	0=HOME, 1=AWAY
0	SDSM Encoder B	0=HOME, 1=AWAY

Table 8 shows the format of the lower byte of the calibrator status word. Items marked with an asterisk are not currently available from the calibrator hardware, but may be implemented in the future. If the missing telemetry is required, the software must retain a copy of the most recently sent commands and determine from this record the current state of the hardware. Since both A/B encoders are powered whenever SRCA Side A or Side B is powered, both encoder side telemetry is valid.

Table 9. Telemetry High Byte Format

Bits (MSB=15)	Function	Value
15-8	Unused	Don't Care
7	Grating Coarse Encoder A	0=HOME, 1=AWAY
6	Grating Fine Encoder A	0=HOME, 1=AWAY
5	Slit Encoder A	0=HOME, 1=AWAY
4	Filter Wheel Encoder A	0=HOME, 1=AWAY
3	Grating Coarse Encoder B	0=HOME, 1=AWAY
2	Grating Fine Encoder B	0=HOME, 1=AWAY
1	Slit Encoder B	0=HOME, 1=AWAY
0	Filter Wheel Encoder B	0=HOME, 1=AWAY

Table 9 shows the format of the upper byte of the calibrator status word. For the Grating motor, the Coarse Encoder is active (i.e., home) over a single range of steps. The Fine Encoder is active for a single step at multiple positions throughout the motor rotation. The true Home position is when both the Coarse and Fine Encoder telemetry points are active. Since both A/B encoders are powered whenever SRCA Side A or Side B is powered, both encoder side telemetry is valid.

50.2 MODIS RESET/UPLOAD DESCRIPTION

50.2.1 Introduction.

The following summarizes the activities which take place after a reset to the MODIS processors. Differences between the two processors (Control Processor or Formatter Processor) will be noted below as needed.

1. Upon coming out of reset, the Startup ROM (SUROM) is enabled. This means that the lower 32K of RAM memory (physical memory addresses 00000-07FFF) is not available. Instead, the 8K SUROM is mapped into these locations (nothing exists from 02000-7FFF in this mode).

2. The code in the SUROM performs a memory test of the physical memory RAM addresses 08000-1FFFF.

3. When this test is complete, the boot code is copied from the SUROM into two pages of RAM which passed the memory test described above.

4. Execution is then transferred into the RAM copy of the startup code.

5. The SUROM is disabled, making the RAM from 00000-07FFF visible. The newly available RAM memory is tested.

6. With all failed memory blocks located, address state zero in the processor is allocated using only pages which passed the memory test. Within address state zero, logical pages 0-6 are mapped to RAM, pages 7 and 8 are mapped to the system registers, pages 9-13 are mapped to RAM. Pages 14 and 15 were mapped to RAM during step 3 above. Operand and Instruction pages are mapped identically; that is, instructions and data occupy a single 64K unpaged address space.

7. The system register containing reset information is checked. This register exists at logical address 800A in the Control Processor and at logical address 801B in the Format Processor. For each of the possible resets, there is a single bit in the resets register. The bits are active low. If the bit corresponding to the upload reset is low, the processor transfers control to a small upload program, described below. If the upload bit is high, a standard reset is assumed.

8. For a standard reset, the Flight Software is copied from EEPROM addresses 80000-8CFFF to logical addresses 0000-CFFF (skipping the pages mapped to the system registers). The actual RAM addresses used will be determined by the results of the memory tests performed in steps 2 and 5, above. Note that the RAM copy of the Startup code is loaded into logical addresses E000-FFFF, which are not loaded from EEPROM. This address range is used as stack and heap by the flight software, and so does not need to be loaded.

9. Control is transferred to address 0000 of the flight software program and normal execution begins.

50.2.2 Upload Mode.

In step 7 above, if an upload reset is detected, control is transferred to the upload code, also stored in the Startup ROM, and copied over to the RAM as part of step 3. As defined in the 152928 Flight software Requirements Specification, CDRL F306B, the Upload code exists to provide a means of loading an entirely new program into the MODIS instrument. This would be used, for example, if the EEPROMs containing the flight software failed. The upload module is different for each processor. These modules are derived from the actual flight software by starting with the full flight software module and removing functions not required for the upload activity until the resulting code fits into the 8K Startup ROM along with the startup code described above.

In the Control Processor, the main functions supported in the upload mode are the 1553 interface code, the command interpreter, and the memory transfer modules. In the Formatter, the functions supported in the upload mode are the internal serial link code and the memory transfer modules. Note that this means that both MODIS processors cannot be in upload mode simultaneously, since the internal serial link is not supported by the Control Processor upload module. If both processors need to be uploaded with new code, the Control Processor can be loaded first, the new Control Processor program run, followed by commands to set the Formatter into upload mode for its reprogramming. The command interpreter in the Control Processor Upload code supports only the commands: MEMORY_LOAD_INITIATE, MEMORY_DUMP_INITIATE, MEMORY_TRANSFER_CLEAR, RESTART

The MEMORY_LOAD_INITIATE and MEMORY_DUMP_INITIATE commands behave as in the flight software, with the following exceptions: 1) Table load and dumps are not supported, as the flight software to which those tables refer do not exist in Upload mode. 2) accesses to the Format Processor are not supported, as noted above. The MEMORY_TRANSFER_CLEAR command cancels all load and dump transactions currently in progress. The RESTART command specifies a jump address which is the starting address of the newly loaded program.

50.2.3 Possible Conflict.

In upload mode, the MODIS instrument cannot generate telemetry as defined by 151840. There is not enough room in the 8K Startup ROM to support this. Options for the Housekeeping Telemetry subaddress are as follows: 1) Disable this subaddress so that no telemetry data is generated by the MODIS instrument. 2) Enable the subaddress, and place a fixed set of data into it. This would require defining a single bit, which would indicate that the telemetry data is not to be used for ground processing (or for any other reason). Critical housekeeping temperature and bilevel status telemetry processed by the Spacecraft BDU will still be available

Will either of these solutions, disabling the subaddress or enabling with a fixed buffer and a Not_For_Ground flag (TLM_NFG) result in alerts being set off on the spacecraft or the ground which would need to be disabled before sending the upload reset command?

50.3 MODIS MEMORY TYPES & REMARKS

50.3.1 Memory Types. There are four basic types of memory which can be accessed for loads and dumps:

1. MODIS Tables
2. Instruction Logical
3. Operand Logical
4. Physical

Physical memory is the actual hardware address of the various memory chips and other devices. Logical memory (Instruction and Operand) is used by the processor memory management unit and is generally of interest only to the software. Tables are a special case of Operand Logical memory and represents locations where certain pre-defined MODIS data structures are located.

There is an internal limit to the amount of data which can be transferred (load or dump) by a single bus command. This limit is 32 words.

50.3.2 RAM/EEPROM vs Address types. RAM is located at physical addresses 00000-1FFFF (hex). EEPROM is located at physical addresses 80000-93FFF(HEX).

50.3.3 Memory Dumps. Dumps can be performed from any memory address in either processor. This includes RAM, EEPROM, and in the case of the Format Processor, the Science Data Buffer and Format Engine Writable Control Store. Dumps can be sent down via the 1553 or the High Rate Data Link (HRDL), in which case it is embedded in the Memory Data packet.

50.3.4 Memory Loads. Loads can be performed to any memory address in either processor. Loads to EEPROM require extra processing, as the EEPROM write enable commands must be properly interleaved with the memory load commands, as described below.

50.3.5 Halt CP RAM XFER. MODIS has a HALT_CP_RAM_XFER command that can halt load or dump activities if it is sent before they are completed. It functions in the following manner.

MODIS requires each 32-word load to be prefixed with a load initiate command. The MODIS CP (which has the 1553 interface) is responsible for routing load init commands and load data to the FP across an internal serial link. Each processor keeps track of where it is in the load process.

The states on the CP are INACTIVE, INITIATE_RECEIVED, and WAITING_FOR_VERIFY.

The states on the FP are INACTIVE and WAITING_FOR_DATA.

The normal state on both processors is INACTIVE. The processors move through the different states as the load initiate commands and data are received over the 1553, and possibly relayed over the serial link. If any load activity takes place when the processor is in a state when it is not expecting that activity, the action is not performed, and the state for that processor is set to INACTIVE.

The main use of the HALT_CP_RAM_XFER command is to reset the handshaking between the spacecraft and the two MODIS on-board processors. If there is some sort of failure in the load or dump process, either processor could be left in one of its non-INACTIVE state. The HALT_CP_RAM_XFER will reset the state of both processors to INACTIVE.

50.4 FLIGHT SOFTWARE COMPONENT CHECKSUMS

There are 5 components of the flight software stored in EEPROMs which can be changed via commands from the test equipment (or ground control equipment) The five components are:

1. Control Processor (CP) Flight Software
2. CP Macro Table
3. Format Processor (FR) Flight Software
4. Normal Mode WCS
5. Test Mode WCS

Items 1 and 2 are installed in the CP, items 3-5 are installed in the Format Processor. In order to provide confirmation of which version of each component is loaded in the instrument, the flight software on each processor computes a 16-bit word CRC checksum over the appropriate range of EEPROM for each component (CRC = Cyclic Redundancy Checksum, which is described in 50.5. These five values are reported out in the CP telemetry panel as the following points (the values given are for the currently released versions of each component):

	Telemetry Point	Value	Component
1.	SS_CP_STATUS_04:	992E	CP Flight Software
2.	SS_CP_STATUS_05:	2E82	CP Macro Table.
3.	SS_CP_STATUS_06:	0E9F	FP Flight Software
4.	SS_CP_STATUS_07:	2180	Normal Mode WCS
5.	SS_CP_STATUS_08:	9A72	Test Mode WCS

Each time a re-release of any of these software components occurs, the software description document (154133) is updated and new checksums are computed for the altered components. Note that points SS_CP_STATUS_06 _07 and _08 are computed by the FP, and so will have a value of 0000 until the formatter is turned on.

50.5 MODIS FLIGHT SOFTWARE CRC CHECKSUM ALGORITHM

The CRC checksum algorithm used throughout the MODIS flight software is an adaptation of a table driven algorithm given in an article in Embedded Systems Programming's January 1992 issue called implementing CRCs by Jack W. Crenshaw (pp. 18-45). This CRC algorithm can detect:

100% of all single bit errors.

100% of all two bit errors.

100% of all odd numbers of errors.

100% of all burst errors less than 17 bits wide.

99.9969% of all bursts errors 17 bits wide.

99.9985% of all bursts wider than 17 bits.

The mathematics underlying the algorithm will not be discussed here, only a description of the final algorithm. One of the advantages of this algorithm is that it can be reduced to simple table lookups and bit level operations: AND, XOR, shifting.

The algorithm will be described from the bottom-level up. Since the 1750A processor is a 16-bit architecture, all of the computations which follow are performed using 16-bit integers. The CRC value itself is a 16-bit integer.

Begin by defining a table of 256 integers, indexed from 0-255. The table has fixed values and is initialized using the following algorithm:

```
FOR i IN 0 .. 255 LOOP
    X = i XOR (i shifted left 4 bits);
    Y = lower byte of X;
    Z1 = Y shifted  left 8 bits;
    Z2 = Y shifted  left 3 bits;
    Z3 = Y shifted right 4 bits;
    CRC_Table(i) = (Z1) XOR (Z2) XOR (Z3);
END LOOP;
```

The CRC_Result on a single byte is a function of the byte to be processed and the prior value of the CRC, as shown below:

```
function Process_Byte(Input_Byte, OLD_CRC) return integer is
begin
    Table_Index = Input_Byte XOR (Lower Byte of OLD_CRC);
    NEW_CRC = (Upper Byte of OLD_CRC) XOR CRC_Table(Table_Index);
    return NEW_CRC
end Process_Byte;
```

To process a 16 bit word, process the upper byte first, then the lower.

To process a block of N 16-bit words, use an initial CRC value of 0, and call the function Process_Byte in the following manner:

```
Set CRC_Result = 0;
FOR i IN each of the N words LOOP
    Set Upper_Byte to the upper byte of word i;
    Set Lower_Byte to the lower byte of word i;
    CRC_Result = Process_Byte(Upper_Byte, CRC_Result);
    CRC_Result = Process_Byte(Lower_Byte, CRC_Result);
END LOOP;
```

The final returned value for CRC_Result is the CRC for the block.

50.6 USER CONTROLLED MODIFICATIONS TO THE DC RESTORE FUNCTION

This section summarizes how to use several highly specialized test commands to facilitate temporarily installing particular PV gain and/or PV & PC offset values to accommodate various ambient test conditions. They should only be used by experienced test/operations personnel.

The initial value for Gain and Offset of each FPA channel has been determined by SBRS Systems Engineering from various system tests. The default value for the DC Restore function is ON for both PV and PC bands. Thus, by default, the flight software will attempt to keep all channels within their dynamic range. For testing or checkout purposes, the users may wish to apply specific gain or offset values to the electronics. There are several means by which this can be performed as described below.

50.6.1 All channel table upload. Using this method, a completely new table of gain or offset values can be loaded for all FPA channels (except PC gains). In this case, the previous values in the table are lost, and cannot be recovered. In general, the DC Restore option should be disabled, since if it is left enabled, the software may begin changing the loaded values, which is probably not desired. To disable the DC Restore function for both PV and PC bands, issue the following commands:

```
SET MOD FR_PV_DCRCMP TO OFF
SET MOD FR_PC_DCRCMP TO OFF
```

50.6.2 Single channel change. If the user is focusing on a particular channel, or a small number of channels, the software provides several commands for changing a single parameter in the gain or offset tables. Again, the users will probably want to turn off the DC Restore function as described above, for similar reasons. As above, the previous value for the individual channel being modified will be lost. The following commands illustrate the use of this feature:

A. SET MOD FR_PVGN1C WITH B 1, C 25, V X#23

B. SET MOD FR_PVOS1C WITH B 19, C 7, V 100

C. SET MOD FR_PCPREOS1C WITH B 32, C 10, V 128

D. SET MOD FR_PCPSTOS1C WITH B 36, C 3, V 34

Command A shows the form of the command to set a single value in the Gain Table. This command applies only to the PV bands, since the PC bands have fixed gains. In this command the value following the B is used to select the band, and must be in the range 1-30; the value following the C selects the channel, and has limits which are band specific as listed in the table below; the value following the V is the new gain value, and must be in the range 0-255.

Band	Channel Limits
1-2	1-40
3-7	1-20
8-12	1-10
13-14	1-20
15-30	1-10
31-36	N/A

Bands 13 and 14 require further discussion. Each channel in these bands actually consist of two detectors, whose outputs are averaged into a single output value. Furthermore, each pair is sampled twice, once with High gain and once with low gain. For simplicity of the command structure, channels 1-10 in these bands refer to the samples with low gain and channels 11-20 refer to the samples with high gain. The detector pairs each receive the same gain value. Note the designations High and Low are arbitrary, in that the gain value called high can be set to any legal value, and need not be higher than the value called Low.

Command B shows the command to set a single PV Offset value. The parameters are identical to the parameters for the single channel gain command, and the same limits, definitions and restrictions apply.

Commands C and D show how to modify the preamp and postamp offsets for the PC bands. In both commands, and the band must be in the range 31-36, the channel must be in the range 1-10. The postamp value must be in the range 0-255, and the preamp value must be in the range 0-63.

50.6.3 Override table values with a single value. The software provides a means of temporarily overriding the values in the gain and offset tables. When using these commands, it is strongly recommended that the DC Restore function be turned off. The following commands show how this value might be used:

```
SET MOD FR_PV_DCRCMP TO OFF
SET MOD FR_PC_DCRCMP TO OFF
TEST MOD FR_PVOFFSET WITH OS 134
SET MOD FR_OFFSETTAB TO TEST
SET MOD FR_OFFSETTAB TO NORMAL
SET MOD FR_PV_DCRCMP TO ON
SET MOD FR_PC_DCRCMP TO ON
```

The first two commands turn off the DC Restore function, as recommended. The third command says that when the override function is enabled, the value to use is 134. The fourth command enables the override. From this point on, the values in the Offset table are ignored, and an offset value of 134 will be sent out for all PV channels. When the fifth command is sent, the table values will once again be used. During the time that the override function is enable, the offset table can still be loaded, and if the DC Restore function is not turned OFF, the values can be modified, but will not be sent out.

A similar function exist for the PV Gain table.

```
TEST MOD FR_PVGAIN WITH GN 96
SET MOD FR_GAINTAB TO TEST
SET MOD FR_GAINTAB TO NORMAL
```

For the PC bands, there is one TEST command used to specify both the preamp and postamp override values. Once again, DC Restore should be turned off when this feature is used:

```
SET MOD FR_PV_DCRCMP TO OFF
SET MOD FR_PC_DCRCMP TO OFF
TEST MOD FR_PCOFFSET WITH OS X#5A95
SET MOD FR_OFFSETTAB TO TEST
SET MOD FR_OFFSETTAB TO NORMAL
SET MOD FR_PV_DCRCMP TO ON
SET MOD FR_PC_DCRCMP TO ON
```

In this case, the second command above specifies that the override values be 90 decimal, (5A hexadecimal) for the preamp offsets and 149 decimal (95 hexadecimal) for the postamp offsets.

Additionally, the table of ideal blackbody sector outputs can be overridden by a similar technique. When used, this feature will ignore the 36 band by 50 temperature table normally used to determine the offsets and instead uses a single value for all bands and channels. DC Restore need not be turned off when using this feature.

```
TEST MOD FR_BBRAD WITH OS 134
SET MOD FR_BBRADTAB TO TEST
SET MOD FR_BBRADTAB TO NORMAL
```

Finally, there is a "Fast Restore" function for the PV bands. This function performs a binary search through the offset range in a attempt to quickly locate the optimal value. Once commanded, this search can take up to eigth scans (approximately 12 seconds) to complete, and should not be interrupted. During this search, the output of the PV channels will jump about significantly during the first few scans, and gradually settle about the ideal value. The command to start the Fast Restore function is:

```
TOGGLE MOD FR_INT_02
```

50.7 SCAN DATA COLLECT SHIFT BY DELTA ENCODER COUNTS

Formatter command FR31 (SET_FR_ENC_DELTA TO 0,-8192,+8192) provides a simple way to globally shift all the scan view data collects by the selected encoder count delta. This allows placing the large 1354 FD Earth collect window over other views or internal scan cavity features.

Figure 50-1 graphically illustrates the process for a sample encoder delta of -2900 counts, which nearly places the center of the Earth collect over the center of the BB view. Simple calculations provide relations between Encoder count shifts and Frame of Data (FD) shifts. The Encoder period is 180.318 µs and the sample FD period is 333.333 µs.

The start of the five scan views are defined in terms of Encoder counts and Vernier counts as listed in Table 30-5B. Vernier counts are insignificant compared to the large Earth collect window, and are ignored for Encoder Delta operations.

Before commanding an Encoder delta count, the PC and PV DCR functions should be turned Off. The BB view is used to provide the DCR reference, but the shifted BB collect may end up over an undesirable background level to establish valid DCR values.

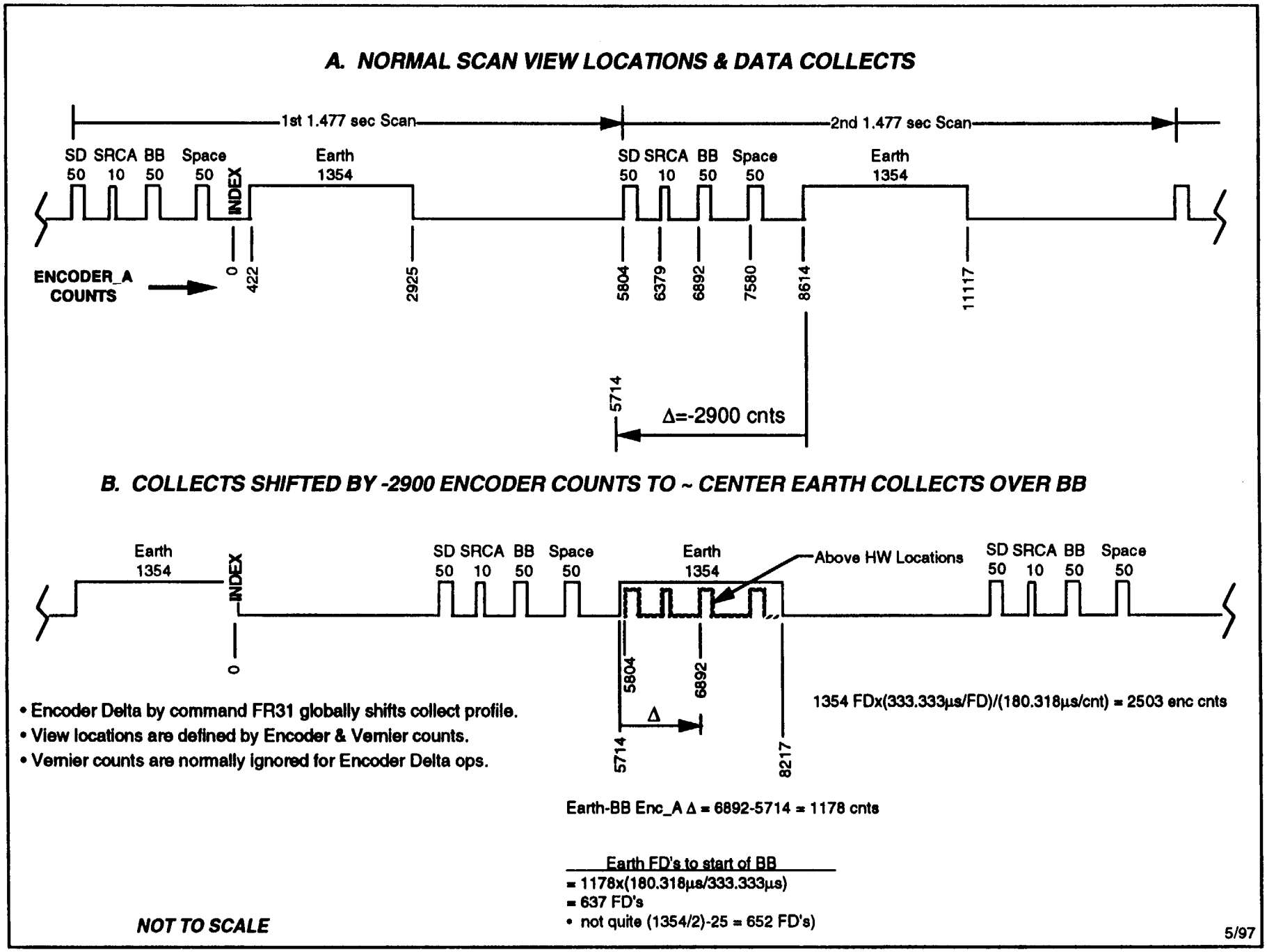

Figure 50-1. Scan Collect Shift by Delta Encoder Counts